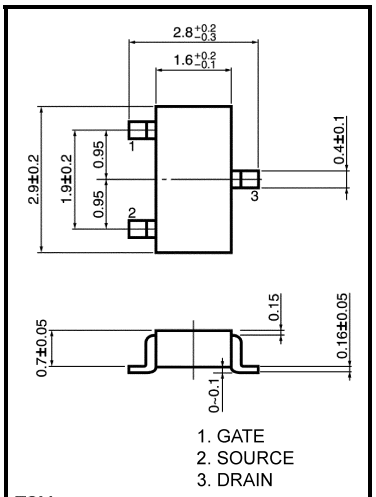
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K02T

High Speed Switching Applications

- Small package
- Low on resistance: R_{on} = 200 mΩ (max) (V_{GS} = 4 V)
  : R_{on} = 250 mΩ (max) (V_{GS} = 2.5 V)
- Low gate threshold voltage: V_{th} = 0.6~1.1 V (V_{DS} = 3 V, I_D = 0.1 mA)

Unit: mm



1. GATE
2. SOURCE
3. DRAIN

TSM

JEDEC	—
JEITA	—
TOSHIBA	2-3S1A

Weight: 0.01 g (typ.)

Maximum Ratings (Ta = 25°C)

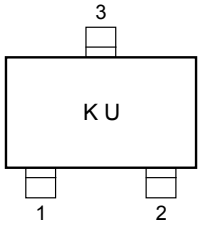
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	2.5	A
	Pulse	I_{DP}	5.0	
Drain power dissipation (Ta = 25°C)		P_D (Note1)	1250	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note1:Mounted on FR4 board

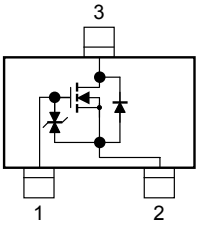
(25.4 mm × 25.4 mm × 1.6 t, Cu pad: 645 mm^2, t = 10 s)

Note2: The pulse width limited by max channel temperature.

Marking



Equivalent Circuit



Handling Precaution

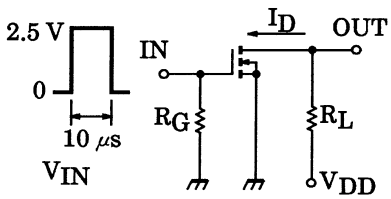
When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

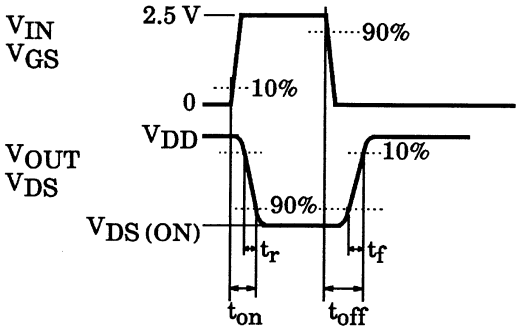
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±5	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 1 mA, V_{GS} = 0	30	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.6	—	1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 1.25 A (Note)	2.2	—	—	S
Drain-source ON resistance		$R_{DS(ON)}$	I_D = 1.25 A, V_{GS} = 4 V (Note)	—	140	200	mΩ
			I_D = 1.25 A, V_{GS} = 2.5 V (Note)	—	180	250	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	115	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	24	—	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	60	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 15 V, I_D = 0.5 A, V_{GS} = 0~2.5 V, R_G = 4.7 Ω	—	52	—	ns
	Turn-off time	t_{off}		—	80	—	

Note: Pulse test

Switching Time Test Circuit



V_{DD} = 15 V
R_G = 4.7 Ω
D.U. ≦ 1%
V_{IN} : t_r, t_f < 5 ns
COMMON SOURCE
Ta = 25°C



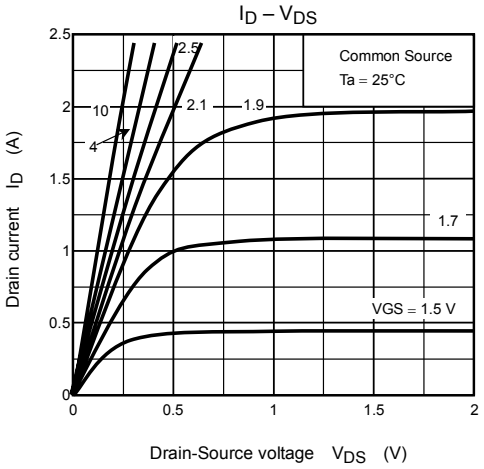
Precaution

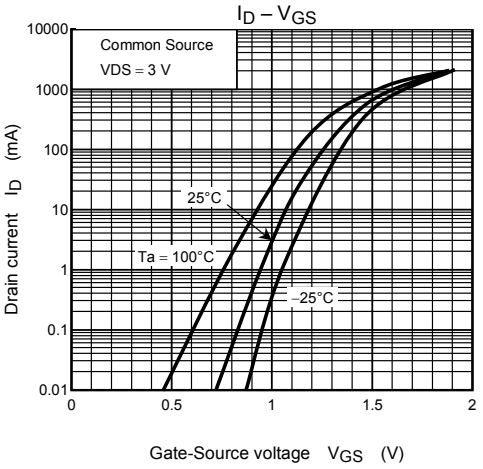
V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = 100 μA for this product. For normal switching operation, $V_{GS(ON)}$ requires higher voltage than V_{th} and $V_{GS(off)}$ requires lower voltage than V_{th}.

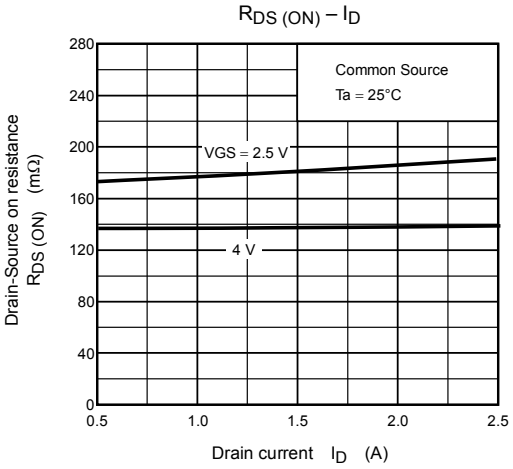
(Relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(ON)}$)

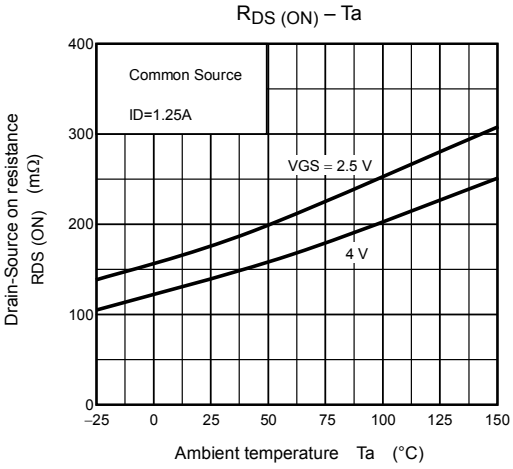
Please take this into consideration for using the device.

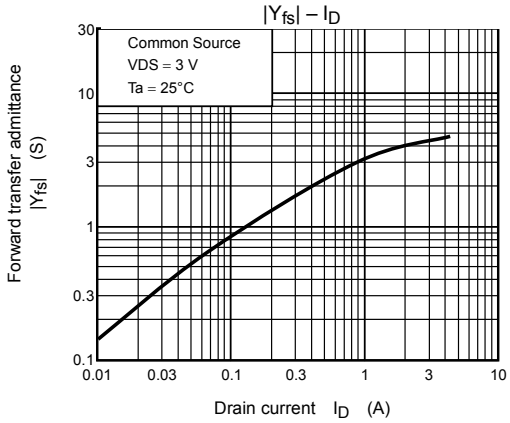
V_{GS} recommended voltage of 2.5 V or higher to turn on this product.

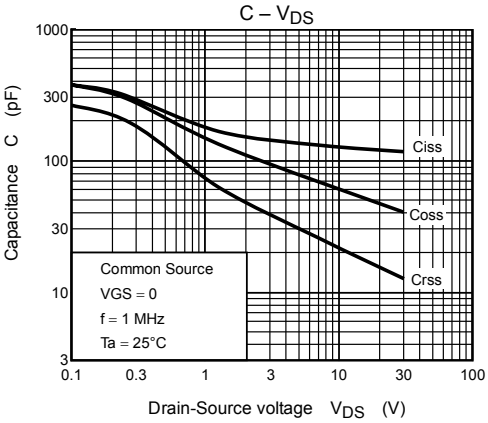

ID – VDS
Common Source
Ta = 25°C
10
4
2.5
2.1
1.9
1.7
VGS = 1.5 V
Drain current ID (A)
Drain-Source voltage VDS (V)


ID – VGS
Common Source
VDS = 3 V
25°C
Ta = 100°C
−25°C
Drain current ID (mA)
Gate-Source voltage VGS (V)


RDS (ON) – ID
Common Source
Ta = 25°C
VGS = 2.5 V
4 V
Drain-Source on resistance RDS (ON) (mΩ)
Drain current ID (A)


RDS (ON) – Ta
Common Source
ID=1.25A
VGS = 2.5 V
4 V
Drain-Source on resistance RDS (ON) (mΩ)
Ambient temperature Ta (°C)


|Yfs| – ID
Common Source
VDS = 3 V
Ta = 25°C
Forward transfer admittance |Yfs| (S)
Drain current ID (A)


C – VDS
Ciss
Coss
Crss
Common Source
VGS = 0
f = 1 MHz
Ta = 25°C
Capacitance C (pF)
Drain-Source voltage VDS (V)

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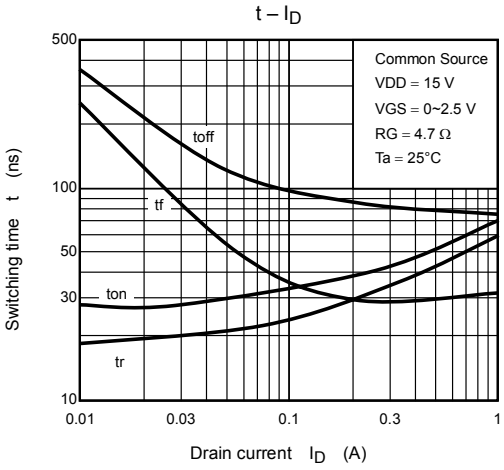
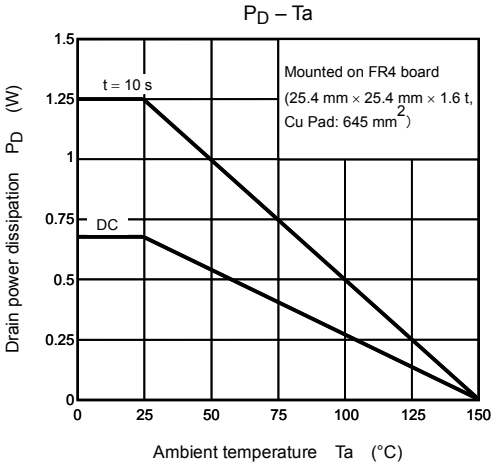
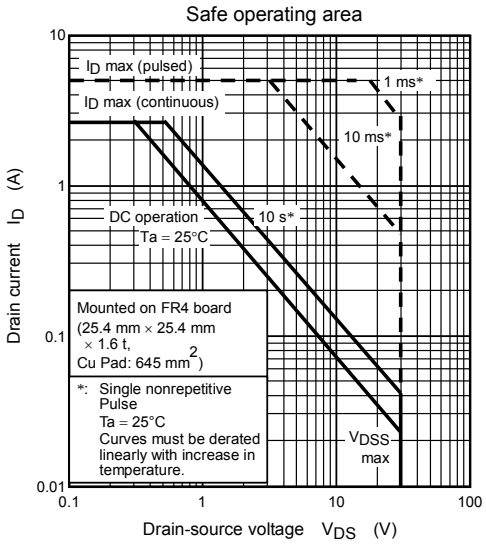
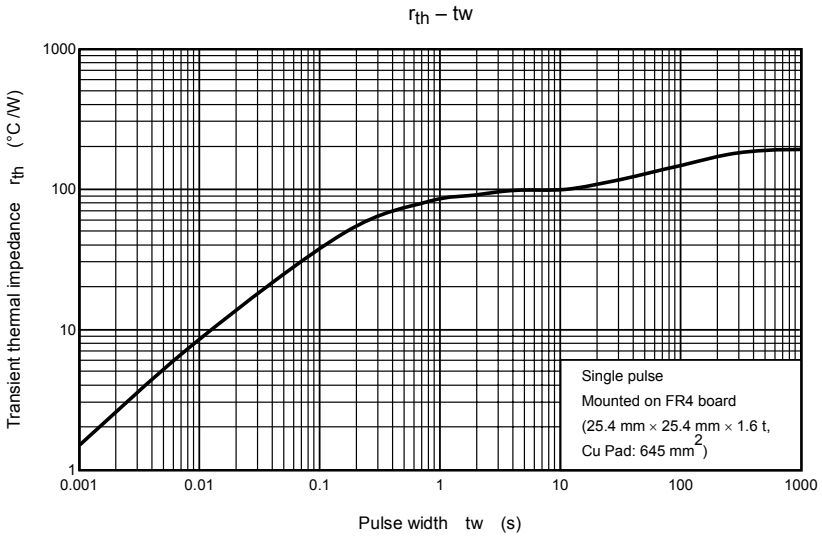

t – ID
Common Source
VDD = 15 V
VGS = 0~2.5 V
RG = 4.7 Ω
Ta = 25°C
toff
tf
ton
tr
Switching time t (ns)
Drain current ID (A)
500
100
50
30
10
0.01
0.03
0.1
0.3
1


PD – Ta
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t,
Cu Pad: 645 mm2)
t = 10 s
DC
Drain power dissipation PD (W)
Ambient temperature Ta (°C)
1.5
1.25
1
0.75
0.5
0.25
0
0
25
50
75
100
125
150


Safe operating area
ID max (pulsed)
ID max (continuous)
1 ms*
10 ms*
10 s*
DC operation
Ta = 25°C
Mounted on FR4 board
(25.4 mm × 25.4 mm
× 1.6 t,
Cu Pad: 645 mm2)
*: Single nonrepetitive
Pulse
Ta = 25°C
Curves must be derated
linearly with increase in
temperature.
VDSS
max
Drain current ID (A)
Drain-source voltage VDS (V)
10
1
0.1
0.01
0.1
1
10
100


rth – tw
Single pulse
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t,
Cu Pad: 645 mm2)
Transient thermal impedance rth (°C/W)
Pulse width tw (s)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000

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