Contents

Introduction

Siemens is THE allround-supplier of Communication ICs. Siemens offers ICs for Digital Exchange Systems, Digital Terminals, Data Transmission Analog and Networks, Mobile Communications and Analog Telephone Sets.

Communication ICs from Siemens – that means innovative and wide ranging problem solving. Siemens Semiconductor Division has integrated system know-how verified by wide field experience and excellent chip technology.

A short look to the product segment ISDN, demonstrates: For the development of ISDN equipment from terminals to PBX and public switching systems Siemens offers the broadest range of ISDN chips available on the merchant market. Siemens is the worldwide market leader for ISDN ICs, due to their high level of functionality resulting in greatly simplified system design.

In addition, the industry standard IOM-2 interface supports flexible system architecture with compatible devices.

Siemens represents technology leadership, offers powerful software and application tools.

Siemens is your partner for Communication ICs:

- Innovative complete system solutions
- Highly optimized devices
- Reliable volume production lines and advanced technology innovation
- Technical support all over the world
- Long term experience and skilled expert teams
- Long term customer relationships
- Excellent quality
- Basic success factors for further innovations
  – Experienced R+D team
  – Device macros
  – Design tools
  – Technology

Due to the fact that Siemens offers a broad range of Communication ICs the overview of the spectrum is presented in this brochure.

If you have further questions or if you need application support, please contact your local Siemens office. Addresses you will find in this brochure.

Call Siemens – your partner for Communication ICs!

1 Quality Assurance

The high quality and reliability of integrated circuits from Siemens are the result of carefully managed design and production which is systematically checked and controlled at each stage.

The procedures are subject to a quality assurance system; full details are given in the brochure “Quality Assurance Integrated Circuits”.

Figure 1 and 2 show the most important stages of the QA system. Quality assurance (QA) departments, independent of production and development, are responsible for the selected measures, acceptance procedures and information feedback loops. Operating QA departments have state-of-the-art test and measuring equipment at their disposal, work according to approved methods of statistical quality control, and are provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

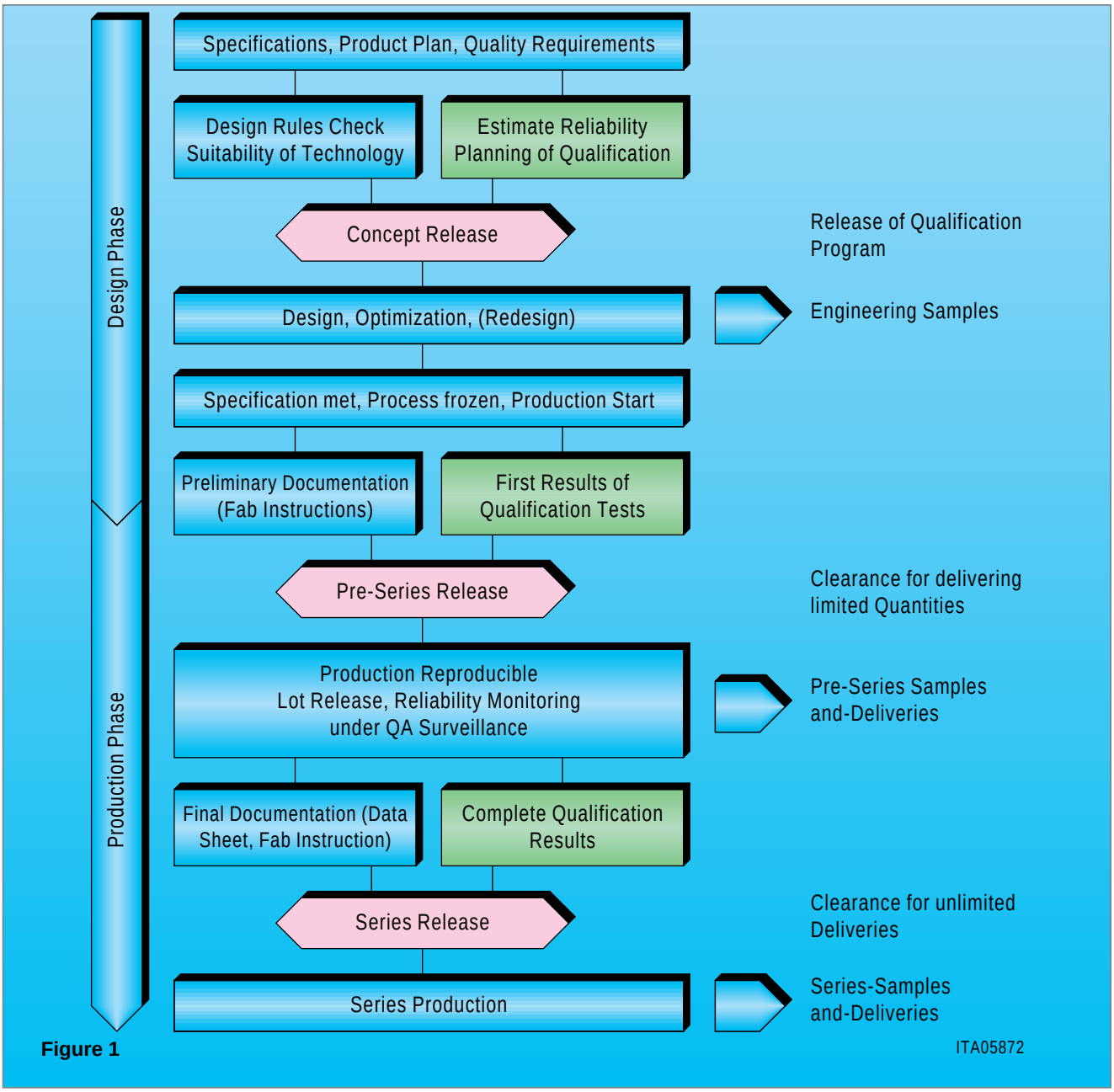


Figure 1

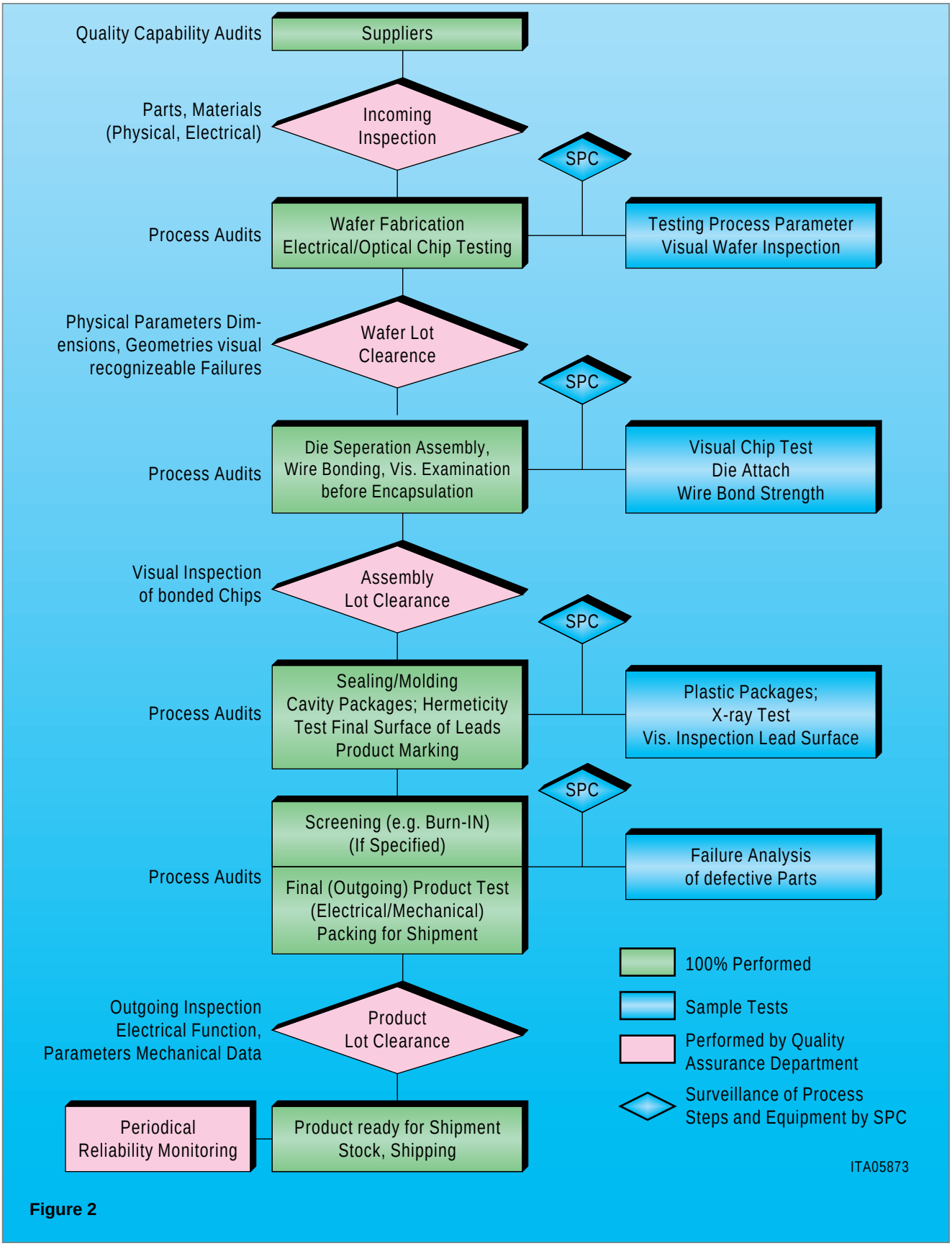

Quality Capability Audits
Suppliers
Parts, Materials (Physical, Electrical)
Incoming Inspection
SPC
Process Audits
Wafer Fabrication Electrical/Optical Chip Testing
Testing Process Parameter Visual Wafer Inspection
Physical Parameters Dim-ensions, Geometries visual recognizeable Failures
Wafer Lot Clearence
SPC
Process Audits
Die Seperation Assembly, Wire Bonding, Vis. Examination before Encapsulation
Visual Chip Test Die Attach Wire Bond Strength
Visual Inspection of bonded Chips
Assembly Lot Clearance
SPC
Process Audits
Sealing/Molding Cavity Packages; Hermeticity Test Final Surface of Leads Product Marking
Plastic Packages; X-ray Test Vis. Inspection Lead Surface
SPC
Screening (e.g. Burn-IN) (If Specified)
Process Audits
Final (Outgoing) Product Test (Electrical/Mechanical) Packing for Shipment
Failure Analysis of defective Parts
100% Performed
Sample Tests
Performed by Quality Assurance Department
Surveillance of Process Steps and Equipment by SPC
Outgoing Inspection Electrical Function, Parameters Mechanical Data
Product Lot Clearance
Periodical Reliability Monitoring
Product ready for Shipment Stock, Shipping
ITA05873

Figure 2

2 Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems as hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure the minimum percent defectives to ensure statistically that the PDA of released lots is less than the AQL agreed. Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

3 Reliabilitiy

3.1 Measures taken during development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuits and layout, e.g. specifying minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers guarantees the immediate identification and elimination of unintentional violations of these design standards.

3.2 In-process control during production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measurements. The tests have been arranged such that the individual process steps can be reproduced continuously.

The decreasing failure rates reflect the never ending effort in this direction; in the course of the years they have been reduced considerably despite an immense increase in IC complexity.

3.3 Reliability monitoring

The general course of IC failure rate versus time is shown by a so-called “bathtub” curve.The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has ended, the “constant” failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment. Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test. The acceleration factor F for the life test can be obtained from Arrhenius's equation

$$F = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature and k is Boltzmann's constant.

Important for factor F is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for individual failure mechanisms.

For all Siemens ICs the reliability data from life tests is converted to an operating temperature of T_A = 55 °C, assuming an average activation energy of 0.5 eV. The acceleration factor for life tests at 125 °C is thus 22, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line this is described in the brochure “Quality Assurance Integrated Circuits”. Such tests are e.g. humidity test at 85 °C and 85 % relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

Quality principles, organization, responsibility and competence for quality assurance procedures and measures during design and production of ICs are summarized in the Semiconductor Group Quality Assurance System. This system also covers ISO 9000/EN 29000 requirements. It is documented in a Quality Assurance Manual. This manual is a guideline mandatory for all Semiconductor Group departments. Suppliers are also tied into the QA system.

CECC certification for the independent test and trials center of Semiconductor Group, which the Villach Plant also profits from.

The Villach Plant was certified to the internationally recognized standard ISO 9002 in 1991.

GSM One-Chip Logic Device
GOLD PMB 2705

GSM/PCN

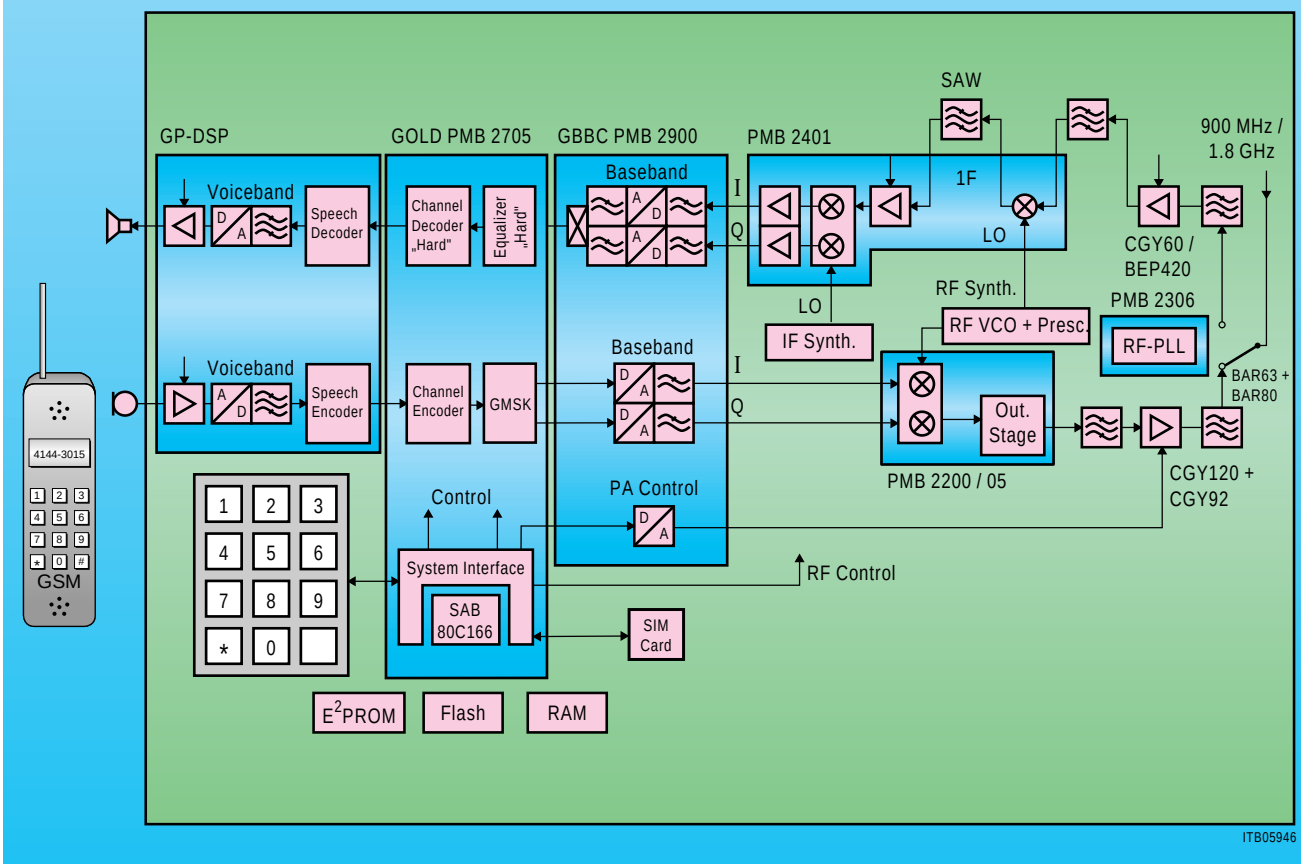
Introduction

GSM and PCN have evolved in the last few years from pan-european into global standards for digital cellular mobile radio systems. The radios are small, easy-to-use and very competitively priced with the older analog systems as the explosive growth in subscribers clearly testifies.

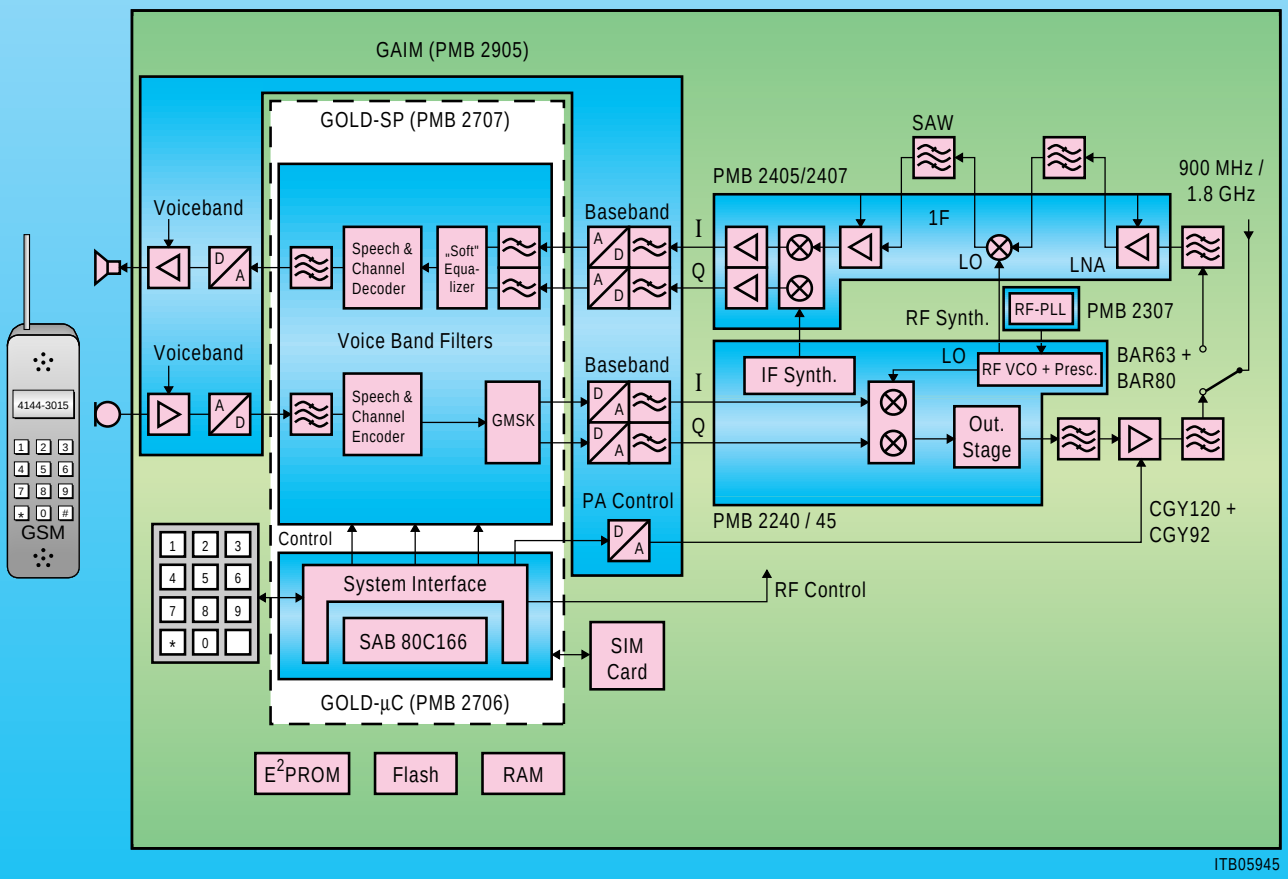
Siemens Semiconductor has played a leading role in this growth as the first supplier of commercially available standard GSM/PCN chip sets. Now after production optimizations of the GOLD chip set, Siemens is offering an evolutionary step forward in intergration level to provide a complate 3-V generation with a 6 chip solution, GOLD plus.

Product Overview

Type	Short Title	Description	Applications	Page
GSM Baseband				
PMB 2705	GOLD	GSM One-Chip Logic Device	GSM, PCN, PCS-1900	14
PMB 2706	GOLD µC	GSM System Controller	GSM, PCN, PCS-1900	16
PMB 2707	GOLD-SP	GSM Signal Processor	GSM, PCN, PCS-1900	18
PMB 2708	GOLD-SX	GSM Co-Processor for Advanced Features	GSM, PCN, PCS-1900	18
PMB 2900	GBBC	GSM Baseband Codec	GSM, PCN, PCS-1900	19
PMB 2905	GAIM	GSM Analog Interface Module	GSM, PCN, PCS-1900	20
GSM RF				
PMB 2200		Direct Vector Modulator	Cellular (GSM, PDC, DAMPS, CDMA), WLAN, QPSK/QAM modulation up to 1 GHz)	37
PMB 2205		Direct Vector Modulator	Cellular (GSM, PCN, PCS, PDC, DAMPS, CDMA), Cordless (PHS), WCPE, WLL, WLAN, QPSK/QAM modulation	41
PMB 2240		GSM Transmitter, 2.7 V	Cellular (GSM, PDC); QPSK/QAM modulation 0.8 GHz to 1.0 GHz	21
PMB 2245		PCN Transmitter, 2.7 V	Cellular (PCN, PCS), Cordless (PHS); QPSK/QAM modulation 1.65 GHz to 1.85 GHz	21
PMB 2247		PCS Transmitter, 2.7 V	Cellular (PCN, PCS), Cordless (PHS); QPSK/QAM modulation 1.8 GHz to 1.95 GHz	21
PMB 2306		PLL	All analog and digital systems as RF- and IF-synthesizer up to 220 MHz	47
PMB 2401		Receiver/Demodulator Circuit	Cellular (GSM, PDC, DAMPS, CDMA), WLAN, QPSK/QAM modulation up to 0.9 GHz	43
PMB 2405		GSM Receiver, 2.7 V	Cellular (GSM, PDC, DAMPS), WLAN, QPSK/QAM modulation up to 2.5 GHz	23
PMB 2407		PCN/PCS Receiver, 2.7 V	Cellular (PCN, PCS) WLAN, QPSK/QAM modulation up to 2.5 GHz	23



Block Diagram of a GSM Handy Phone (1st Gen.)



Block Diagram of a GSM/PCN Fullrate & Halferate Mobile

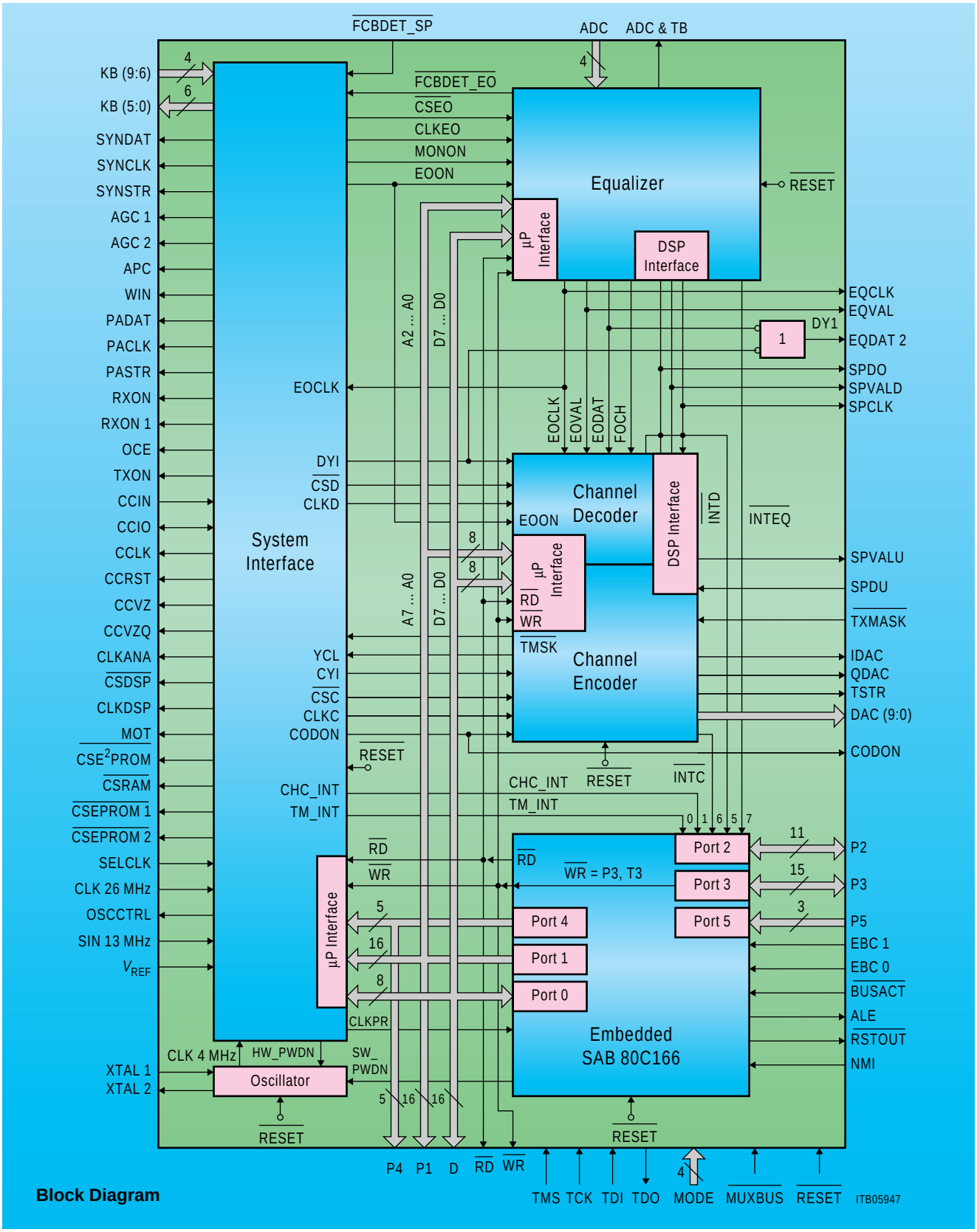
General Description

The GSM One-Chip Logic Device (GOLD) PMB 2705 performs the tasks of bit error protection, ciphering, radio channel equalization, bit error detection and correction, synchronization etc., and above all the microcontroller core controls all the RF- and baseband functions of a GSM-mobile terminal.

Type	Package
PMB 2705-F	P-TQFP-176-1 (SMD)

Features

- Four function modules integrated on one chip
  – 16-bit microcontroller
  – Channel codec
  – Equalizer
  – System interface
- One special external-channel-codec mode selectable by software
- Four operational modes selectable via pins:
  – Normal mode
  – External-controller mode
  – External-channel-codec mode (different from special mode!)
  – External-equalizer mode
- Four single modes selectable via pins
  – Controller test mode
  – System interface test mode
  – Channel-codec test mode
  – Equalizer test mode
- Two sizes of address spaces covered by chip-select signals selectable via pin:
  – 256 Kbyte
  – 2 Mbyte
- Programmable power saving modes
- JTAG-boundary scan (acc. to IEEE Std. 11491)
- Single supply voltage (+ 5 V)
- Low power consumption
- Temperature range – 25 °C to 85 °C



Block Diagram

General Description

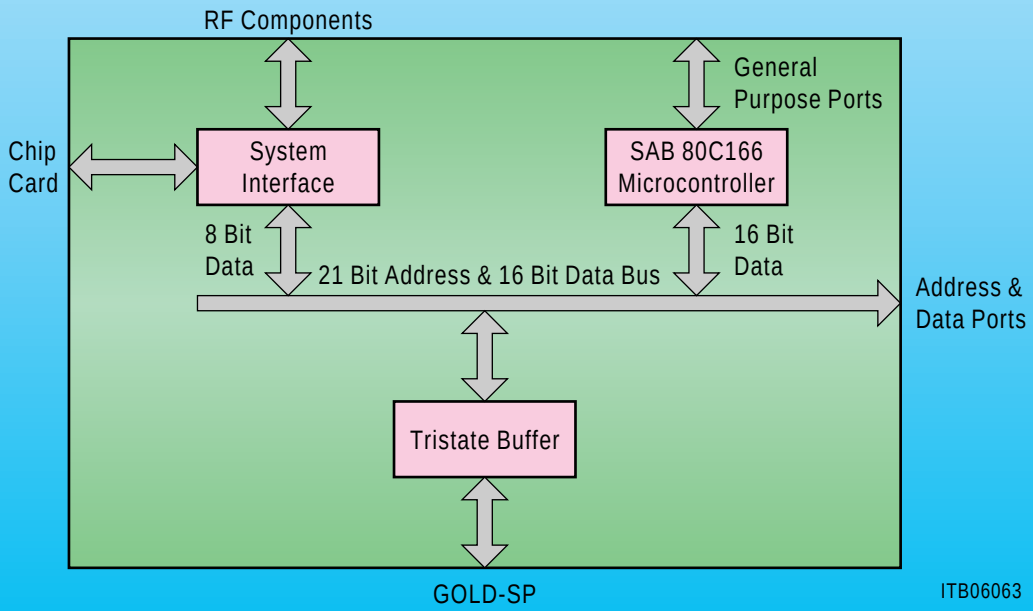
The GOLD System Controller (GOLD-µC) is part of a chip set, which covers all functions of a mobile radio provided for the **G**lobal **S**ystem for **M**obile communications, GSM. A mobile terminal which contains this chip set will meet all performance requirements set down in the GSM recommendations for speech and data services.

GOLD-µC contains a 16-bit microcontroller type 80C166 with an address space being extended from 256 Kbyte to 2 Mbyte and a system interface block which comprises a series of GSM-specific interfaces and control functions.

Type	Package
PMB 2706-F	P-TQFP-144-2 (SMD)

Features

- Integrated 16-bit microcontroller (SAB 80C166) with 2-Mbyte linear address space
  Complete development tooling available
- System interface with synthesizer, AGC, AFC and PA control, chip card interfacing, timing signal generation, clock generation
- Bidirectional tristate buffer
  GOLD-SP can access to controller memory
- Package P-TQFP-144, 20 × 20 mm, 0.50 mm pitch
- 3-V supply voltage (± 10 %)



Block Diagram

General Description

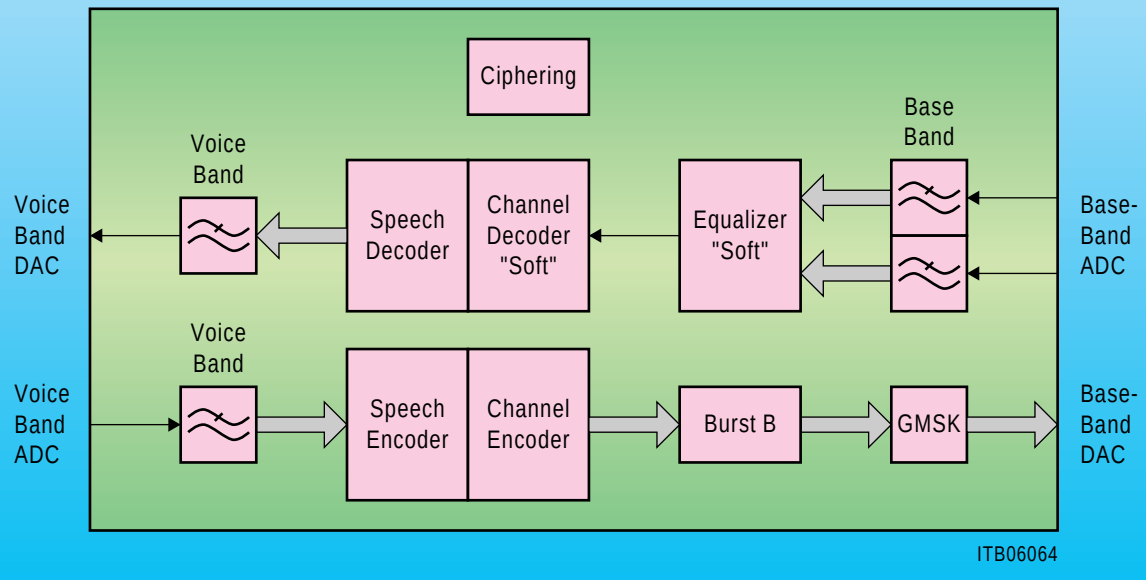
The GOLD Signal Processor (GOLD-SP) is part of a chip set, which covers all functions of a mobile radio provided for the **G**lobal **S**ystem for **M**obile communications, GSM. A mobile terminal which contains this chip set will meet all performance requirements set down in the GSM recommendations speech and data services.

GOLD-SP contains a fullrate speech codec, a channel codec with soft-decision decoding and a complex Viterbi equalizer, all as DSP firmware. Moreover all digital filtering needed for baseband and voiceband processing, and also GMSK modulation is performed on this chip.

Type	Package
PMB 2707-F	P-TQFP-100-1 (SMD)

Features

- Two parallel DSP cores type SPC each with high performance (26 MIPS @ 2.7 V), low current consumption (< 1 mA/MIPS), all memory needed for fullrate operation on chip, shared access to complete controller memory
- GSM functions realized as DSP firmware
  - Complex soft-output equalizer
  - Frequency correction burst handling
  - Full duplex handsfree
  - Channel coding
  - Soft-decision decoding (bit-by-bit)
  - Speech coding and decoding (RPE-LTP)
- Digital baseband filter
  Automatic amplitude calculation
  Automatic amplitude offset measurement
- Ciphering with A51/A52
- Digital voiceband filters (receive, transmit)
- GMSK modulator
- PLL-based system clock generation
- Package: P-TQFP-100, 14 × 14 mm, 0.50 mm pitch
- 3-V supply voltage (± 10 %)



Block Diagram

General Description

The GOLD-SX is part of a complete chip set which covers all functions of a mobile radio for the Global System for Mobile communications, GSM. A mobile terminal which contains this chip set can meet all performance requirements set down in the Technical Specifications for GSM, PCN and PCS-1900.

GOLD-SX is used for advanced features. The function of the GOLD-SX is dependent on its firmware.

The first version of the GOLD-SX performs Half-Rate speech encoding including Voice Activity Detection (VAD) and Discontinuous Transmission (DTX), as well as Half-Rate speech decoding including Discontinuous Reception (DRX, Comfort Noise).

A planned version will perform: Enhanced Full-Rate speech coding including all the DTX functions as in Half-Rate speech coding.

Type	Package
PMB 2708-F	P-TQFP-64-1 (SMD)

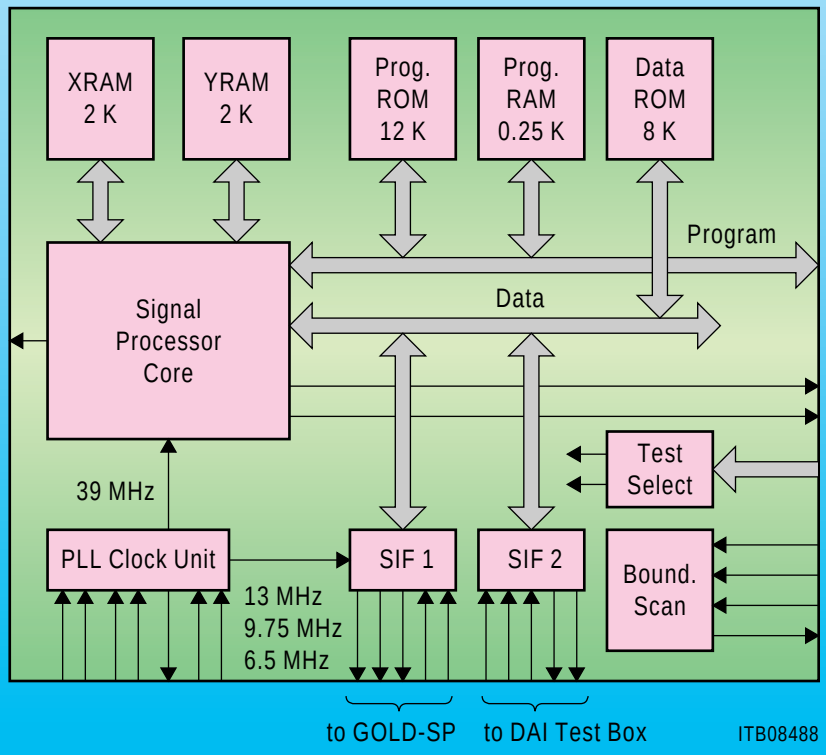
Features

Firmware:
The GOLD-SX is available in versions with different mask programmed ROM code:

- Half-Rate Codec
  - GSM Half-Rate Speech Codec (GSM 6.02, 6.06, 6.07, 6.20)
  - Voice activity detection, VAD (GSM 6.42)
  - Discontinuous transmission, DTX (GSM 6.41)
  - Comfort noise generation, DRX (GSM 6.22)
  - Serial data exchange with Half-Rate Channel Codec and voiceband unit on GOLD-SP
  - Serial data exchange with system simulator interfacing box
- Enhanced Full-Rate Codec
  - GSM Enhanced Full-Rate Codec
  - Voice activity detection, VAD
  - Discontinuous transmission, DTX
  - Comfort noise generation, DRX
  - Serial data exchange with Enhanced Full-Rate Channel Codec and voiceband unit on GOLD-SP
  - Serial data exchange with system simulator interfacing box

Hardware:

- DSP core of type SPCE (Siemens Signal Processor Core Enhanced) offering high performance (39 MIPS @ 39 MHz, 2.7 V) and current consumption (approx. 0.6 mA/MIPS)
- 12 K Program ROM and 0.25 K RAM, 8 K Data ROM on-chip
- PLL-based clock generation (13-MHz input)
- Package: P-TQFP-64, 10 × 10 mm², 0.50 mm pitch
- 3-V supply voltage (± 10 %)



Block Diagram

Preliminary Data

Overview

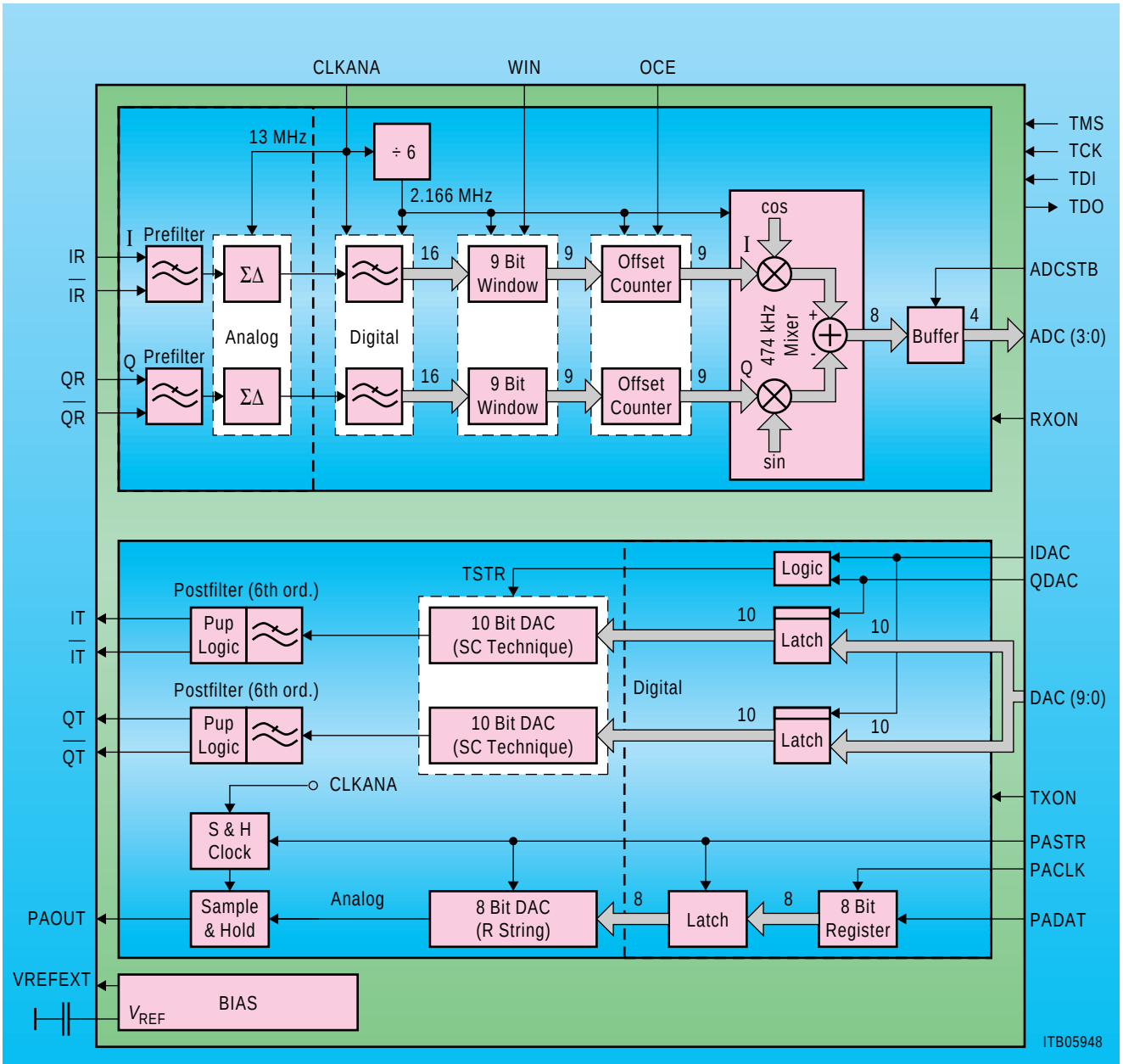
The GSM Baseband Codec (GBBC) performs the analog-to-digital and the digital-to-analog conversion of the baseband signals and additionally the digital-to-analog conversion of the control signal provided for the RF power amplifier.

GBBC is part of a chip set, which covers the functions of a mobile radio provided for the Global System for Mobile communications, GSM. A mobile terminal which contains this chip set will meet all performance requirements set down in the GSM recommendations.

Type	Package
PMB 2900-H	P-MQFP-64-1 (SMD)

General Features

- JTAG-boundary scan (acc. to IEEE Std. 1149.1)
- Single supply voltage (+ 5 V)
- Ambient temperature range – 25 °C to 85 °C



Block Diagram

General Description

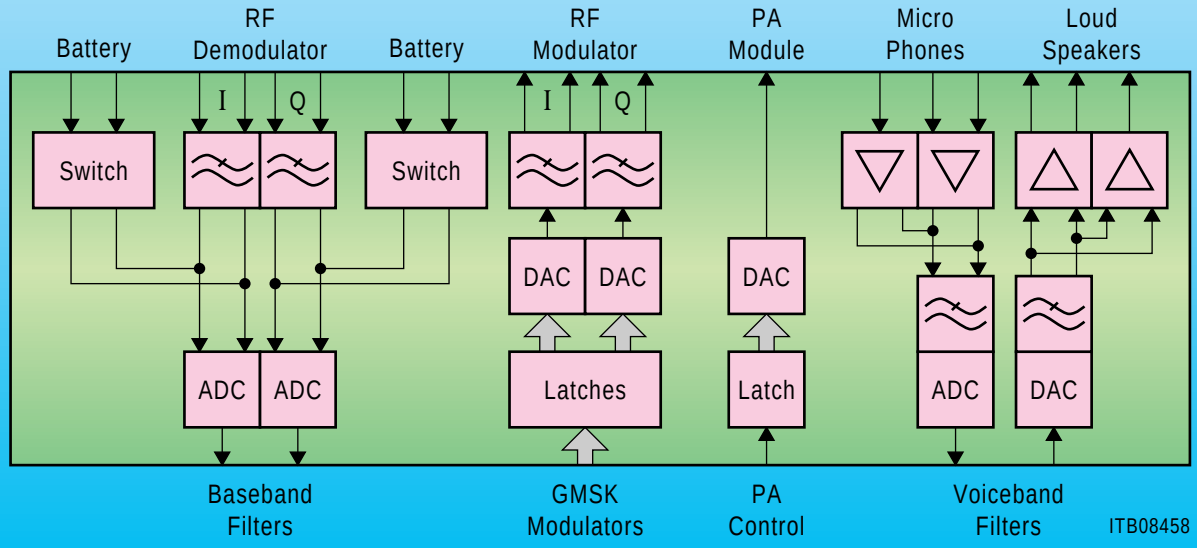
The **G**SM **A**nalog **I**nterfacing **M**odule (GAIM) is part of a chip set, which covers all functions of a mobile radio provided for the **G**lobal **S**ystem for **M**obile communications, GSM. A mobile terminal which contains this chip set will meet all performance requirements set down in the GSM recommendations for speech and data services.

GAIM is provided for analog-to-digital and digital-to-analog conversion of baseband and voiceband signals as well. Moreover digital-to-analog conversion of an RF power control signal can be performed by this circuit.

Type	Package
PMB 2905-F	P-TQFP-64-1 (SMD)

Features

- Baseband receive A-to-D converter
  analog antialiasing filter (2nd order Bessel)
  2nd order sigma-delta modulators for
  baseband receive and battery measurements
- Baseband transmit D-to-A converter
  10 bit switched-capacitor-type DAC
  analog postfilter (6 th order Bessel)
- Power ramping control D-to-A converter
  8-bit resistor-string-type DAC
- Voiceband receive D-to-A converter
  low pass filter following
  digital Σ-Δ-modulator on GOLD-SP
  two programmable earpiece gain stages
- Voiceband transmit A-to-D converter
  2nd order sigma-delta modulator analog
  antialiasing filter two programmable
  microphone gain stages
- Package
  P-TQFP-64-1, 10 × 10 mm, 0.5 pitch
- 3-V supply voltage (± 10 %)



Block Diagram

General Description

The PMB 2240, 2245, 2247 family are single-chip transmitters which include a prescaler for the RF-oscillator signal and a fixed PLL for the IF-oscillator signal. The transmitter family is designed for use in combination with the single-chip receiver family PMB 2405, 2407 and the PLL PMB 2307 for mobile telephones according to the GSM, PCN and PCS standards and other vector modulated digital systems. It is fabricated using Siemens B6HF silicon process:

GSM Chipset	PCN Chipset	PCS Chipset	
PMB 2240	PMB 2245	PMB 2247	TX
PMB 2405	PMB 2407	PMB 2407	RX
PMB 2307	PMB 2307	PMB 2307	PLL

The PMB 2240/45/47 transmitters include the active structures for the main oscillator circuit. Alternatively the oscillator signal can be supplied from an external source. The oscillator signal is buffered for off-chip use.

There is a prescaler by 64/65 for the RF-oscillator signal on chip, which can be used to implement the PMB 2307 PLL circuit.

The on-chip FIX-PLL consists of the system clock divider, the IF-oscillator signal divider, the phase detector and the charge pump. The IF-oscillator signal divider is driven by the oscillator on the PMB 2405/07 or by an external discrete VCO. The IF-oscillator signal divider ratio of PMB 2240 and PMB 2245 is fixed. It can be selected either divided by 1 or by 3 using PMB 2247 and PMB 2407 to drive the FIX-PLL with two IF frequencies (450 MHz or 150 MHz) to avoid spurious problems for PCS application.

The two oscillator signals (IF and RF) are combined in the transmit mixer, and the image sideband and other mixing products are to be suppressed by an external interstage filter. The filtered signal reenters the chip at the modulator inputs. The modulator generates two orthogonal carriers which are mixed with the I- and Q modulation signals by two multipliers. The phase between the two carriers can be fine-adjusted to 90° (orthogonality) by two external resistors for maximum SSB suppression. The outputs of the multipliers are added and amplified by a linear output stage.

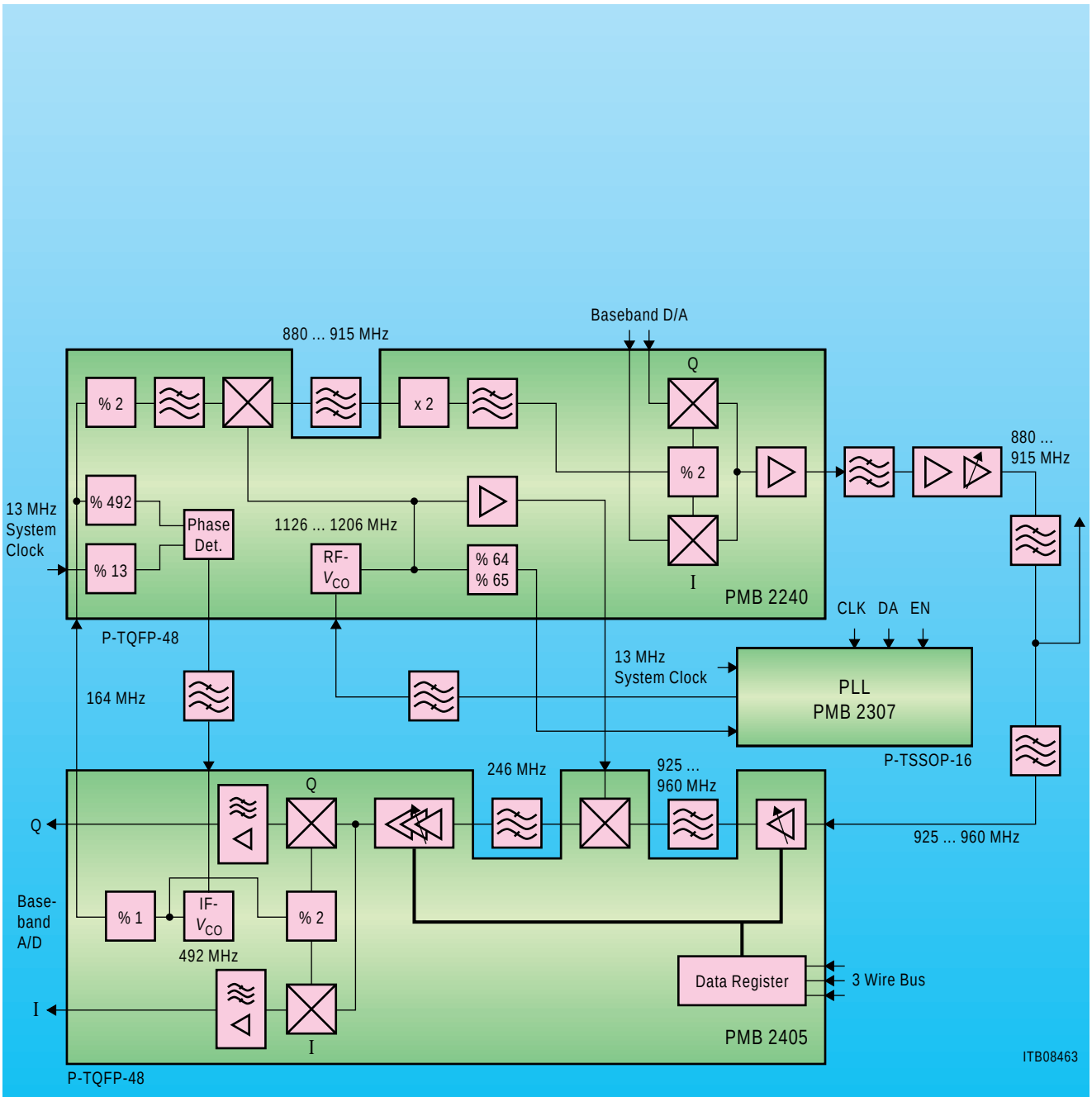
Type	Package
PMB 2240-F	P-TQFP-48-1 (SMD)
PMB 2245-F	P-TQFP-48-1 (SMD)
PMB 2247-F	P-TQFP-48-1 (SMD)

Application

- Vector modulated cellular and cordless systems:
- PMB 2240: GSM, PDC, DAMPS
- PMB 2245: PCN, PCS, PHS
- PMB 2247: PCN, PCS, etc.
- Various modulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK etc.
- Analog systems with FM- and AM modulation
- Space and power saving optimizations of existing discrete transmitter circuits

Features

- Transmitter with I/Q modulator
- Direct I/Q modulation
- Generation of orthogonal carriers with possibility of phase adjust with external resistors
- 30-dB carrier rejection, 40-dB SSB rejection
- 48-dB rejection of third order products with 500-mVpp I/Q-drive level
- High output power with appropriate power matching network at 500-mVpp I/Q-drive level
  PMB 2240: – 3 dBm, PMB 2245: – 6 dBm
  PMB 2247: – 8 dBm
- Integrated active part of RF oscillator
- Possibility to use external RF-oscillator signal
- The RF-oscillator signal is buffered for off-chip use, especially for receiver PMB 2405/07
- Prescaler for the RF-oscillator signal
- Possibility to use the IF oscillator integrated on the PMB 2405/07
- Possibility to use external IF-oscillator signal
- Fixed IF frequency PLL (FIX-PLL) for IF-VCO (PMB 2240, 2245), switchable IF PLL working at 450-MHz or 150-MHz IF frequency (PMB 2247)
- Supply voltage range 2.7 to 5.5 V
- P-TQFP-48 package
- Temperature range – 30 °C to 85 °C



GSM Application PMB 2240 / PMB 2405 / PMB 2307

General Description

The PMB 2405, 2407 family are single-chip double-conversion heterodyne receivers with LO-phase shifting circuitry for the I/Q-phase demodulation on chip. It also includes a switchable low noise amplifier, the second local oscillator with a VCO output buffer, a programmable gain controlled IF amplifier, two differential operational amplifiers for base band signal filtering and a power-down circuitry.

The receiver family is designed for use in combination with the single chip transmitter family PMB 2240, 2245, 2247 and the PLL PMB 2307 for mobile telephones according to the GSM, PCN and PCS standards and other vector modulated digital systems. It is fabricated using Siemens B6HF silicon process.

GSM Chipset	PCN Chipset	PCS Chipset	
PMB 2405	PMB 2407	PMB 2407	RX
PMB 2240	PMB 2245	PMB 2247	TX
PMB 2307	PMB 2307	PMB 2307	PLL

The input signal is amplified by the internal LNA and filtered by an external filter. The filtered signal and the first local oscillator signal LO1 are mixed down to an intermediate frequency (IF). The amplification of the IF signal is performed by a digitally programmable gain-controlled amplifier.

The second local oscillator signal LO2 is generated either by an on-chip oscillator or by an external VCO. The internal LO2 signal is fed to a divider (PMB 2405-by 1; 2407-by 1 or 3) and then to a buffered output and also to a divider, which generates orthogonal signals at half the VCO frequency. The filtered IF signal re-enters the chip at the IF input, where it is amplified and converted to the final output frequency with each of the orthogonal signals. The resulting in-phase and in-quadrature signals pass through differential output drivers.

Two differential operational amplifiers can be used as active baseband filters. At both outputs the differential offset is sensed via the sample and hold circuitry. A feedback loop corrects the remaining offset error below the tolerable input value of the GAIM PMB 2905 or any other baseband A/D converter.

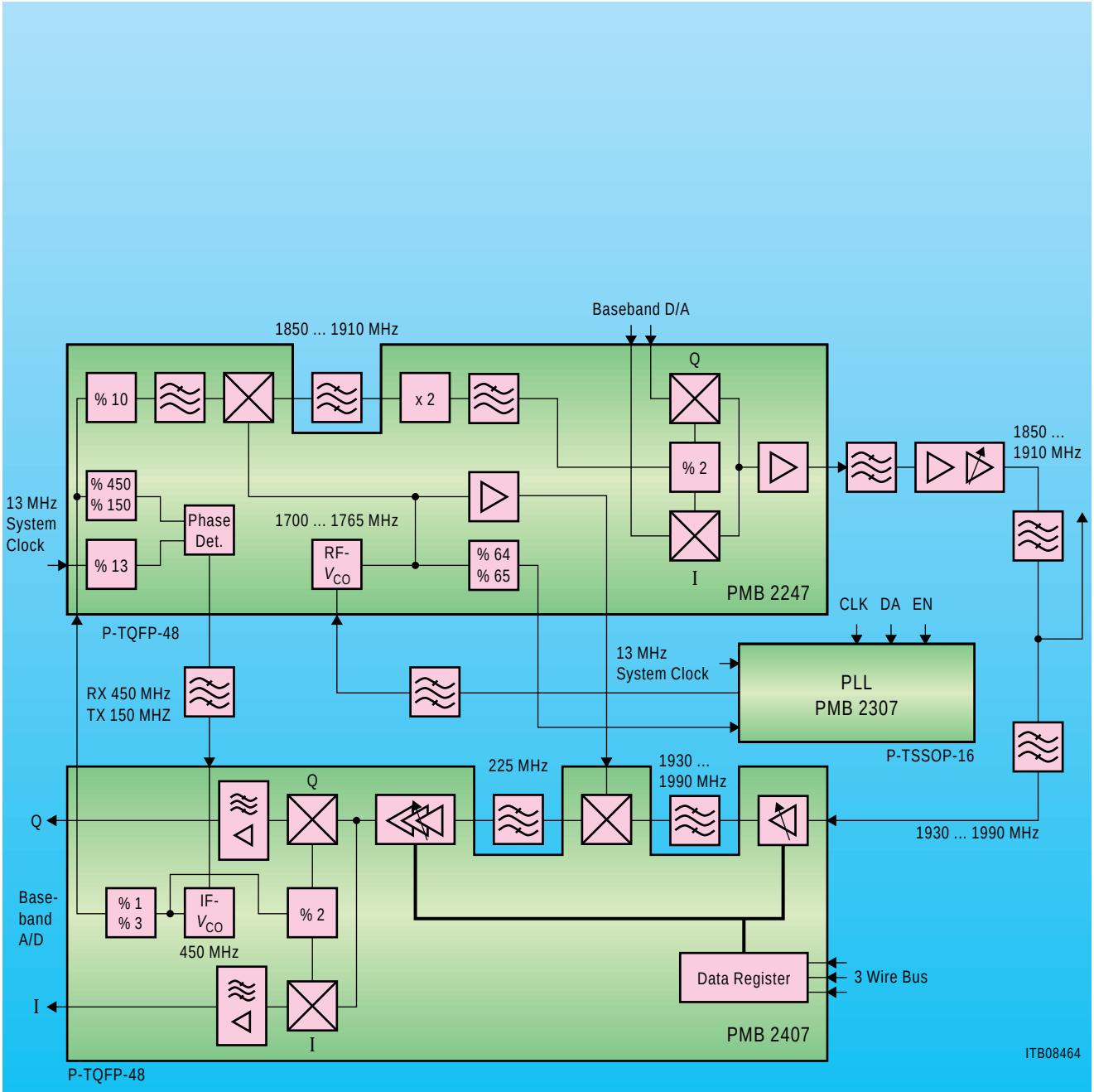
Type	Package
PMB 2405-F	P-TQFP-48-1 (SMD)
PMB 2407-F	P-TQFP-48-1 (SMD)

Applications

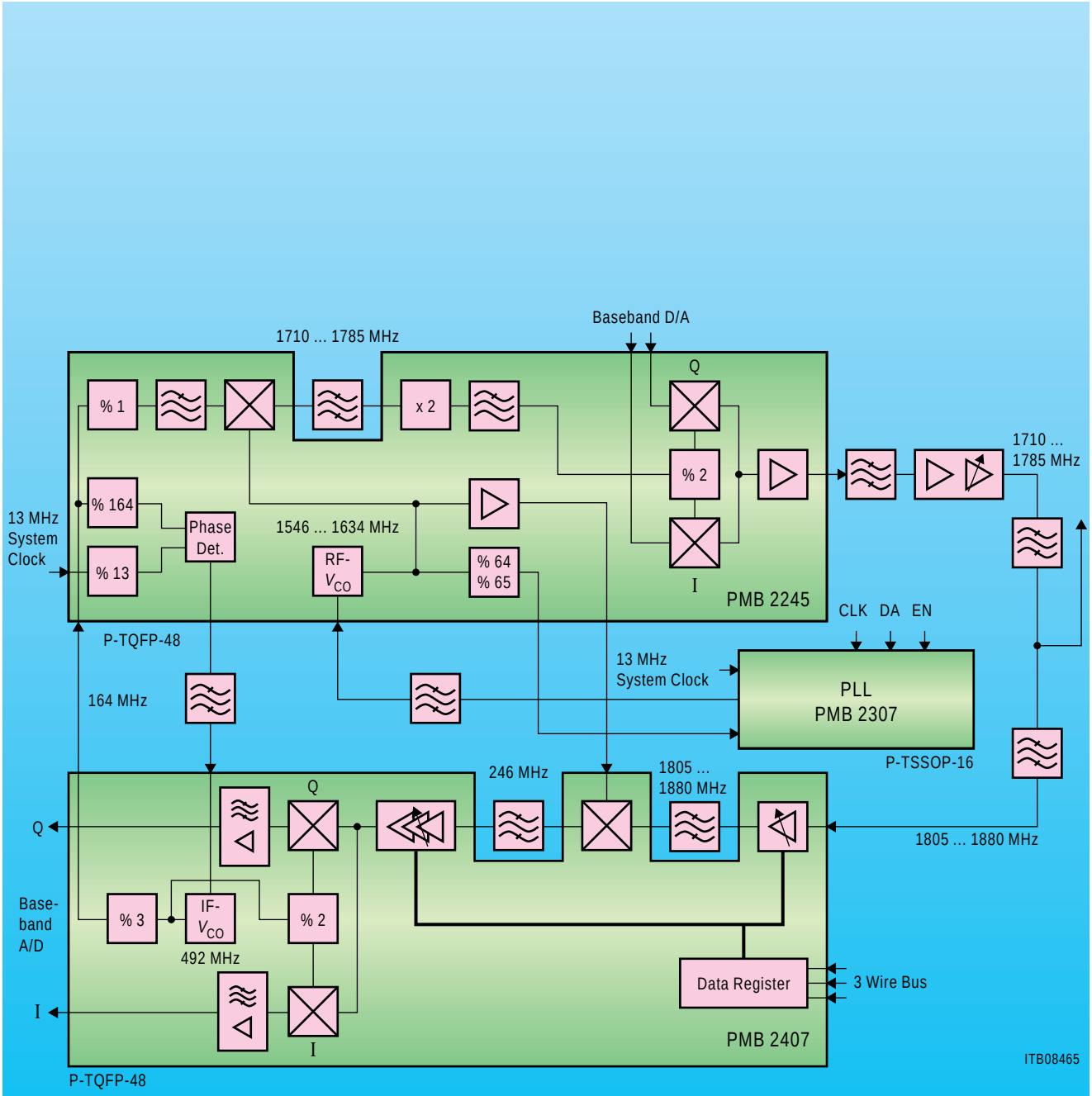
- Vector modulated cellular and cordless systems:
  PMB 2405: GSM, PDC, DAMPS,
  PMB 2407: PCN, PCS (DCS1900), WLAN etc.
- Various demodulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK
- Space and power saving optimizations of existing discrete demodulator circuits

Features

- Heterodyne receiver with demodulator
- On-chip, low noise amplifier (LNA),
- Demodulation and generation of I/Q components
- Low mixer noise 9 dB (SSB)
- High input intercept point + 2 dB
- Integrated phase shifter
- IF amplifier with 80 dB programmable gain control (PGC) in steps of 2 dB
- On-chip second LO oscillator with external tuning circuit or possibility to use it as amplifier
- Two differential operational amplifiers for use as base band filter or amplifier
- Low power consumption due to highly flexible power-down capability
- Wide input frequency range up to 2.5 GHz
- Wide IF range from 40 MHz to 300 MHz
- Supply voltage range 2.7 to 4.5 V
- P-TQFP-48 package
- Temperature range – 30 °C to 85 °C



PCS Application PMB 2247 / PMB 2407 / PMB 2307



PCN Application PMB 2245 / PMB 2407 / PMB 2307

DECT (Digital European Cordless Telecommunication)

Introduction

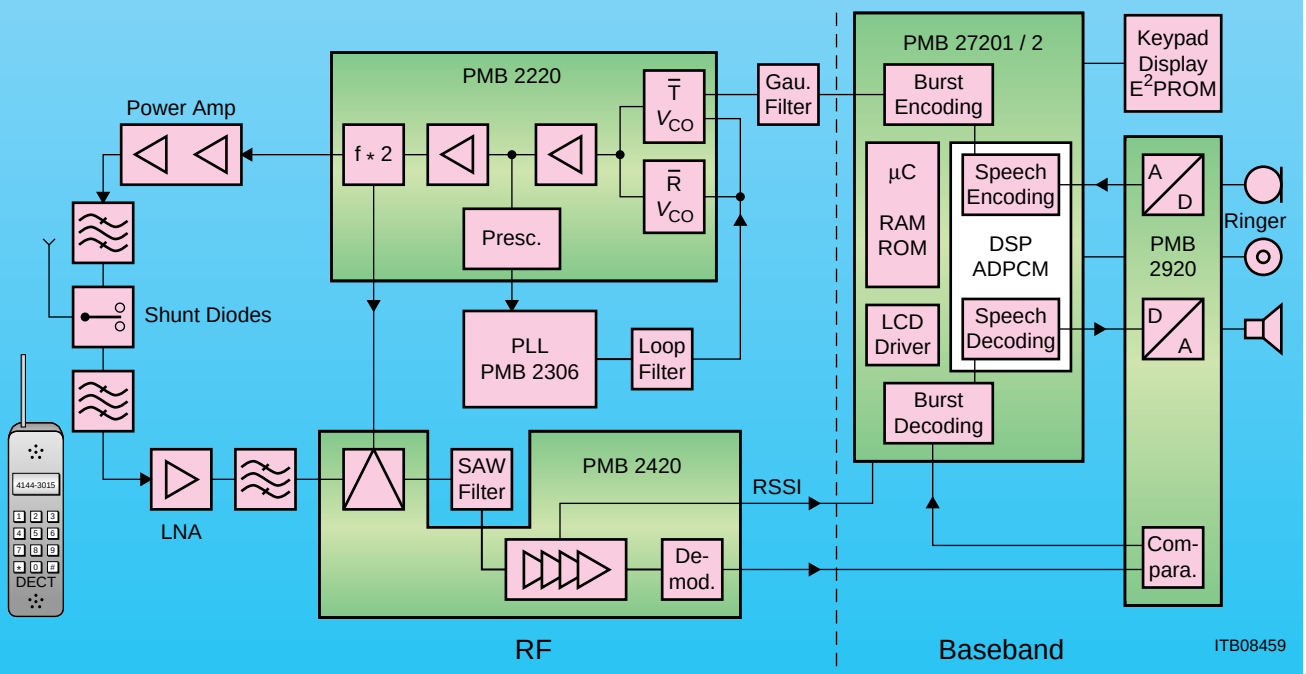
DECT is the coming **D**igital **E**uropean **C**ordless **T**elecommunication standard which has been defined for a wide range of different applications. It meets the requirements of cordless equipment users of home applications, of the office environment (e.g. cordless PBX) and of public use as wireless local loop.

DECT is the result of teamwork between industry, administration and service providers from all over Europe. It will be introduced in all EU countries and has high potential to be accepted as a standard also outside Europe.

As the first supplier worldwide, Siemens Semiconductor offers a complete highly integrated DECT system solution which covers baseband processing as well as the RF front end. The Siemens' solution for the DECT mobile station cuts down component count of first generation design from more than 500 parts to less than 200 components and saves cost, board space and power. Besides solutions for DECT home terminals and handheld systems, solutions are provided for cordless key systems, cordless PBX and wireless local loop applications, too.

Product Overview

Type	Description	Applications	Page
DECT Baseband			
PMB 27201/2	DECT Baseband Controller for Handhelds		28
PMB 27251/2	DECT Baseband Controller for Basestation		29
PMB 2727	DECT Burst Mode Controller for PBX		30
PMB 2728	DECT Burst Mode Controller and ADPCM Codec for Keys Systems		31
PMB 2920	DECT Baseband Analog IC		32
DECT RF			
PMB 2220	DECT Transmitter, 3 V	Cordless (DECT); FSK modulation	33
PMB 2306	PLL	All analog and digital systems as RF- and IF synthesizer up to 220 MHz	47
PMB 2420	DECT Receiver, 3 V	Cordless (DECT), FSK modulation	34



DECT System Solution

General Description

The DECT-Digital Circuit for Handhelds is one of the devices of the Siemens chip set for the digital cordless telephone specified by the DECT standard.

The device designed for cordless handhelds is a highly integrated circuit and realizes most of the system functions needed in such an equipment.

The circuit contains a digital signal processor, an 8-bit 80C51-compatible microcontroller and the burst mode controller. Furthermore the circuit handles the interfacing of the different components of the DECT chipset and feature LCD controller.

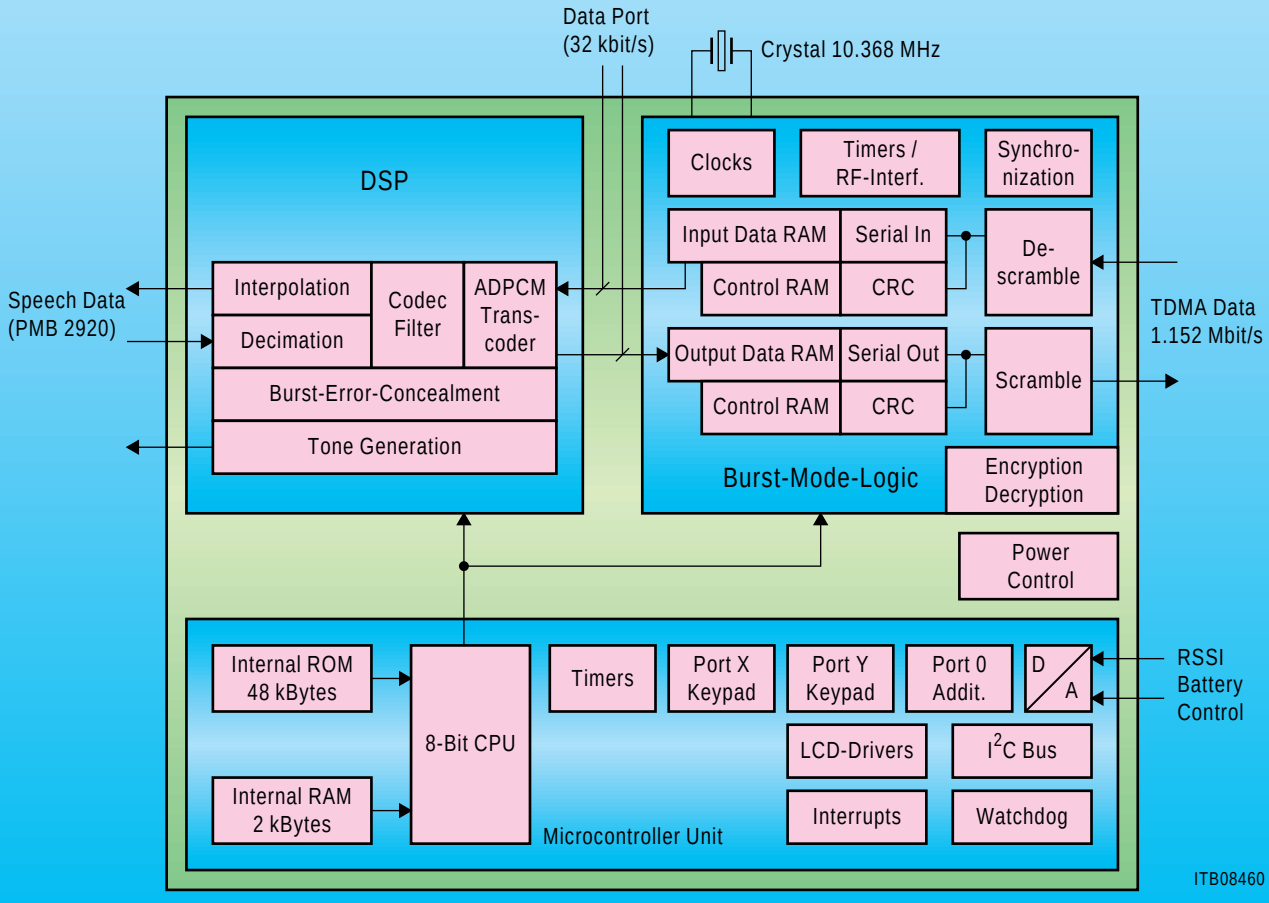
The device is fabricated using Siemens advanced CMOS technology and will be available in a 128 pin package.

Further baseband controllers are PMB 27221 (romless version with 4 K RAM).

Type	Package
PMB 27201/2	P-TQFP-128-1 (SMD)

Features

- 8-bit µC with integrated ROM/RAM
- Integrated LCD controller
- 32-kbit/s ADPCM-transcoder
- Digital filtering and gain stages
- Burst mode controller
- Power-down mode programmable
- Low voltage detection
- Power supply 3.0 … 5.1 V
- Low power consumption
- Advanced low power CMOS technology
- Encryption
- PMB 27201: 64 K ROM, 4 K RAM
- PMB 27202: 48 K ROM, 2 K RAM



Block Diagram PMB 27202

General Description

The DECT-Digital Circuit for Basestations is one of the devices of the Siemens chip set for the digital cordless telephone specified by the DECT standard.

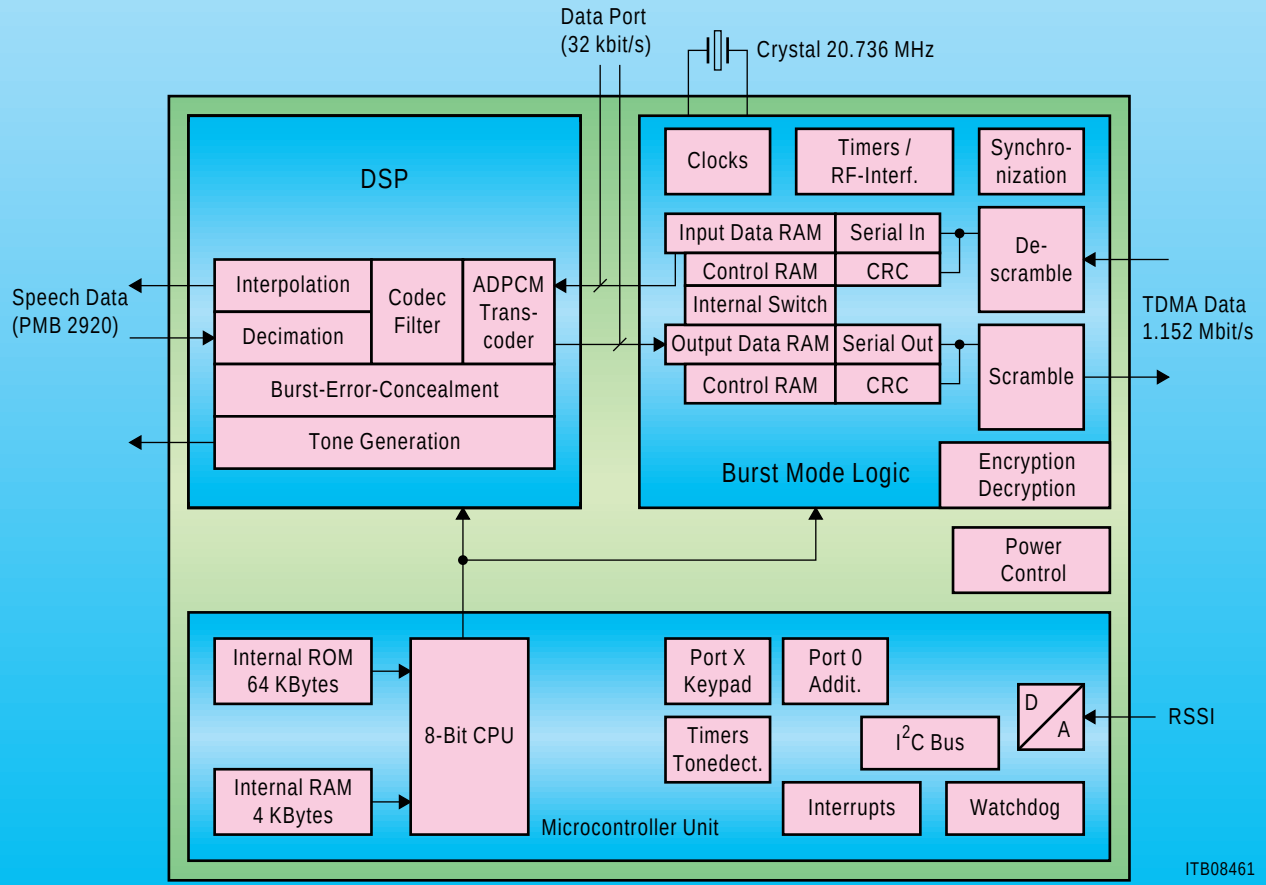
The device designed for single cordless fixed stations is a highly integrated circuit and realizes most of the system functions needed in such an equipment. The circuit contains a digital signal processor, an 8-bit 80C51-compatible microcontroller and the burst mode controller. Furthermore the circuit handles the interfacing of the different components of the DECT chipset.

The device is fabricated using Siemens advanced CMOS technology and will be available in a 128 pin package.

Type	Package
PMB 27251/2	P-TQFP-128-1 (SMD)

Features

- 8-bit µC with integrated ROM/RAM
- 32 bit/s ADPCM-transcoder
- Digital filtering and gain stages
- Echocancellation
- Burst mode controller
- Internal calls possible
- Power supply voltage: 5 V ± 5 %
- Low power consumption
- Advanced low power CMOS technology
- Encryption
- PMB 27251: 6 K RAM
- PMB 27252: 64 K ROM, 4 K RAM



Block Diagram PMB 27252

General Description

The DECT Multichannel Burst Mode Controller is one of the devices of the Siemens chip set designed cordless applications specified by the DECT standard.

The device can handle up to twelve DECT channels. It supports most of the Medium Access Control (MAC) layer and Physical layer (PHL) functions specified in the DECT standard. An interface to a standard 8-bit microcontroller (Motorola and Intel compatible) is implemented.

Furthermore 3 IOM-2 interfaces are integrated e.g. for direct connection of U_{P0} transceivers (ISAC-P TE). The on-chip RF interface allows the control of the DECT-RF circuitry with a minimum of discrete components.

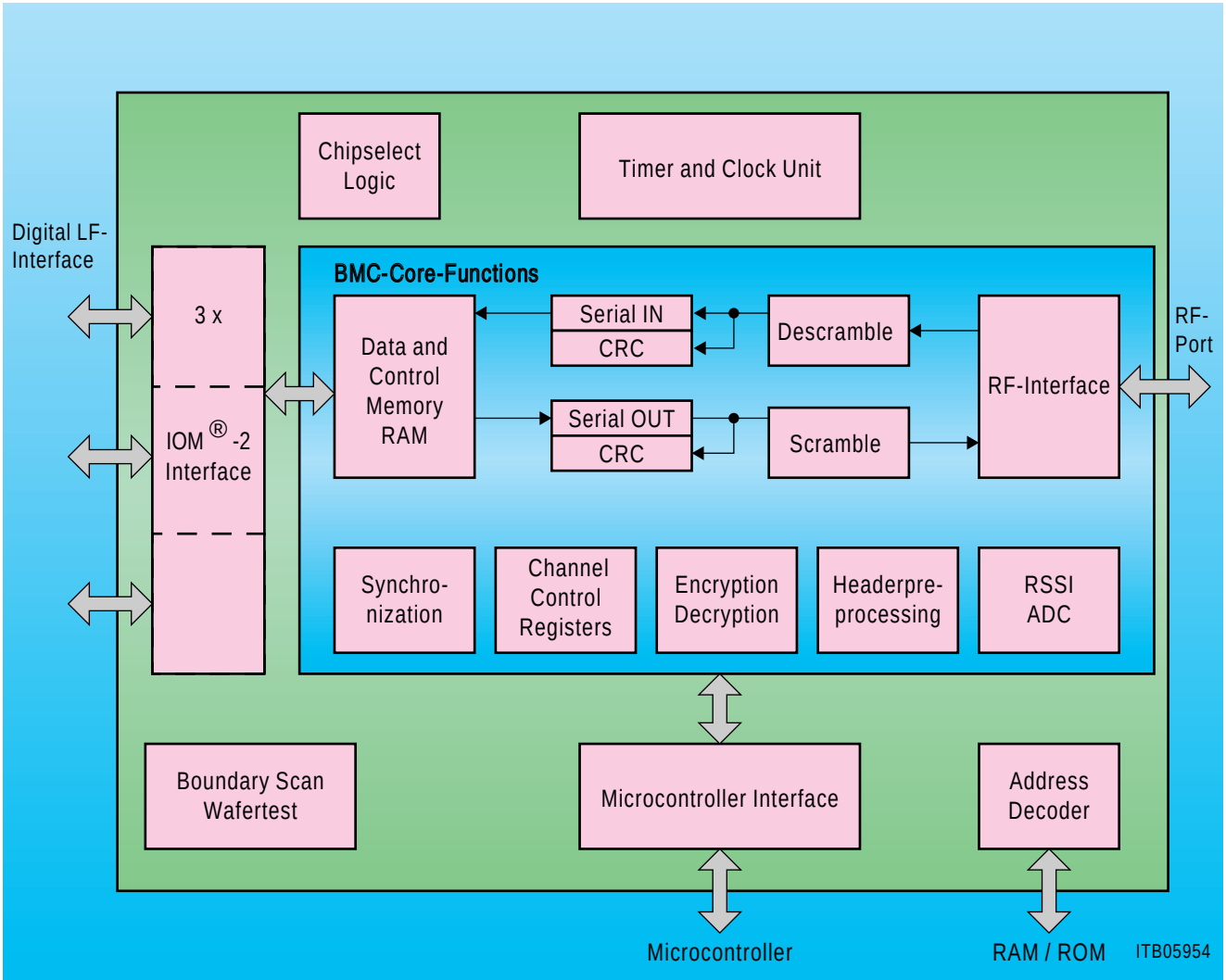
The circuit can be used in DECT basestations (Radio Fixed Parts RFPs). The device supports unprotected data transmission.

The device is fabricated using Siemens advanced CMOS technology and will be available in a 100 pin package.

Type	Package
PMB 2727-H	P-MQFP-100-2 (SMD)

Features

- Power-down mode programmable
- Power supply voltage: 5 V ± 5 %
- Low power consumption: 100 mW (5 V)
- Advanced low power CMOS technology



Block Diagram

General Description

The DECT PBX circuit is one of the devices of the Siemens chip set designed for cordless basestations specified by the DECT standard.

The circuit consists of two main functional blocks, these are the Burst Mode Controller (BMC) and the Digital Signal Processor (DSP).

The BMC can handle up to six DECT channels. It supports the timecritical functions specified in the DECT standard. Either 6 internal connections between handheld or 2 internal and 2 external connections can be handled. An interface to a standard 8-bit microcontroller (Motorola/Mitsubishi and Intel compatible) is implemented. The on-chip RF interface allows the control of the DECT-RF circuitry with a minimum of discrete components.

The one-chip DSP can handle PCM/ADPCM
– transcording and echosupression due to the DECT
– standard for two channels.

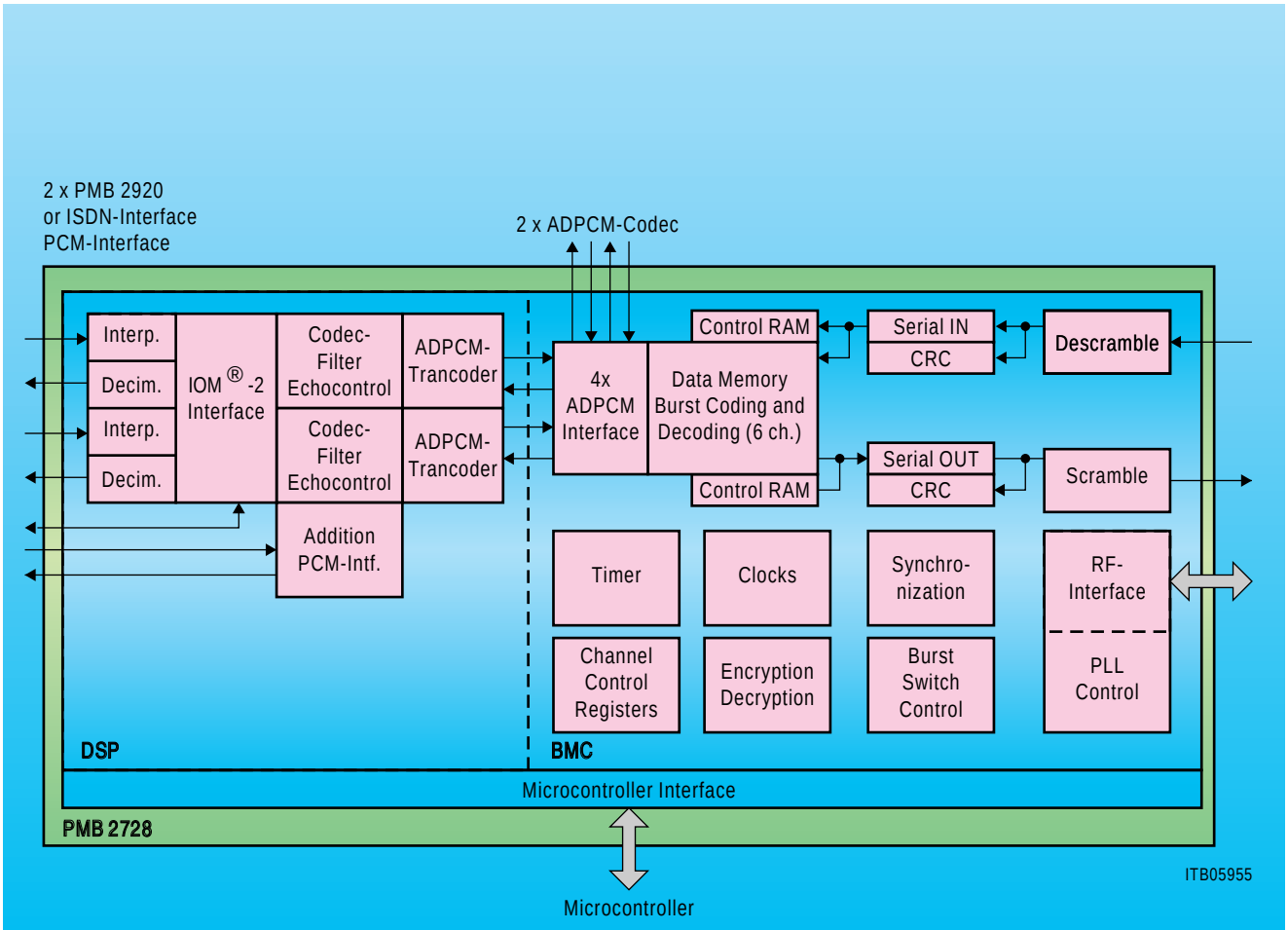
Type	Package
PMB 2728-H	P-MQFP-100-2 (SMD)

Features

- Power supply voltage: 5 V ± 5 %
- Low power consumption
- 100 pin P-MQFP packaging
- Advanced low power CMOS technology

Furthermore 1 IOM-2 interface is integrated e.r. for connection of an ISDN interface device (ISAC-S) or of a high feature codec device (ARCOFI, PSB 2163). For analog line interfaces two circuits PMB 2920 can be directly connected to the PMB 2728. Furthermore an additional PCM interface is implemented for connection of an answering machine.

The device is fabricated using Siemens advanced CMOS technology and will be available in a 100 pin package.



Block Diagram

General Description

The DECT-Analog Circuit is one of the devices of the Siemens chip set for the digital cordless telephone specified by the DECT standard.

The device designed for cordless handhelds and cordless fixed stations is a highly integrated circuit and realizes the analog front end functions needed in such systems. The circuit contains an A/D- and a D/A converter and adjustable gain stages. Connection of microphone and earpiece is possible with a minimum of external components.

Furthermore the device generates the reference voltages for the A/D converter the TXDA output voltage stabilization and the LCD-display-driver modules integrated in the DECT-Digital Circuit.

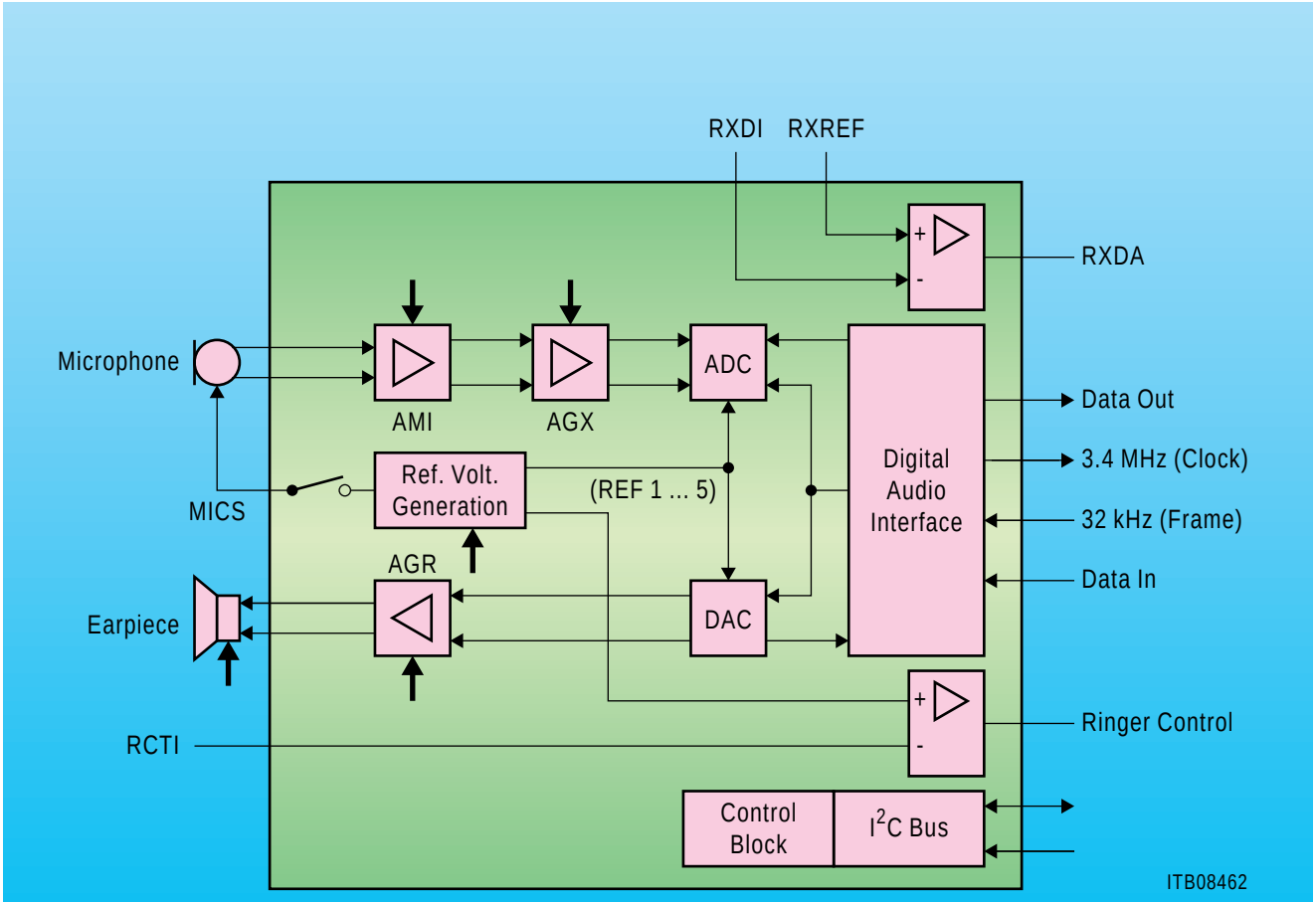
The reference voltages can be used together with external components and the PMB 27201, 27202, 27221, 27251, 27252 and 2728 for volume control of the ringer.

The device is fabricated using Siemens advanced ACMOS technology and will be available in a 24 pin package.

Type	Package
PMB 2920-S	P-SSOP-24-1 (Shrink, SMD)

Features

- High performance A/D- and D/A conversion
- Adjustable analog amplifiers
- Analog front end for direct connection of a handset mouth and earpiece
- On-chip microphone supply generation
- Power savings power-down and MUTE functions
- Comparator for preprocessing of the demodulated receive signal
- Reference voltage generation for on-chip A/D- and D/A converters and for the DECT-Digital Circuit
- Support of volume control of the tone ringer signal



Block Diagram

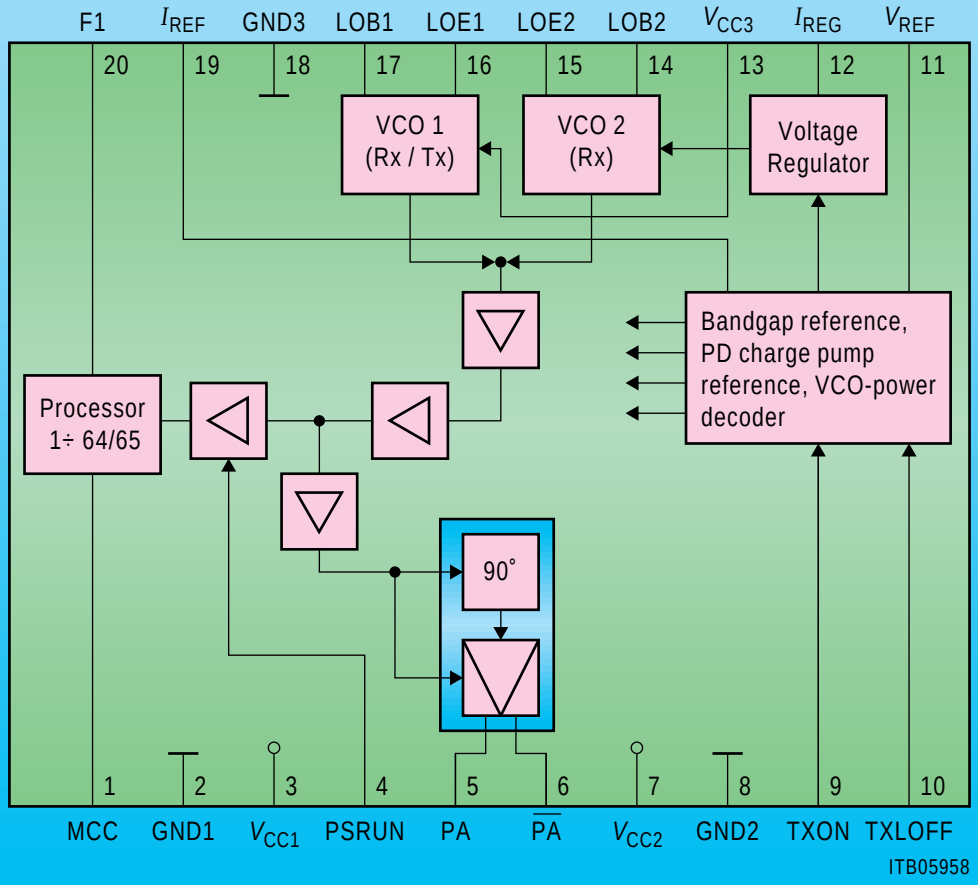
General Description

The PMB 2220 is a high speed analog bipolar IC and is one of the Siemens chipset for the Digital European Cordless Telephone. Combined with PLL (i.e. PMB 2306) and a power amplifier, the PMB 2220 device performs a complete DECT transmitter. Additionally the phase locked loop can be switched to receive mode and be used as a local oscillator for the receiver mixer of PMB 2420.

Type	Package
PMB 2220-S	P-SSOP-24-1 (Shrink, SMD)

Features

- Either single VCO operation (for receive and transmit) or dual VCO operation (one for receive and one for transmit) possible
- 64/65-prescaler on chip
- Frequency doubler for receive and transmit mode with balanced driver outputs
- Supply voltage regulator (with external pnp-transistor) for the two VCO's
- Power-down for the inactive VCO
- Current reference output for PLL charge pump to get constant lock-in time
- Wide power supple range 3.0 ... 5.5 V



Block Diagram

General Description

The PMB 2420 is a high speed analog bipolar IC and is one of the Siemens chipset for the Digital European Cordless Telephone specified by the DECT standard. All control inputs and the RSSI signal output match with the PMB 27201/2 and 27221 and 27251/2 and 2728 and 2727 digital circuits.

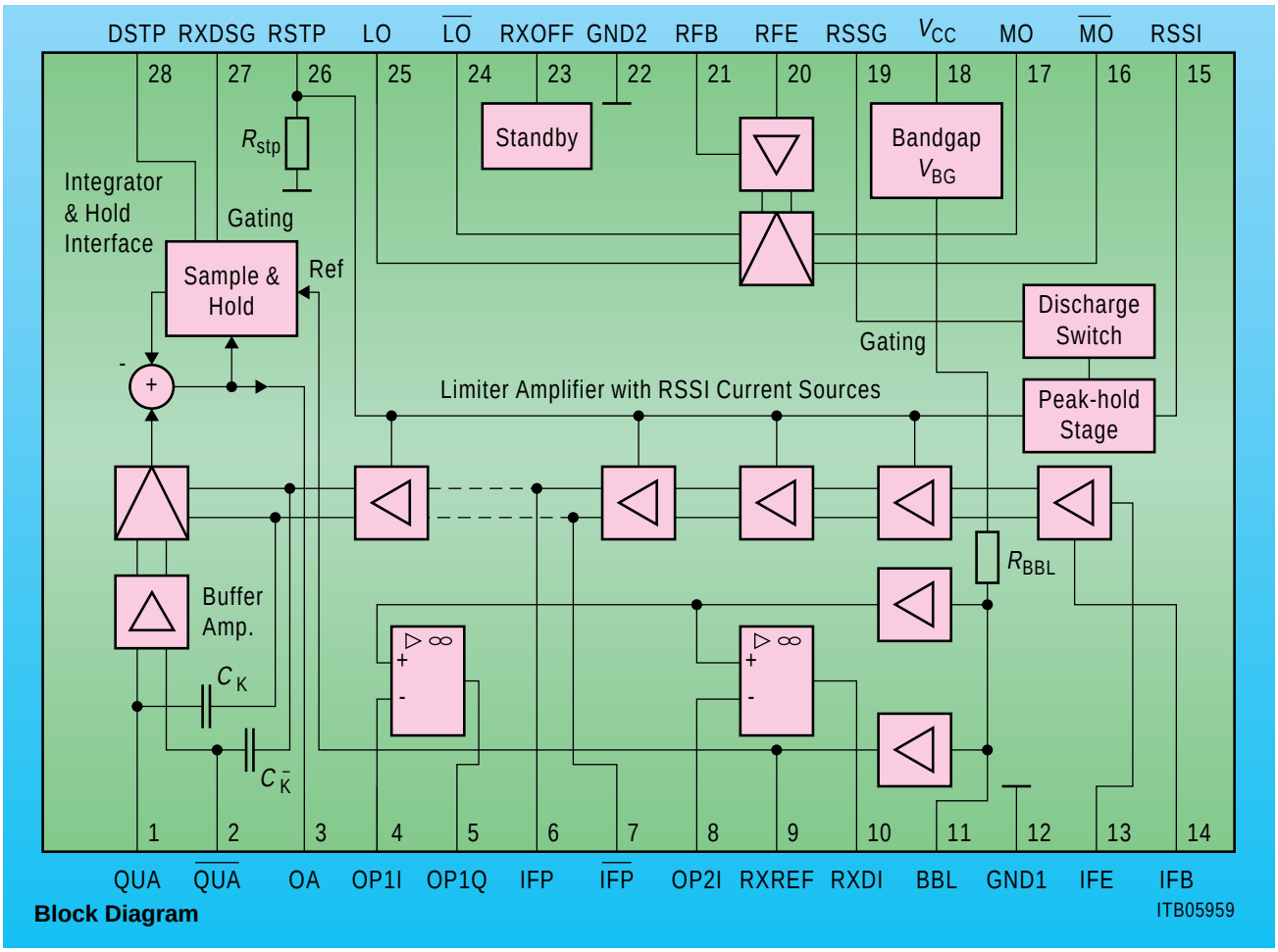
The IC operates as a heterodyne receiver using an intermediate frequency (IF) at 110 MHz. It consists of a mixer to downconvert the DECT-RF signal from 1.89 GHz to 110 MHz, a limiter amplifier, a field strength measurement unit (RSSI) with a peak-hold output, a coincidence demodulator, a sample-and-hold circuit for offset compensation and two operational amplifiers for basehand filtering.

Features

- Wide supply range 3.0 … 5.5 V
- Single conversion solution;
  advantages are: low supply current of total RF part
  no second IF image frequency and therefore insensitive to strong transmitters at FM radiofrequencies
  low total component count 1st mixer included on chip

Type	Package
PMB 2420-S	P-SSOP-28-1 (Shrink, SMD)

- Single balanced RF mixer with current-saving open collector output on chip
- Limiter and RSSI dynamic range: 75 dB for IF between 40 MHz and 115 MHz
- RSSI output independent of supply voltage and temperature with 3 dB accuracy
- Peak-hold output for the RSSI signal, reset by the controller via RSSG
- Sample-and-hold control circuit for baseband threshold acquisition, loop opened and closed via RXDSG, offset compensation value is stored during standby mode
- Timing for RSSI and sample-and-hold determined by the controller
- Two operational amplifiers on chip for baseband filtering, included in sample and hold control loop
- Standby mode with reduced supply current
- Balanced circuitry throughout the RF and IF
- Parts to improve signal isolation
- Maybe applied as part of a complete DECT-chipset solution



Block Diagram

RF-Building Blocks

Introduction

The era of the mobile communications has lead to an explosion in the variety of RF applications. Active for many years in this field with high performance IC solutions, Siemens RF ICs have found use in almost all wireless systems and are generally recognized for their high performance, functionality and cost-effectiveness.

Building upon the success of the PMB 2200 modulator family, the PMB 2401 receiver and Siemens PLLs (TBB 200/TBB 206/PMB 2306), the new B6HF 25 GHz bipolar technology will allow for a further increase in performance, 3-V lower current consumption as well as for higher frequencies. Starting with the new prescalers PMB 2313/2314, all the standard RF-building blocks will be gradually moved to B6HF.

Product Overview

Type	Description	Applications	Page
Modulator/Transmitter ICs			
PMB 2200	Direct Vector Modulator	Cellular (GSM, PDC, DAMPS, CDMA), WLAN, QPSK/QAM modulation up to 1 GHz	37
PMB 2201 B6HF	Direct Vector Modulator + Mixer, 2.7 V	Cellular (GSM, PDC, DAMPS, CDMA), WLAN, QPSK/QAM modulation 0.8 GHz to 1.5 GHz	38
PMB 2202 B6HF	Direct Vector Modulator + Mixer, 2.7 V	Cellular (PCN, PCS, PDC), Cordless (PHS, WCPE) WLL, WLAN, QPSK/QAM modulation 1.5 GHz to 2.5 GHz	38
PMB 2205	Direct Vector Modulator	Cellular (GSM, PCN, PCS, PDC, DAMPS, CDMA), Cordless (PHS, WCPE) WLL, WLAN, QPSK/QAM modulation	41
PMB 2207 B6HF	Vector Modulator + Upconverter Mixer, 2.7 V	Cellular (GSM, PCN, PCS, PDC, DAMPS, CDMA), Cordless (PHS) WCPE, WLL, WLAN, QPSK/QAM modulation	42
PMB 2220	DECT Transmitter, 3 V	Cordless (DECT), FSK modulation	33
PMB 2240 B6HF	GSM Transmitter, 2.7 V	Cellular (GSM, PDC), QPSK/QAM modulation 0.8 GHz to 1.0 GHz	21
PMB 2245 B6HF	PCN Transmitter, 2.7 V	Cellular (PCN, PCS), Cordless (PHS), QPSK/QAM modulation 1.65 GHz to 1.85 GHz	21
PMB 2247 B6HF	PCS Transmitter, 2.7 V	Cellular (PCN, PCS), Cordless (PHS), QPSK/QAM modulation 1.8 GHz to 1.95 GHz	21
Demodulator/Receiver ICs			
PMB 2401	Receiver/Demodulator Circuit	Cellular (GSM, PDC, DAMPS, CDMA), WLAN, QPSK/QAM demodulation up to 0.9 GHz	43
PMB 2402	Broadband Receiver/Vector Demodulator	CATV, Satellite (MSAT, VSAT), DS, WLL, WLAN	44
PMB 2405 B6HF	GSM Receiver, 2.7 V	Cellular (GSM, PDC, DAMPS), WLAN, QPSK/QAM demodulation up to 2.5 GHz	23
PMB 2407 B6HF	PCN/PCS Receiver, 2.7 V	Cellular (PCN, PCS), WLAN, QPSK/QAM demodulation up to 2.5 GHz	23
PMB 2420	DECT Receiver, 3 V	Cordless (DECT), FSK demodulation	34

Product Overview (cont'd)

Type	Description	Applications	Page
Frequency Synthesizer, Prescaler ICs			
PMB 2302 B6HF	1.25 GHz Dual PLL with Prescaler, 2.7 V	All analog and digital systems as RF-, IF synthesizer up to 1.25 GHz	45
PMB 2303 B6HF	2.5 GHz Dual PLL with Prescaler, 2.7 V	All analog and digital systems as RF-, IF synthesizer up to 2.5 GHz	45
PMB 2306	PLL Frequency Synthesizer	All analog and digital systems as RF-, IF synthesizer up to 220 MHz	47
PMB 2307	PLL Frequency Synthesizer, 2.7 V	All analog and digital systems as RF-, IF synthesizer up to 220 MHz	47
PMB 2308 B6HF	1.25 GHz PLL with Prescaler, 2.7 V	All analog and digital systems as RF-, IF synthesizer up to 1.25 GHz	49
PMB 2309 B6HF	2.5 GHz PLL with Prescaler, 2.7 V	All analog and digital systems as RF-, IF synthesizer up to 2.5 GHz	49
PMB 2313 B6HF	1.1 GHz Prescaler :64/65 :128/129; 2.7 V	All analog and digital systems as part of RF- and IF synthesizer up to 1.1 GHz	51
PMB 2314 B6HF	2.1 GHz Prescaler :64/65 :128/129; 2.7 V	All analog and digital systems as part of RF- and IF synthesizer up to 2.1 GHz	51
LNA/Mixer, Driver/Mixer, Mixer ICs			
PMB 2330	2.0 GHz Mixer	All analog and digital systems as up- and downconversion mixer up to 2.0 GHz	52
PMB 2331 B6HF	2.0 GHz Mixer, 2.7 V	All analog and digital systems as up- and downconversion mixer up to 2.0 GHz	52
PMB 2332 B6HF	1.1 GHz LNA + Mixer, 2.7 V	All analog and digital systems as frontend-LNA and mixer up to 1.1 GHz	53
PMB 2333 B6HF	3 GHz LNA/Driver + Mixer, 2.7 V	All analog and digital systems as frontend-LNA or preamplifier-driver and mixer up to 3 GHz	54

General Description

The PMB 2200 is a direct quadrature modulator for use in mobile communication equipment.

An external LO signal f_0 is fed to the modulator input. This signal is first doubled and then bandpass filtered at $2f_0$. This frequency is the clock for a 2:1 divider. At the output of the divider orthogonal carriers are provided which are mixed with the baseband modulation signals by two multipliers. The outputs of the multipliers are added and amplified by a linear output stage.

The EN pin allows the modulator to be switched in power-down mode.

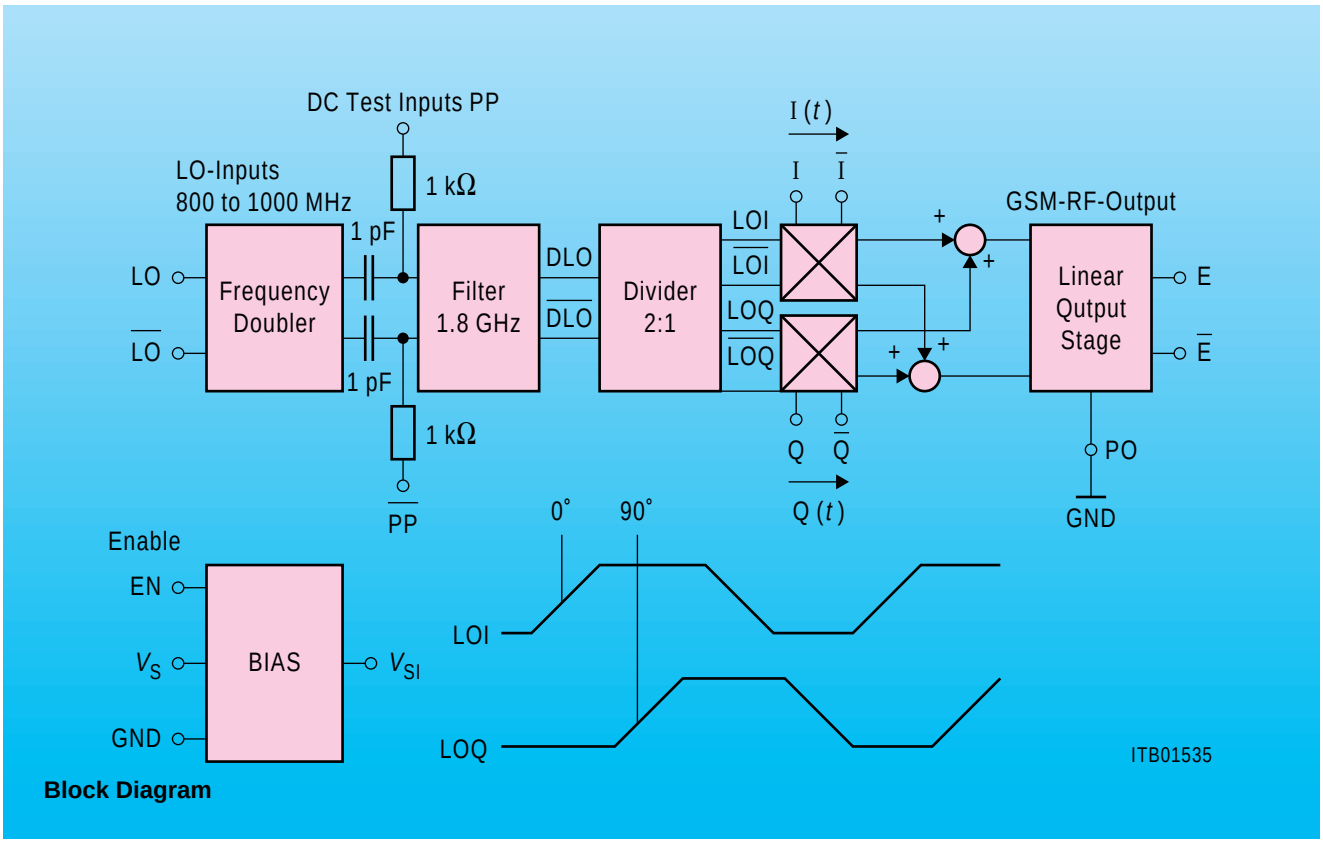
Applications

- Vector modulated cellular and cordless systems: GSM, PDC, DAMPS, CDMA, WLAN, etc.
- Various modulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK etc.
- Analog systems with FM- and AM modulation
- Space and power saving optimizations of existing discrete transmitter circuits

Type	Package
PMB 2200-T	P-DSO-20-1 (SMD)
PMB 2200-S	P-SSOP-20-1 (Shrink, SMD)

Features

- Direct modulation vector modulator
- Linear modulating inputs
- Symmetrical circuitry
- Wide LO-frequency range 0.8 GHz to 1.0 GHz
- Generation of orthogonal carriers without external elements and without trimming
- 35 dB carrier rejection, 42 dB SSB rejection
- 42 dB rejection of third order products
- 0 dBm linear output power
- Modulation frequency range 0 to 400 MHz
- Power-down mode
- P-DSO-20 or P-SSOP-20 package
- Temperature range – 25 °C to 85 °C



Block Diagram

General Description

The PMB 2201, 2202 family is a direct quadrature modulator and double balanced mixer. It is fabricated using Siemens B6HF silicon bipolar process. In a typical application the wanted mixer output product is bandpass filtered and then fed to the modulator LO input. The mixer may also be used to upconvert the modulator output signal to higher frequencies up to 2.5 GHz.

The modulator generates two orthogonal carriers which are mixed with the baseband modulation signals by two multipliers. The outputs of the multipliers are added and amplified by a linear output stage. The modulator and the mixer have separate power supplies and grounds. They can be powered down independently.

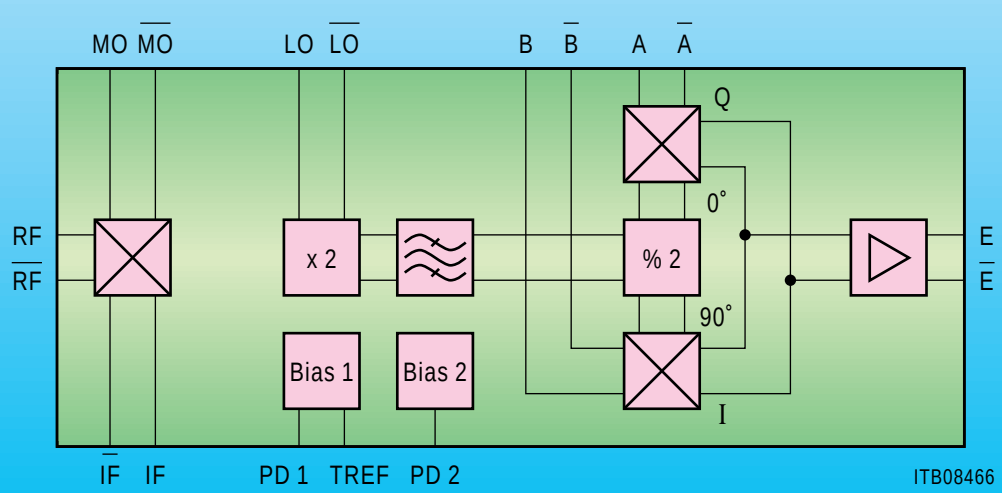
Applications

- Vector modulated cellular and cordless systems:
  PMB 2201: GSM, PDC, DAMPS, CDMA, WLAN,
  PMB 2202: PCN, PCS, PDC, PHS, WCPE, WLL, WLAN, etc.
- Various modulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK etc.
- Analog systems with FM- and AM modulation
- Space and power saving optimizations of existing discrete transmitter circuits

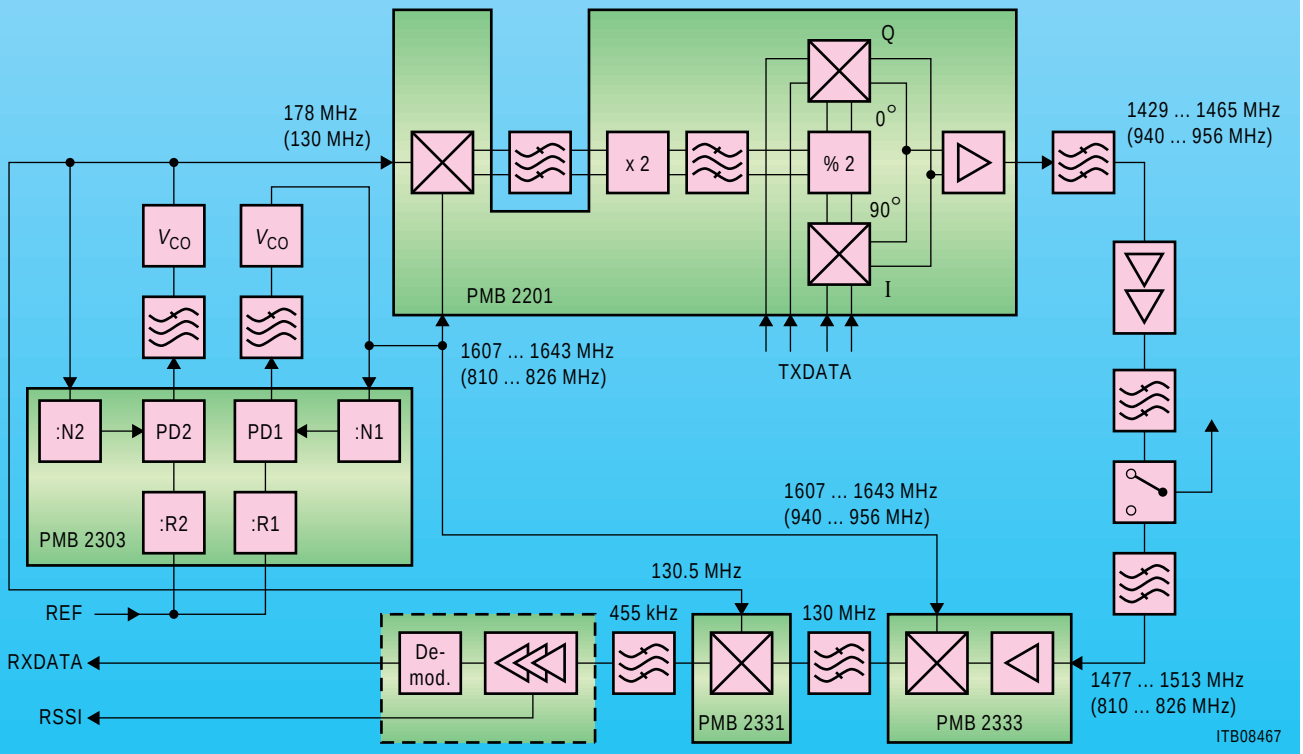
Type	Package
PMB 2201-R	P-TSSOP-24-1 (SMD)
PMB 2202-R	P-TSSOP-24-1 (SMD)

Features

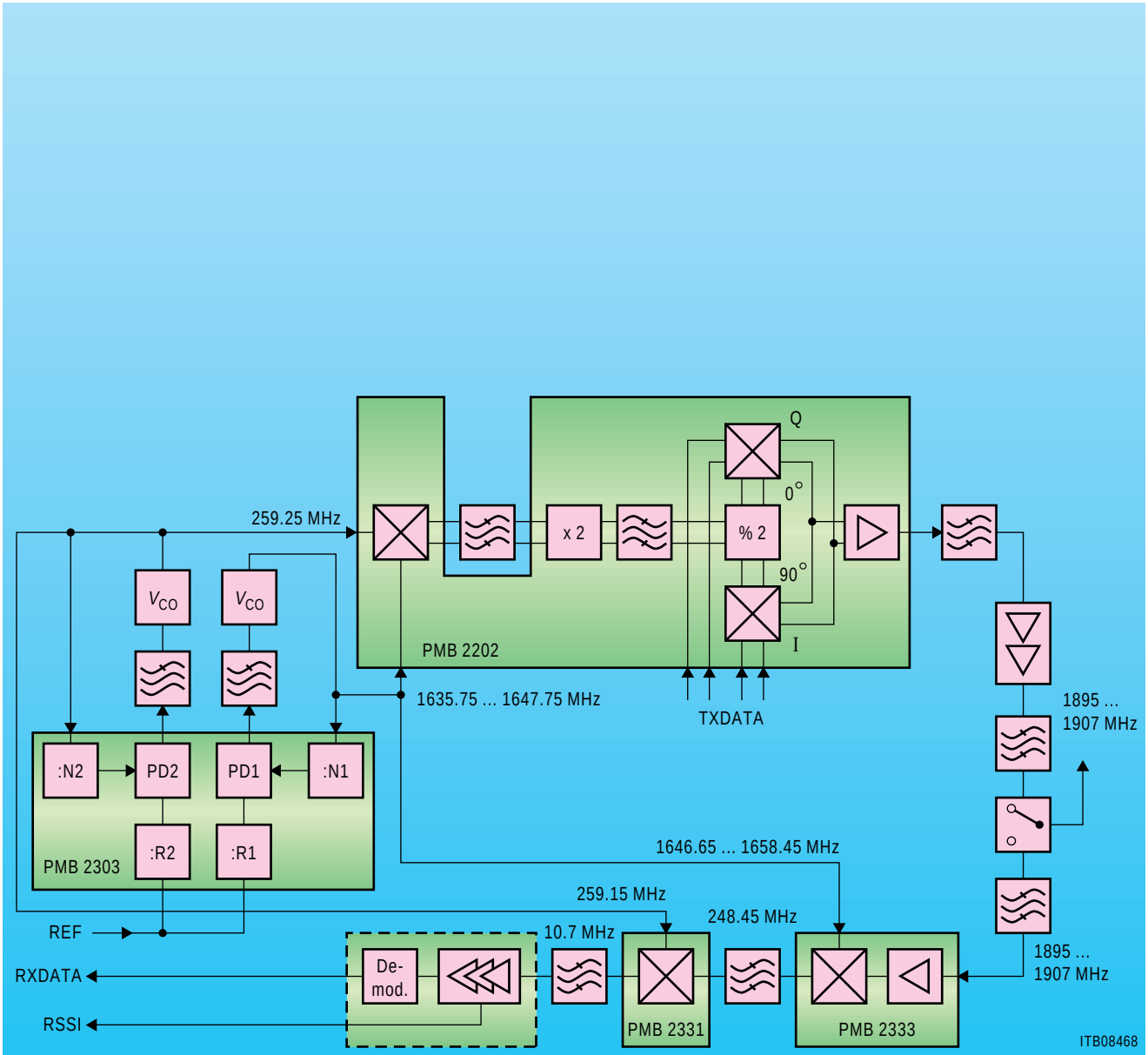
- Direct modulation vector modulator
- Wide LO-frequency range
  PMB 2201: 0.8 GHz to 1.5 GHz
  PMB 2201: 1.5 GHz to 2.5 GHz
- Generation of orthogonal carriers without external elements and without trimming
- 35-dB carrier rejection, 40-dB SSB rejection
- 42-dB rejection of third order products
- 0-dBm modulator output power
- Independent double balanced Gilbert cell mixer
- RF- and IF-frequency range from DC to 2.5 GHz
- Low noise figure, high conversion gain
- Supply voltage range from 2.7 V to 5.5 V
- Low power consumption
- Power-down mode
- P-TSSOP-24 package
- Temperature range – 30 °C to 85 °C



Block Diagram



PDC Application PMB 2201 / PMB 2303 / PMB 2331 / PMB 2333



PHS Application PMB 2202 / PMB 2303 / PMB 2331 / PMB 2333

General Description

The PMB 2205 is a direct quadrature modulator for use in mobile communication equipment.

An external LO signal f_0 is fed to the modulator input. This signal is first doubled and then bandpass filtered at $2f_0$. The filter may be realized by an external tank circuit. Alternatively, a local oscillator operating at $2f_0$ may be connected to the divider input. This signal is the clock for a 2:1 divider. At the output of the divider orthogonal carriers are provided which are mixed with the baseband modulation signals by two multipliers. The outputs of the multipliers are added and amplified by a linear output stage.

The EN pin allows the modulator to be switched in power-down mode.

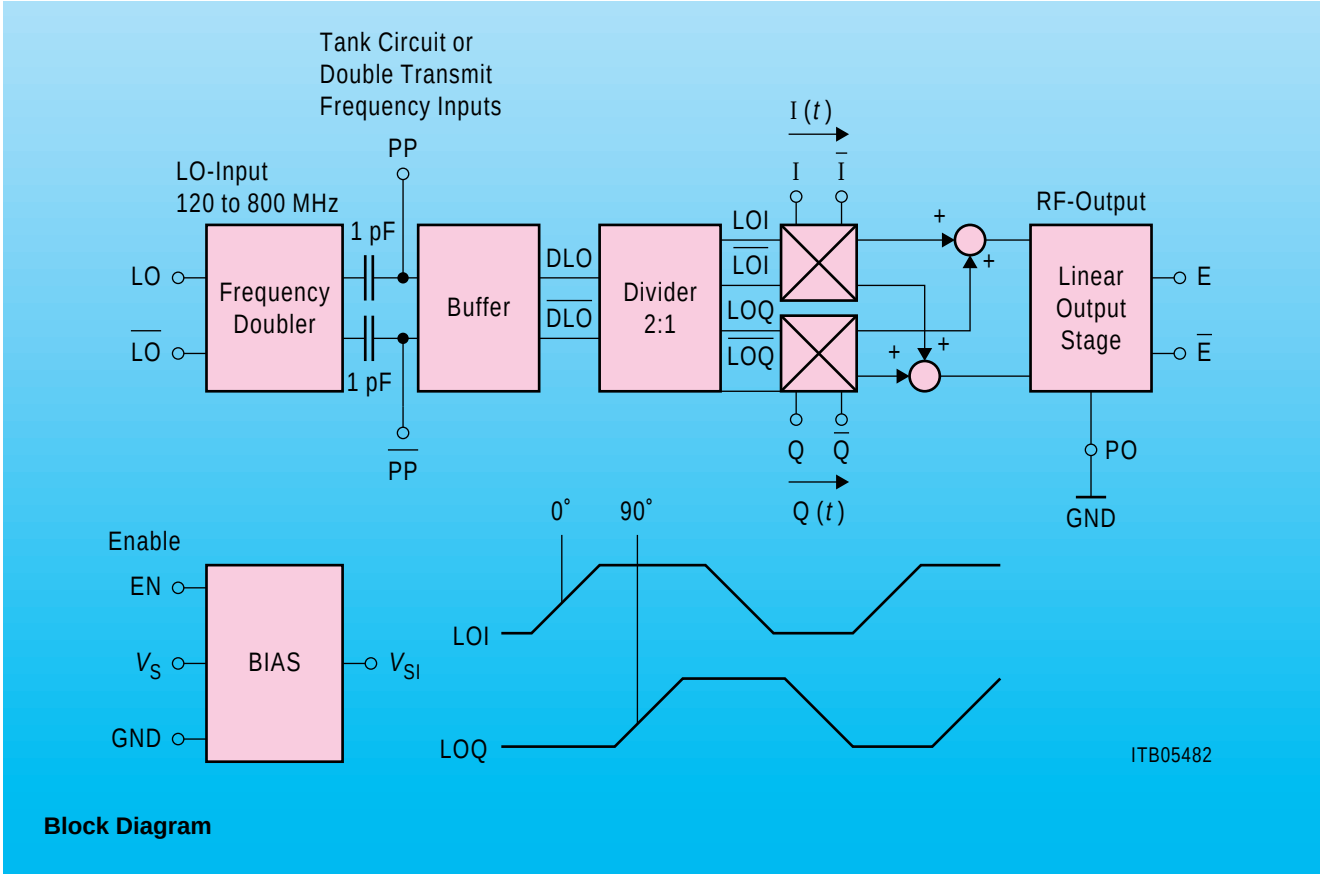
Applications

- Vector modulated cellular and cordless systems: GSM, PCN, PCS, PDC, DAMPS, CDMA, WLAN, etc.
- Various modulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK etc.
- Analog systems with FM- and AM modulation
- Space and power saving optimizations of existing discrete transmitter circuits

Type	Package
PMB 2205-T	P-DSO-20-1 (SMD)
PMB 2205-S	P-SSOP-20-1 (Shrink SMD)

Features

- Direct modulation vector modulator
- Linear modulating inputs
- Symmetrical circuitry
- Wide LO-frequency range 120 MHz to 800 MHz
- LO operation alternatively at transmit frequency or double transmit frequency
- Generation of orthogonal carriers within a wide frequency range
- 35 dB carrier rejection, 42 dB SSB rejection
- 42 dB rejection of third order products
- 0 dBm linear output power
- Modulation frequency range 0 to 400 MHz
- Power-down mode
- P-DSO-20 or P-SSOP-20 package
- Temperature range – 25 °C to 85 °C



Block Diagram

General Description

The PMB 2207 is a direct quadrature modulator and double balanced mixer. It is fabricated using Siemens B6HF silicon bipolar process. In a typical application the modulator output signal is bandpass filtered and then fed to the mixer input for upconversion.

An external LO signal is fed to the modulator input. The modulator generates two orthogonal carriers which are mixed with the baseband modulation signals by two multipliers. The outputs of the multipliers are added and amplified by a linear output stage. The modulator and the mixer have separate power supplies and grounds. They can be powered down independently.

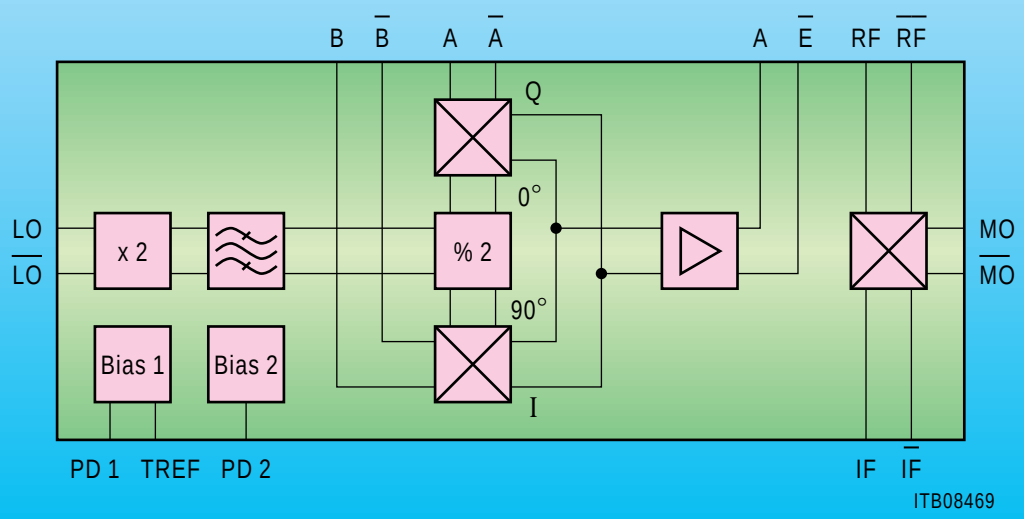
Applications

- Vector modulated cellular and cordless systems: GSM, PCN, PCS, PDC, DAMPS, CDMA, PHS, WCPE, WLL, WLAN, etc.
- Various modulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK etc.
- Analog systems with FM- and AM modulation
- Space and power saving optimizations of existing discrete transmitter circuits

Type	Package
PMB 2207-R	P-TSSOP-24-1 (Shrink, SMD)

Features

- Vector modulator with upconverter mixer
- Wide LO-frequency range from 80 MHz to 800 MHz
- Mixer RF-frequency range up to 2.5 GHz
- Generation of orthogonal carriers without external elements and without trimming
- 35 dB carrier rejection, 40 dB SSB rejection
- 42 dB rejection of third order products
- 0 dBm modulator output power
- Independent double balanced Gilbert cell mixer
- IF-frequency range from DC to 2.5 GHz
- Low noise figure, high conversion gain
- Supply voltage range from 2.7 V to 5.5 V
- Power-down mode
- P-TSSOP-24 package
- Temperature range – 30 °C to 85 °C



Block Diagram

Preliminary Data

General Description

The PMB 2401 is a single-chip double-conversion heterodyne PM receiver with phase shifting circuitry for the I/Q-phase demodulation on chip. It also includes the second local oscillator, a gain controlled 2nd IF amplifier, 2 differential operational amplifiers for audio purposes and power-down circuitry.

The PMB 2401 is designed for digital mobile telephones according the GSM standard and other digital systems.

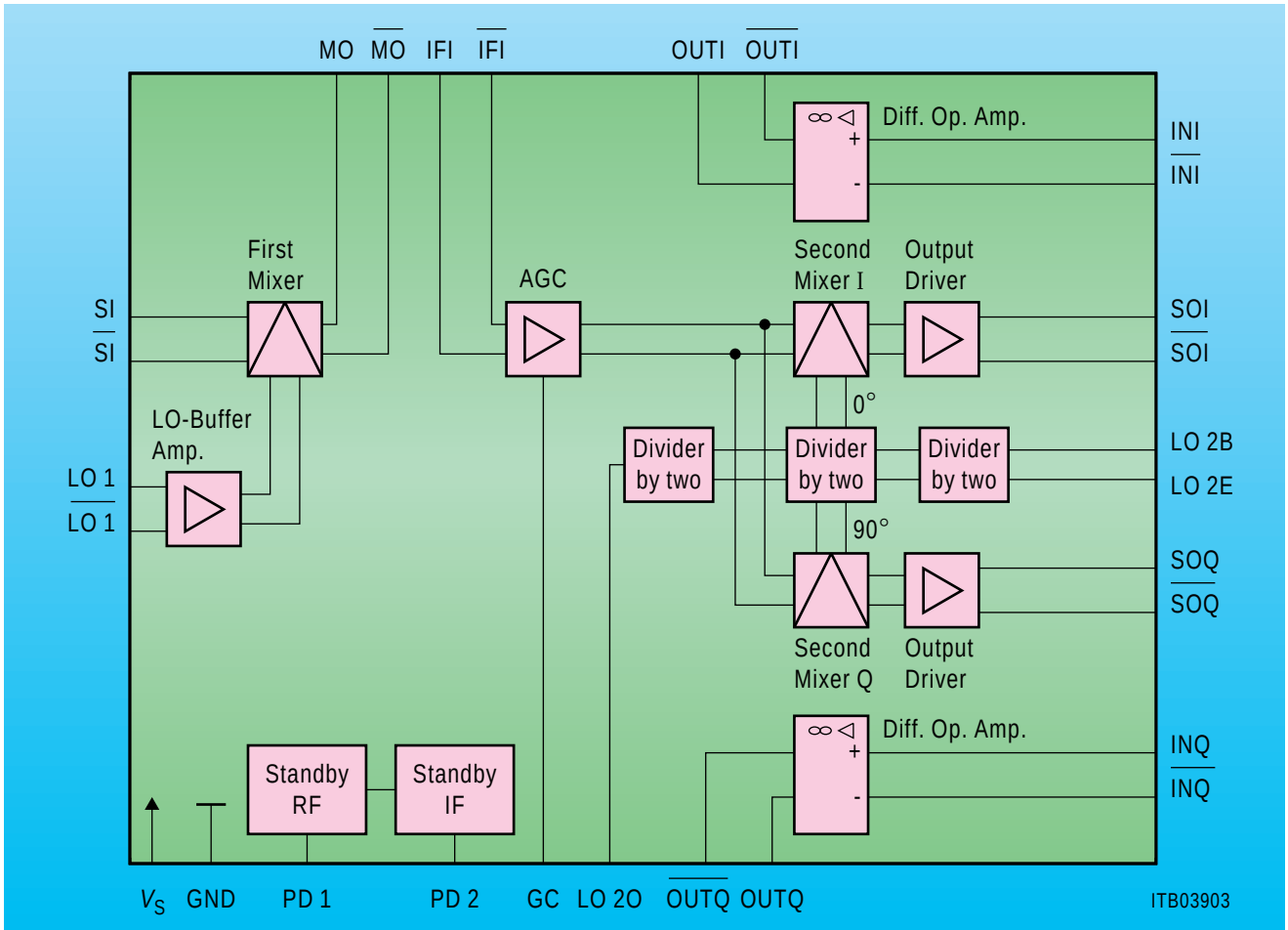
Application

- Digital mobile cellular systems as GSM, PDC, DAMPS
- Various demodulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK
- Space and power saving optimizations of existing discrete demodulator circuits

Type	Package
PMB 2401-T	P-DSO-28-1 (SMD)
PMB 2401-S	P-SSOP-28-1 (Shrink, SMD)

Features

- Heterodyne receiver with demodulator
- Down mixing from 900-MHz receiver band to the base band
- Demodulation and generation of I/Q components
- Lower mixer noise to 10 dB (SSB)
- High intercept point + 2 dBm
- Integrated phase shifter for I/Q demodulator
- 82-dB AGC range
- On-chip second LO oscillator with external tuning circuit
- Two differential operational amplifiers
- Low power consumption due to highly flexible power-down capability
- Wide input frequency range up to 1 GHz
- Wide IF range from 35 MHz to 100 MHz
- P-DSO-28 package, P-SSOP-28 (Shrink)
- Temperature range – 25 °C to 85 °C



Block Diagram

General Description

The PMB 2402 is a single-chip single-conversion heterodyne receiver with phase shifting circuitry for the I/Q phase local baseband demodulation on chip. It also includes the second oscillator, a gain controlled second IF amplifier, two differential operational amplifiers for baseband fitering purposes and power-down circuitry.

The PMB 2402 is designed for digital mobile telephones according to the GSM standard and other digital systems.

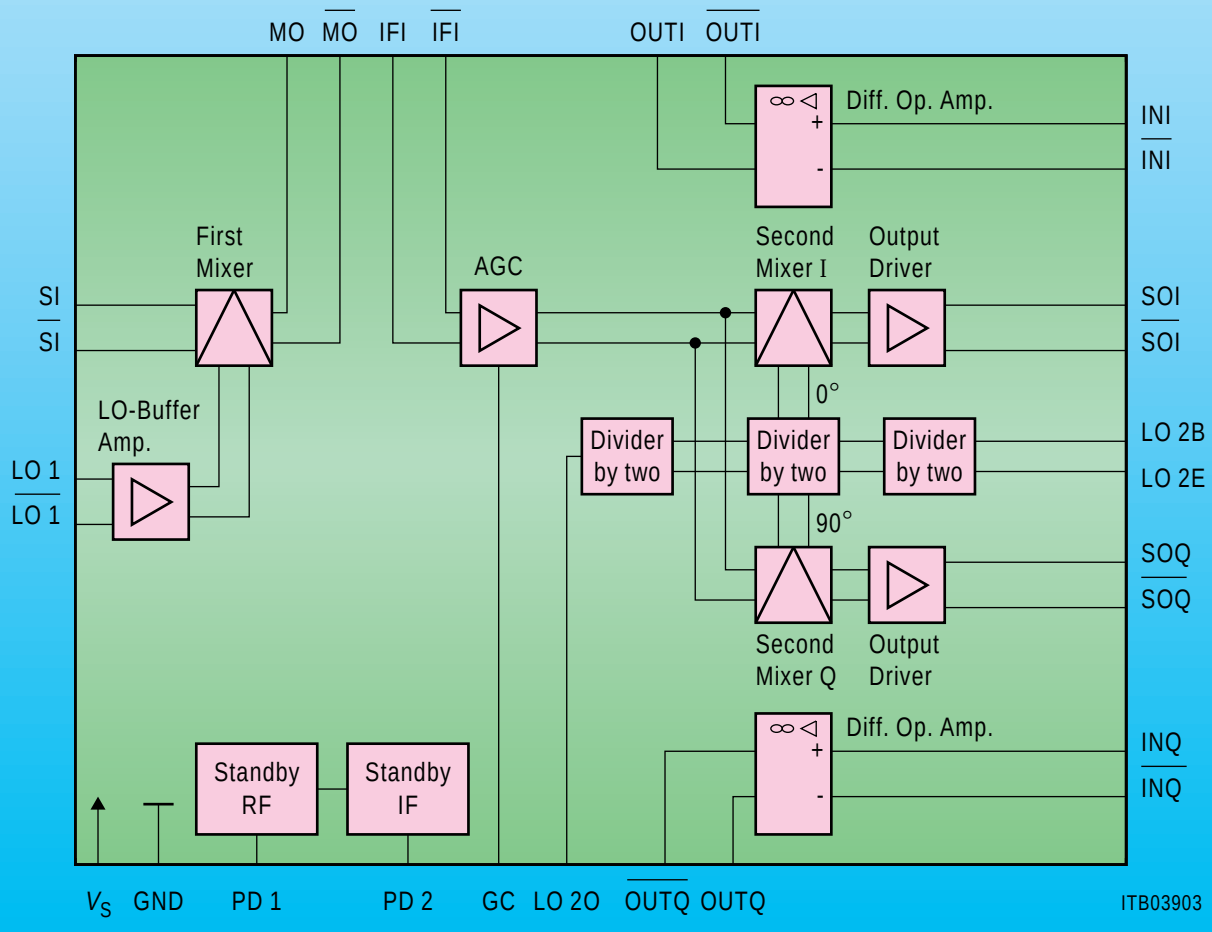
Applications

- Digital wideband systems as CATV, Satellite, DBS, WLAN
- Various demodulation schemes, such as PM PSK, FSK, QAM, QPSK, GM
- Space and power saving optimization of existing discrete demodulator circuit

Type	Package
PMB 2402-S	P-DSO-28-1 (SMD)

Features

- Heterodyne receiver with demodulators
- Down mixing from 900 MHz receiver band to the base band
- Demodulation and generation of I/Q-baseband components
- Low mixer noise 10 dB (SSB)
- Input high intercept point + 2 dBm
- Integrated 0° and 90° phase shifter
- 82 dB AGC range
- On-chip second LO oscillator with external tuning circuit
- Low power consumption due to highly flexible power-down capability
- Wide input frequency range up to 1 GHz
- Wide IF range from 35 MHz to 100 MHz
- Wide output frequency range up to 13.5 MHz
- Temperature range – 25 °C to 85 °C



Block Diagram

General Description

The PMB 2302, PMB 2303 are single chip dual Phase Locked Loop (PLL) synthesizers with programmable frequency dividers for use in mobile communication equipment. It is fabricated using Siemens B6HF silicon bipolar process.

The circuit consists of high speed dual modulus dividers, shift registers, programmable counters (2 A-, 2 N- and 2 R-counters), phase detectors with charge pump and a control logic block.

Since one of the high speed dual modulus dividers is able to handle frequencies of up to 1.25 GHz (2.5 GHz), there is no need to add a dedicated external prescaler. The second dual modulus divider handles frequencies up to 500 MHz. The switching signals for the dividing ratios are generated by the corresponding A-counters.

The A-counter and the N-down-counter are programmable via the 3-wire bus. They are clocked by the dual modulus divider output signals. The carry outputs of the N-counters are connected to the frequency inputs of the corresponding phase detectors and are controlling the loading of the programmed A-/N-counter start values.

The two 11 bit R-counters are also programmable and are serving as reference frequency dividers. Their carry outputs are connected to the corresponding reference frequency inputs of the phase detector and are controlling the loading of the programmed counter start values.

The phase detectors are of PFD-type (phase and frequency sensitive). They have a linear output characteristic in the 0˚ phase error region.

The control logic handles phase detectors output polarity, charge pump output currents and software-generated power-on (all circuit parts except the shift registers and data latches).

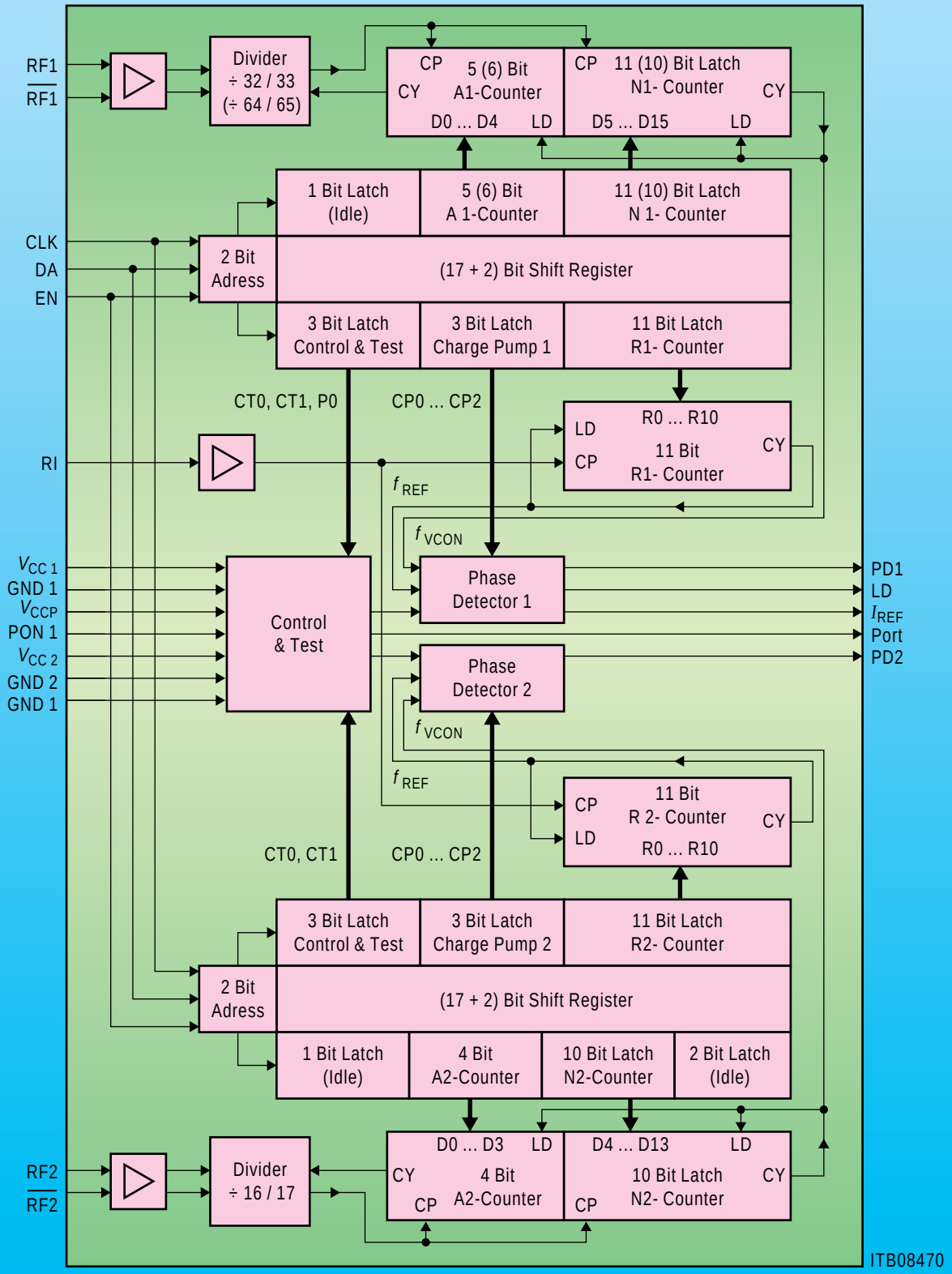
Applications

All mobile communication analog and digital systems as RF- and IF synthesizers

Type	Package
PMB 2302-R	P-TSSOP-20-1 (Shrink, SMD)
PMB 2303-R	P-TSSOP-20-1 (Shrink, SMD)

Features

- Integrated prescaler
- Low operating current
- Different power-down modes
- High input sensitivity, high input frequency
- Two fast phase detectors without dead zone
- Linearization of the phase detector output by current sources
- Large dividing ratios for small channel spacing
- PLL1 PMB 2302 PMB 2303
  max. freq. 1.25 GHz 2.5 GHz
  prescaler: :32/:33 :64/:65
  A1-counter 0 to 31 0 to 63
  N1-counter 32 to 2047 64 to 1023
  R1-counter 3 to 2047 3 to 2047
- PLL2 PMB 2302 PMB 2303
  max. freq. 500 MHz 500 MHz
  prescaler: :16/:17 :16/:17
  A2-counter 0 to 15 0 to 15
  N2-counter 16 to 1023 16 to 1023
  R2-counter 3 to 2047 3 to 2047
- Serial control (3-wire bus: data, clock, enable) for fast programming (f_{max} = 10 MHz)
- Switchable polarity and phase detector current programmable
- 1 port output (TTL push-pull)
- External current setting for phase detector outputs
- Lock detect output with gated pulse (quasi digital lock detect)
- Operating voltage 2.7 V to 5.5 V
- P-TSSOP-20 package
- Temperature range – 30 °C to 85 °C



Block Diagram

General Description

The PMB 2306, PMB 2307 PLL are high speed CMOS ICs are especially designed for use in battery-powered radio equipment and mobile telephones. The intended application will be in GSM, PCN, DECT and other digital mobile systems. The wide range of dividing ratios also allows application in analog systems.

The circuit consists of a reference-, A- and N-counter, a dual-modulus-control logic, a phase detector with charge pump and a serial control logic. The setting of the operating mode and the selection of the counter ratios is done serially at the ports CLK, DA and EN.

The operating modes allow the selection of single or dual operation, asynchronous or synchronous data acquisition, 4 different antibacklash-impulse times, 8 different PD-output current modes, polarity setting of the PD-output signal, adjustment of the trigger-edge of the MOD-output signal, 2 standby modes and the control of the multifunction outputs MFO1 and MFO2.

The reference frequency is applied at the RI input and scaled down by the R-counter. Its maximum value is 50 MHz. The VCO frequency is applied at the FI input and scaled down by the N- or N/A-counter according to single or dual-mode operation. The maximum value at FI is 220 MHz at single-, and 65 MHz at dual-mode operation.

The phase detector is frequency and phase sensitive. It produces a phase detector signal with adjustable anti-backlash impulses in order to prevent a dead zone at very small phase deviations. Phase differences smaller than 100 ps can therefore be resolved.

Programming of the IC is done by a serial data control. The contents of the messages are assigned to the functional units according to the destination address. Single or dual-mode operation as well as asynchronous or synchronous data acquisition is set by status 2 and should therefore precede the programming of the counters.

The PMB 2306/PMB 2307 offer the possibility of synchronous data acquisition to avoid error signals at the phase detector due to non-corresponding dividing factors in the counters produced by asynchronous loading.

Synchronous programming guarantees control during changes of frequency or channel. That means that the state of the phase detector or the phase difference is kept maintained, and in case of “lock in”, the control process starts with the phase difference “zero”.

Synchronous transmission is particularly advantageous when large transfers in channel are to be made in a specific short transient recovery time. For this purpose a larger reference frequency is switched to in order to achieve rapid-“rough”-transient response, increasing the bandwidth of the loop at the time. When reaching the “quasi lock-in” state, the reference frequency is switched back to its original values.

Type	Package
PMB 2306-T	P-DSO-14-1 (SMD)
PMB 2306-R	P-TSSOP-16-1 (Shrink, SMD)
PMB 2307-R	P-TSSOP-16-1 (Shrink, SMD)

Adjustment to the “actual” value then takes place with the usual transient response as for small transfers in channel. The synchronous transmission ensures that no additional phase errors arise due to the change of reference frequencies.

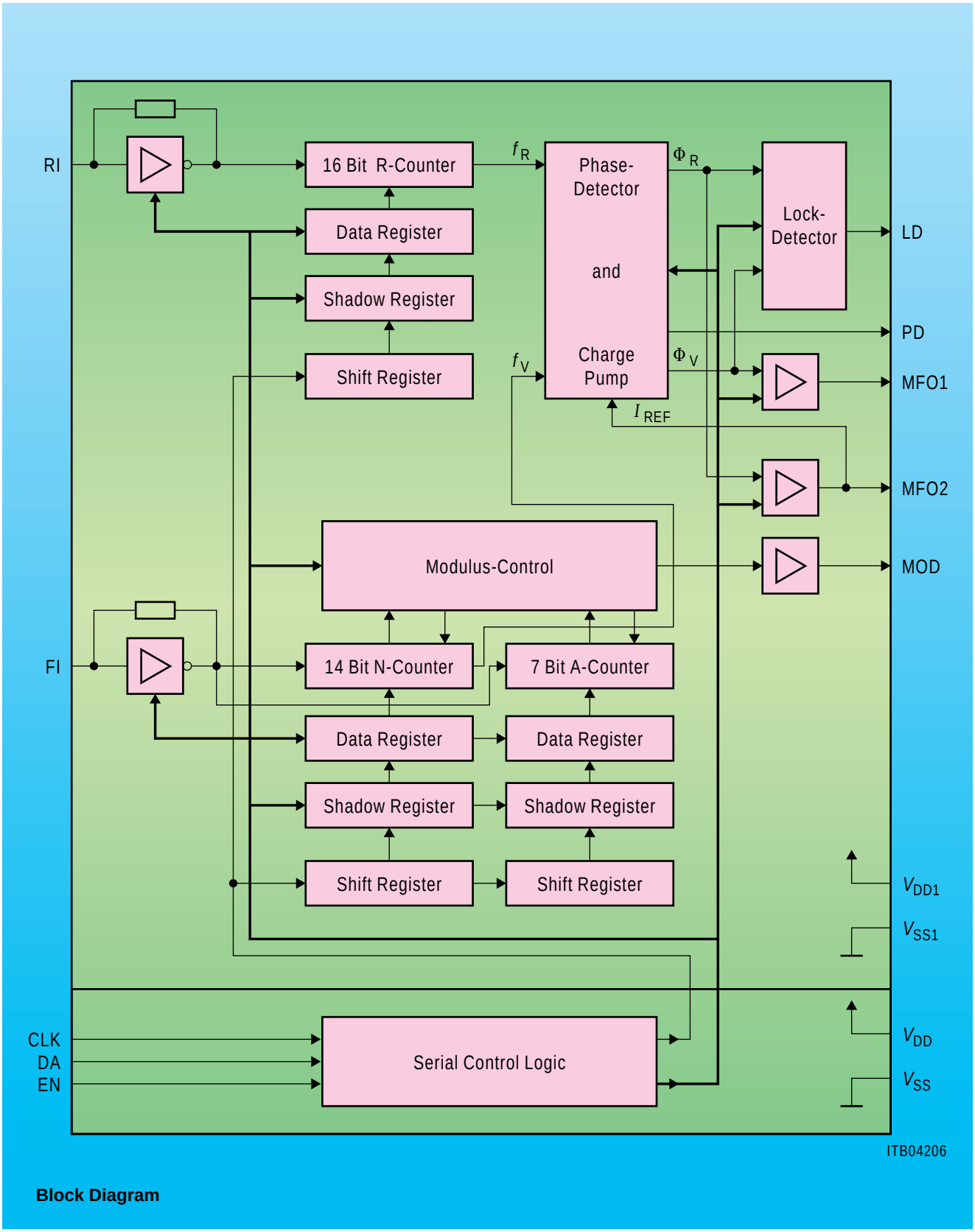
The PMB 2306/2307 has two standby modes (standby1, 2) to reduce the current consumption.

- Standby1 switches off the whole circuit, the current consumption is reduced to below 1 µA.
- Standby2 switches off the counters, the charge pump and the outputs, only the preamplifiers stay active.

The standby modes do not affect the port output signal. For the influence on the other output signals see standby table.

Features

- Low operating current consumption
- Low operating voltage
  PMB 2306: 3 V to 5.5 V
  PMB 2307: 2.7 V to 5.5 V
- High input sensitivity, high input frequencies (220 MHz)
- Extremely fast phase detector without dead zone
- Linearization of the phase detector output by current sources
- Synchronous programming of the counters (N-, N/A-, R-counters) and system parameters
- Fast modulus switchover for 65-MHz operation
- Switchable modulus trigger edge
- Large dividing ratios for small channel spacing
  – A-scaler 0 to 127
  – N-scaler 3 to 16380
  – R-scaler 3 to 65535
- Serial control (3-wire bus: data, clock, enable) for fast programming (f_{max} ~ 5 MHz)
- Switchable polarity and rate of trimming rise of the phase detector
- 2 multifunction outputs
- Digital phase detector output signals (e.g. for external charge pump)
- f_{rn}, f_{yn} outputs of the R- and N-scalers
- Port 1 output (e.g. for standby of the prescaler)
- External current setting for PD output
- Lock detect output with gated antibacklash pulse (quasi digital lock detect)



Block Diagram

General Description

The PMB 2308, PMB 2309 are Phase Locked Loop (PLL) synthesizers with programmable frequency dividers for use in mobile communication equipment. It is fabricated using Siemens B6HF silicon bipolar process.

The circuit consists of high speed dual modulus divider, shift register, programmable counter (A-, N- and R-counter), phase detector with charge pump and a control logic block.

Since the high speed dual modulus divider is able to handle frequencies of up to 1.25 (2.5) GHz, there is no need to add a dedicated external prescaler. The switching signals for the dividing ratio 16/17 (32/33) is generated by the A-counter.

The A-counter and the N-down-counter are programmable via the 3-wire bus. They are clocked by the dual modulus divider output signal. The carry output of the N-counter is connected to the frequency input of the phase detector and is controlling the loading of the programmed A-/N-counter start values.

The 11 bit R-counter is also programmable and is serving as reference frequency divider. Its carry output is connected to the reference frequency input of the phase detector and is controlling the loading of the programmed counter start value.

The phase detector is of PFD-type (phase and frequency sensitive). It has a linear output characteristic in the 0˚ phase error region.

The control logic handles phase detector output polarity, charge pump output current and software-generated power-down (all circuit parts except the shift registers and data latches).

Applications

All mobile communication analog and digital systems as RF- and IF synthesizers

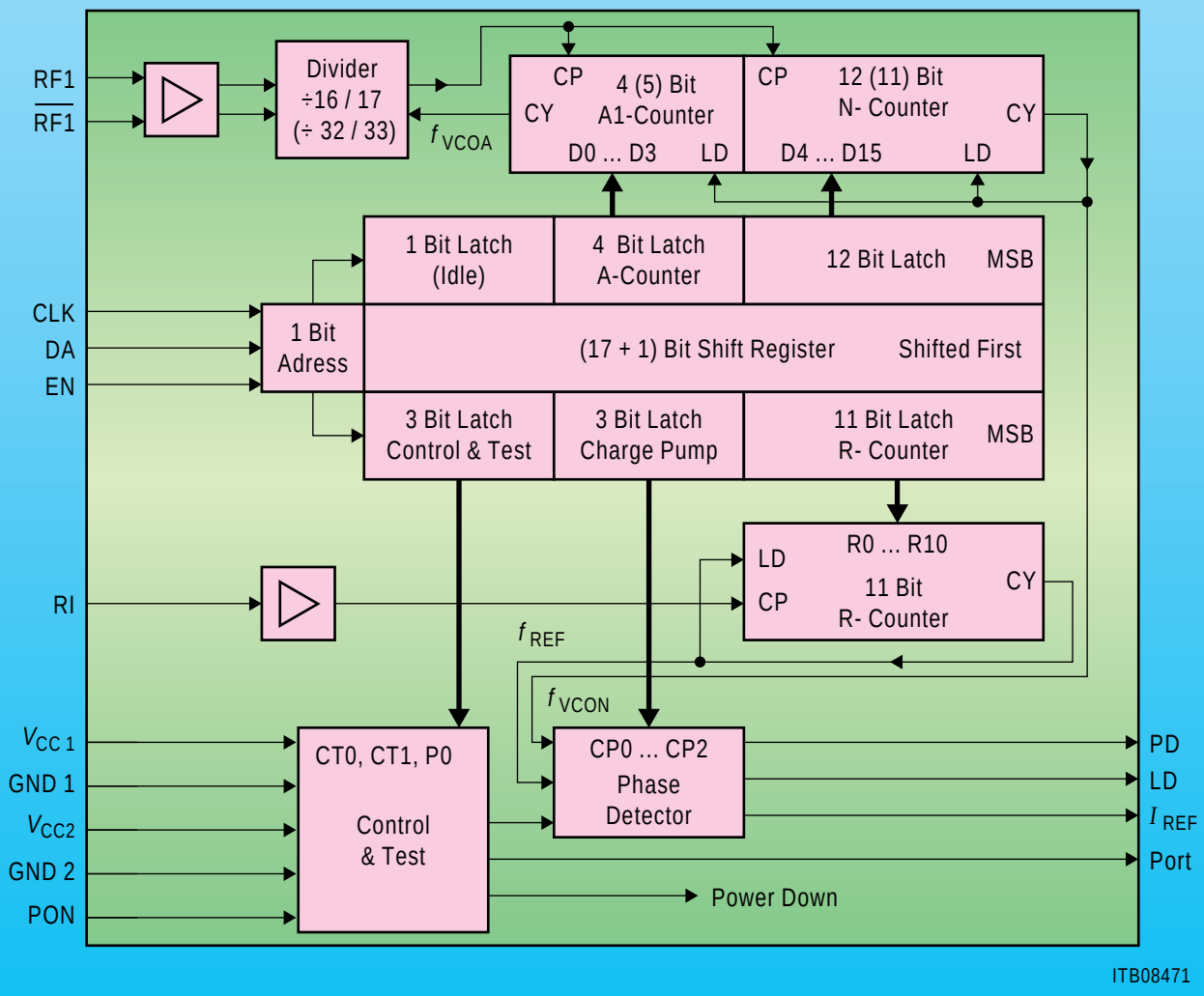
Type	Package
PMB 2308-R	P-TSSOP-16-1 (Shrink, SMD)
PMB 2309-R	P-TSSOP-16-1 (Shrink, SMD)

Features

- Integrated prescaler
- Low operating current
- Different power-down modes
- High input sensitivity, high input frequency
- Fast phase detector without dead zone
- Linearization of the phase detector output by current sources
- Large dividing ratios for small channel spacing
-

PLL	PMB 2308	PMB 2309
max. freq. prescaler:	1.25 GHz :16/:17	2.5 GHz :32/:33
A-counter	0 to 15	0 to 31
N-counter	16 to 4095	32 to 2047
R-counter	3 to 2047	3 to 2047

- Serial control (3-wire bus: data, clock, enable) for fast programming (f_{max} = 10 MHz)
- Switchable polarity and phase detector current programmable
- 1 port output (TTL push-pull)
- External current setting for phase detector output
- Lock detect output with gated pulse (quasi-digital lock detect)
- Operating voltage 2.7 V to 5.5 V
- P-TSSOP-16 package
- Temperature range – 30 °C to 85 °C



Block Diagram

General Description

The PMB 2313, PMB 2314 prescaler family is designed for use in mobile radio communication devices. It is fabricated using Siemens B6HF silicon bipolar process. Due to its low power consumption, low supply voltage down to 2.7 V and low phase noise generation it is suitable for the use in various battery powered handheld systems.

The balanced differential inputs of the IC may be connected either symmetrically or asymmetrically.

Depending on the logic level at SW input the dividing ratio is fixed to 1:64/65 or 1:128/129. The MOD input determines whether modulus 1/n or 1/(n+1) (n=64 or n=128, according to SW level) is active.

The IC can be switched to a low-power standby mode (input STB). The MOD input is TTL/CMOS compatible. The emitter follower output is CMOS compatible.

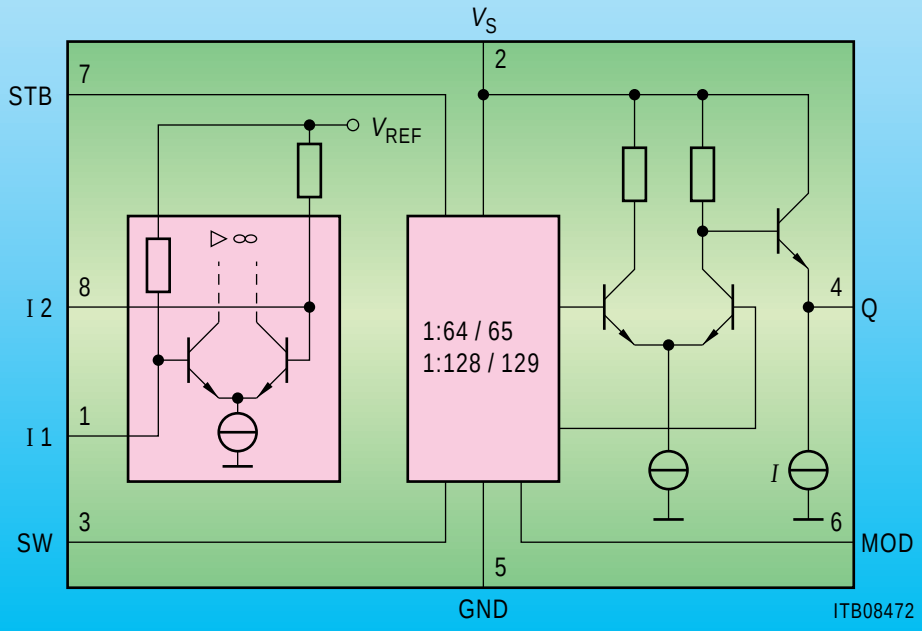
Applications

All analog and digital mobile communication systems as part of RF- and IF synthesizers.

Type	Package
PMB 2313-T	P-DSO-8-1 (SMD)
PMB 2314-T	P-DSO-8-1 (SMD)

Features

- Low operating current
- Power-down mode
- High input sensitivity
- Wide input frequency range
  PMB 2313: 0.1 GHz to 1.1 GHz
  PMB 2314: 0.1 GHz to 2.1 GHz
- Low noise
- Operating voltage 2.7 V to 5.5 V
- P-DSO-8 package
- Temperature range – 30 °C to 85 °C



Block Diagram

General Description

The PMB 2330, PMB 2331 are low power, double balanced up-/downconversion Gilbert cell mixers up to 2.0 GHz. The PMB 2331 is fabricated using Siemens B6HF silicon bipolar process.

Differential signals and symmetrical circuits are used throughout the mixer. The mixer input can be used in balanced or unbalanced configuration. The mixer outputs are high impedance open collector outputs. The adjustable mixer current allows to improve the mixer performance.

An internal bias driver generates supply voltage and temperature compensated reference voltages.

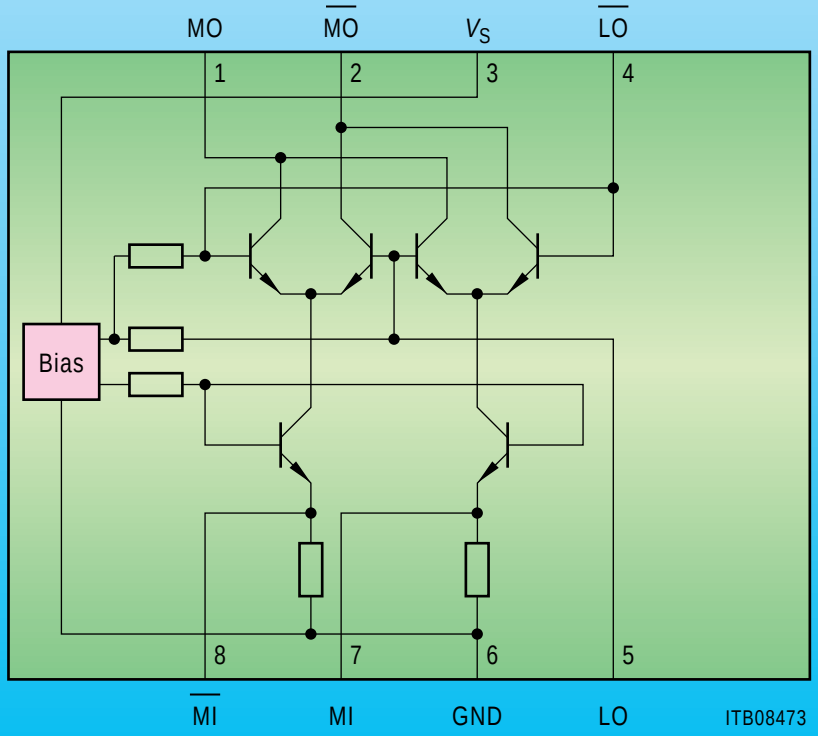
Applications

All analog and digital mobile communication systems as up- / downconverter mixer.

Type	Package
PMB 2330-T	P-DSO-8-1 (SMD)
PMB 2331-T	P-DSO-8-1 (SMD)

Features

- Low operating current
- Low operating voltage:
  PMB 2330: 3.0 V to 7.0 V
  PMB 2331: 2.7 V to 5.5 V
- Power-down mode
- RF- and IF-frequency range up to 2.0 GHz
- Mixer current adjustable
- Low noise figure
- High conversion gain
- Excellent intercept performance
- Good suppression of input signals at output
- High isolation values
- Few external components
- P-DSO-8 package
- Temperature range – 30 °C to 85 °C



Block Diagram

General Description

The PMB 2332 is a low noise amplifier (LNA) up to 1.1 GHz and double balanced mixer up to 3 GHz for use in mobile communication equipment. It is fabricated using Siemens B6HF silicon bipolar process.

The amplified signal is external available for further use at output AO. The DC level at GC allows to switch the LNA gain (on/off: 20 dB).

The mixer is a general purpose up- and downconversion Gilbert cell mixer. Differential signals and symmetrical circuits are used throughout the mixer. The mixer input can be used in balanced or unbalanced configuration. The mixer outputs are high impedance open collector outputs. The adjustable mixer current allows to improve the mixer performance.

An internal bias driver generates supply voltage and temperature compensated reference voltages. The STB pin allows the mixer and bandgap part of the IC to be switched in power-down mode.

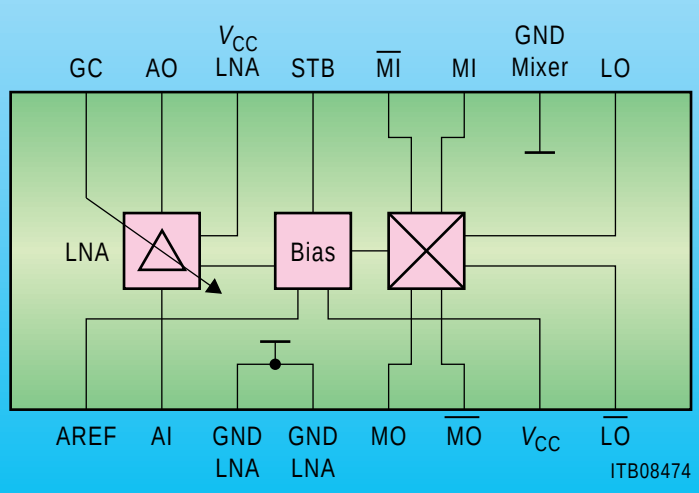
Applications

All analog and digital mobile communication systems as frontend-LNA and up-/ downconverter mixer.

Type	Package
PMB 2332-R	P-TSSOP-16-1 (Shrink, SMD)

Features

- Low operating current
- Power-down mode
- LNA frequency range up to 1.1 GHz
- Switchable LNA gain
- High LNA gain (typ. 20 dB at 900 MHz)
- Low LNA noise figure (typ. 1.5 dB at 900 MHz)
- Double balanced mixer up to 3 GHz with high gain
- Excellent intercept performance
- High isolation values
- Few external components
- Operating voltage 2.7 V to 5.5 V
- P-TSSOP-16 package
- Temperature range – 30 °C to 85 °C



Block Diagram

General Description

The PMB 2333 is a low power amplifier and double balanced mixer up to 3 GHz for use in mobile communication equipment. It is fabricated using Siemens B6HF silicon bipolar process.

The amplifier may be used as low noise amplifier (LNA) or as driver amplifier. The amplified signal is external available for further use at the open collector output AO. The DC level at GC allows to adjust the amplifier current and the gain. Low current is recommended for using the amplifier as LNA, higher current for using it as driver.

The mixer is a general purpose up- and downconversion Gilbert cell mixer. Differential signals and symmetrical circuits are used throughout the mixer. The mixer input can be used in balanced or unbalanced configuration. The mixer outputs are high impedance open collector outputs. The adjustable mixer current allows to improve the mixer performance.

An internal bias driver generates supply voltage and temperature compensated reference voltages. The STB pin allows the mixer and bandgap part of the IC to be switched in power-down mode.

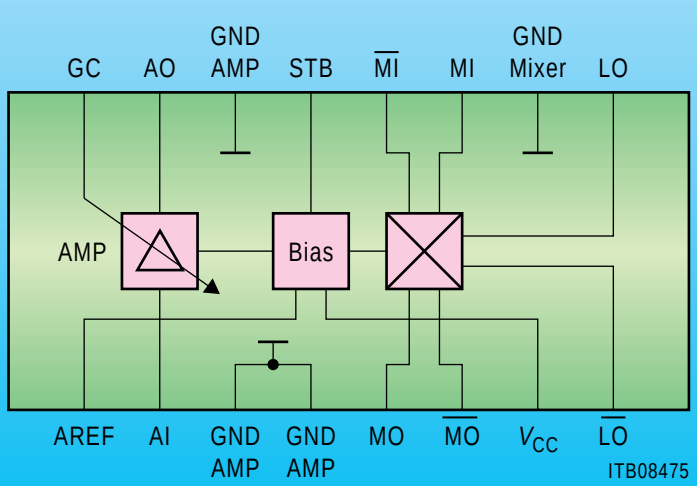
Applications

All analog and digital mobile communication systems as frontend-LNA or preamplifier-driver and up-/downconverter mixer.

Type	Package
PMB 2333-R	P-TSSOP-16-1 (Shrink, SMD)

Features

- Low operating current
- Power-down mode
- Amplifier frequency range up to 3 GHz
- LNA:
  Variable gain,
  High gain (typ. 12 dB at 1.8 GHz),
  Low noise figure (typ. 1.7 dB at 1.8 GHz)
- Driver-amplifier:
  Variable gain,
  High output (typ. +12 dBm at 1.8 GHz)
- Double balanced mixer up to 3 GHz with high gain
- Excellent intercept performance
- High isolation values
- Few external components
- Operating voltage 2.7 V to 5.5 V
- T-SSOP-16 package
- Temperature range – 30 °C to 85 °C



Block Diagram

Digital Terminal ICs

Digital Terminals ICs

Positioning of the described products in different kinds of applications/segments.

Type	Video	Data	Voice	Page
ISAC®-S				
PEB 2085	○	○	•	61
PEB 2086	○	○	•	61
ISAC®-S TE				
PSB 2186	•	•	•	62
ISAC®-P				
PEB 20950			•	63
ISAC®-P TE				
PSB 2196		○	•	64
SmartLink-P				
PSB 2197		○	•	66
ARCOFI®				
PSB 2160	•	○	•	68
ARCOFI®-BA				69
PSB 2161	•	○	•	
ARCOFI®-SP				
PSB 2163	•	○	•	70
PSB 2165			•	71
ITAC®				
PSB 2110		•	•	74
ISAR				
PSB 7110	○	•		73
HSCX-TE				
PSB 21525		•		75
JADE				
PSB 7280	•	•	•	76

• = Main application

○ = Optional

Depending on the application products out of other segments
like ESCC2; IBC; IEC-Q should also be considered.

Overview on ICs for Digital Terminals

ISDN Voice Terminals

With the digitization of the local loops, new ICs are needed to adapt the voice and data sources.

Because of the analog/digital conversion is implemented in the telephone, Digital Signal Processing techniques (DSP) are suitably powerful tools for accomplishing this task. The ARCOFI® PSB 2160, ARCOFI®-BA PSB 2161 and ARCOFI®-SP PSB 2165 or PSB 2163 make the best use of this technology to deliver programmable, telephone specific codec/filter.

The modular concept allows the support of several interfaces like U_{P0} (ISAC®-P), U_{PN} (ISAC®-P TE, SmartLink-P), S_0 (ISAC®-S, ISAC®-S TE) and U_{k0} (IEC-Q, IEC-T). All interface controllers including layer-1, -2 support the IOM-2 Bus and are software compatible.

The adaptation of existing data terminals (DTE) to an ISDN through a variety of interfaces (X.21, V24, RS232C, …) is a subject being covered by a number of emerging standards.

The ITAC ISDN adapter circuit PSB 2110 brings a flexible solution to each configuration.

A typical subscriber terminal configuration is shown in the **figure 1**.

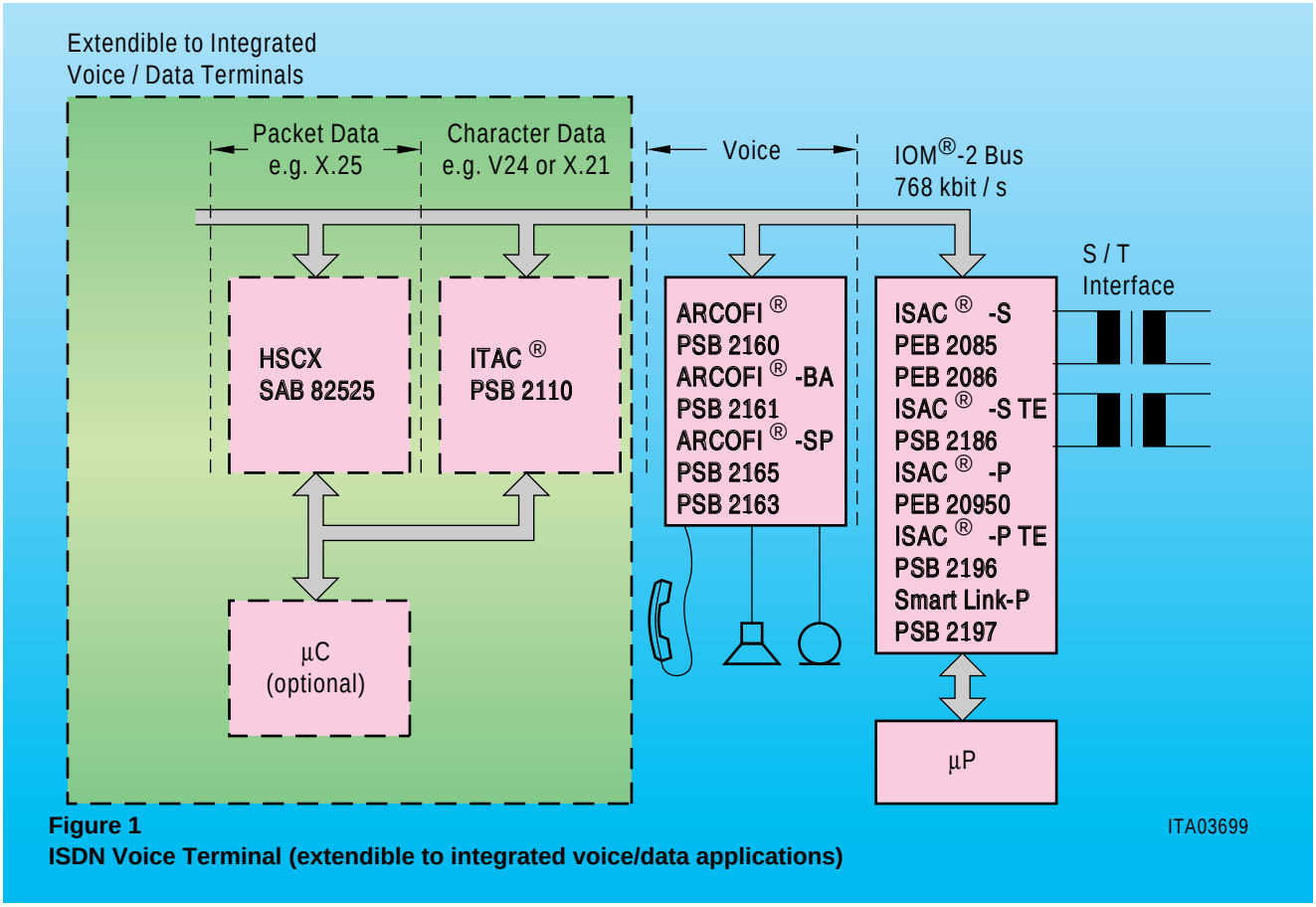


Figure 1
ISDN Voice Terminal (extendible to integrated voice/data applications)

Overview on ICs for Digital Terminals

ISDN Data Access

Shorter dial-up times, higher data rates and simultaneous voice/data transmission comparing to analog transfer via modem make ISDN very interesting for data access.

Especially ISDN data transfer via PC card is becoming more and more popular.

The signs below show 2 solutions of passive PC cards.

The passive low cost version **(figure 2)** is optimal for point-to-point data transfer. The modular concept for this version includes the HDLC controllers and the interface controllers (optional for U_{P0}-, U_{PN}-, S_0-, U_{k0}-interfaces → see ISDN Voice Terminals). The serial controllers HSCX (8-bit interface) and ESCC2 (16-bit interface) can be used in many applications in telecom and datacom systems by offering dual channel HDLC controlling and DMA capability.

The shown enhanced passive PC-card version **(figure 3)** includes the interface controllers and a DSP-based solution. There is a dedicated ROM-coded DSP-version for supporting modem (V.32), fax (V.29), data adaption (V.110, USART framing) and HDLC controlling in development. Please contact the Siemens sales office for details.

Like the ISDN Voice Terminals **(figure 1)** both PC-card version are expendible for voice and active PC-card solutions.

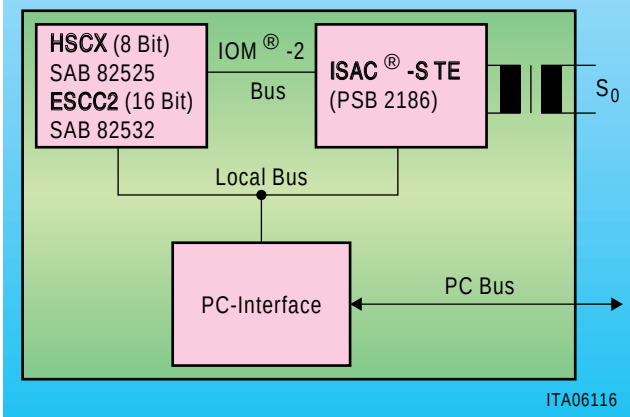


Figure 2
Passive Low-Cost PC-Card Solution

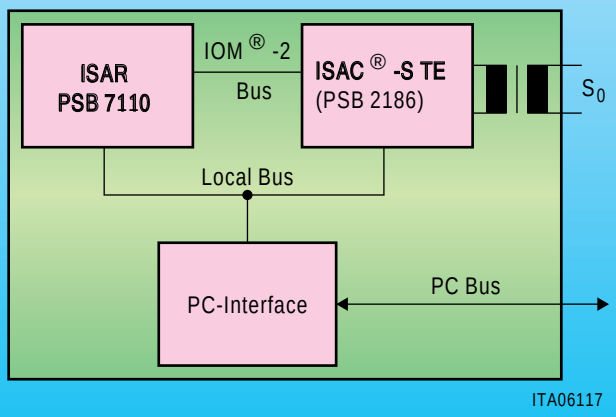


Figure 3
Enhanced Passive PC-Card Solution Optimized ROM-Coded DSP-Solution (in development)

ISDN Video Terminals

Together with the video compression IC (VCP) from 8x8, Siemens offers a system solution for H.320 ISDN-based video communication. This four chip solution includes the VCP ARCOFI-SP (PSB 2165) **J**oint **A**udio **D**ecoder-**E**ncoder JADE (PSB 7280)
ISAC-S (PSB 2186).

The 8×8 VCP is a single-chip programmable video processor, which support the standards H.261, MPEG1, MPEG2 IPEG.

The Siemens audio compression IC JADE supports the following standards: G.711, G.722, G.728.

The **figure 4** shows the 8×8-Siemens videophone solution.

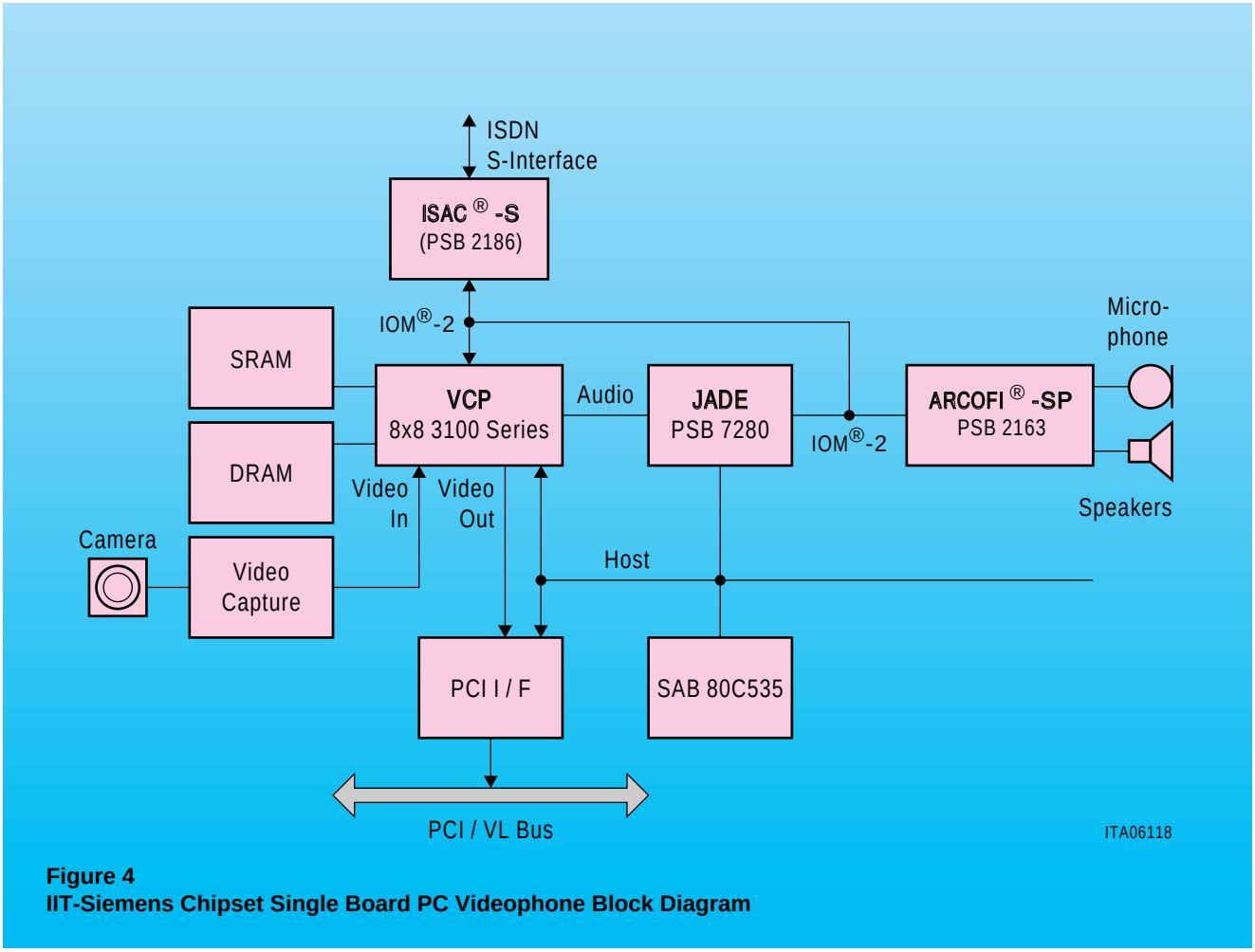


Figure 4
IIT-Siemens Chipset Single Board PC Videophone Block Diagram

Digital Terminal ICs

Product Overview

Type	Short Title	Description	Page
PEB 2085	ISAC®-S	ISDN Subscriber Access Controller	61
PEB 2086	ISAC®-S	ISDN Subscriber Access Controller	61
PSB 2186	ISAC®-S TE	ISDN Subscriber Access Controller	62
PEB 20950	ISAC®-P	ISDN Subscriber Access Controller	63
PSB 2196	ISAC®-P TE	ISDN Subscriber Access Controller	64
PSB 2197	SmartLink-P	Subscriber Access Controller	66
PSB 2160	ARCOFI®	Audio Ringing Codec Filter	68
PSB 2161	ARCOFI®-BA	Audio Ringing Codec Filter	69
PSB 2163	ARCOFI®-SP	Audio Ringing Codec Filter	70
PSB 2165	ARCOFI®-SP	Audio Ringing Codec Filter	71
PSB 7110	ISAR	ISDN Subscriber Access	73
PSB 2110	ITAC®	ISDN Terminal Adapter Circuit	74
PSB 21525	HSCX-TE	High-Level Serial Communication Controller Extended	75
PSB 7280	JADE	Joint Audio Decoder / Encoder	76

General Description

The PEB 2085/86 ISAC-S implements the four-wire S_0 interface used to link voice/data terminals to an ISDN. The component switches B- and D-channels between the S_0 and the ISDN Oriented Modular (IOM) interfaces, the latter being a standard backplane interface for the ISDN basic access. The HDLC packets of the ISDN D-channel are handled by the ISAC-S which interfaces them to the associated microcontroller.

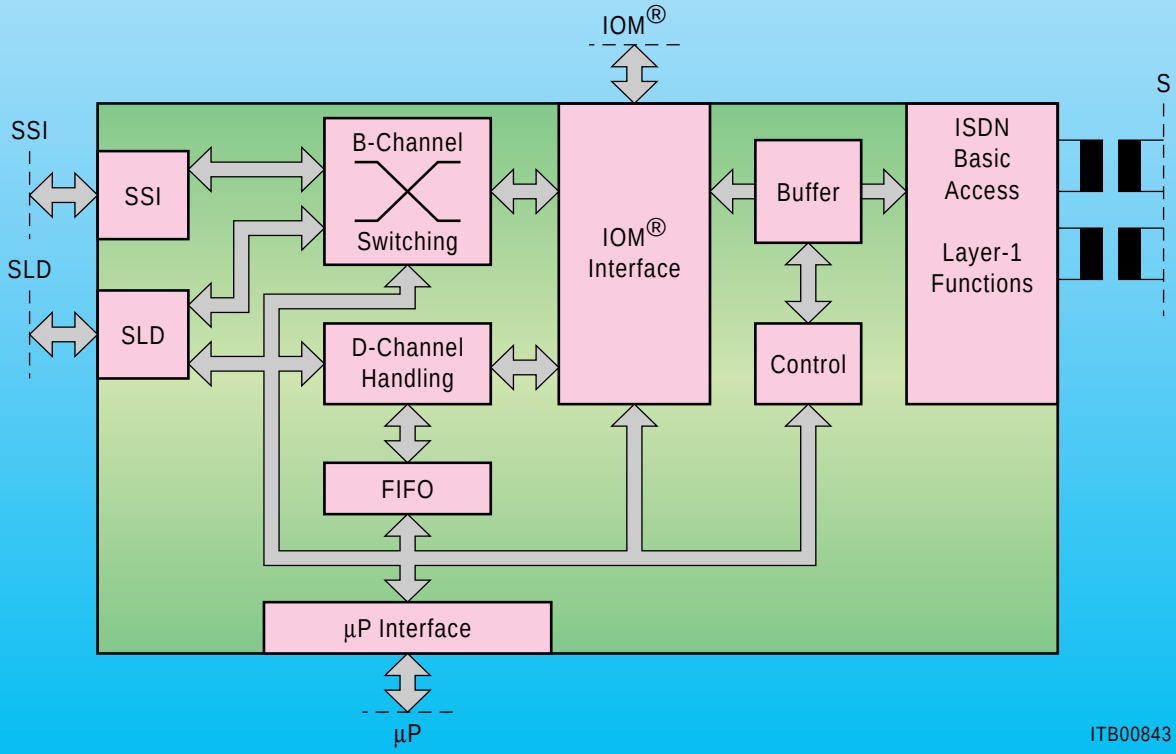
Applications

- Voice/Data Terminals
- ISDN PC Cards/Terminal Adapters
- Videophone
- Video PC Cards/Conferencing Systems
- G4 FAX
- Tele Control Systems
- Point-of-Sales Terminal

Type	Package
PEB 2085-N	P-LCC-44-1 (SMD)
PEB 2085-P	P-DIP-40-2
PEB 2086-H	P-MQFP-64-1 (SMD)
PEB 2086-N	P-LCC-44-1 (SMD)

Features

- Full duplex 2B+D S_0 interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T interface and IOM
- Receive timing recovery according to selected operating mode
- D-channel access control; support of LAPD protocol
- FIFO-buffer (2 × 64 bytes) for efficient transfer of D-channel packets
- 8-bit microprocessor interface, multiplexed or non-multiplexed
- Serial interface: IOM-1, SLD, SSI, IOM-2
- Implementation of IOM-1/IOM-2-MONITOR and C/I-channel protocol to control peripheral devices
- Watchdog timer



Block Diagram

General Description

The PSB 2186 ISAC-S TE implements the four-wire S_0 interface used to link voice/data terminals to an ISDN. The component switches B- and D-channels between the S_0 and the ISDN Oriented Modular (IOM-2) interfaces, the latter being a standard backplane interface for the ISDN basic access. The HDLC packets of the ISDN D-channel are handled by the ISAC-S TE which interfaces them to the associated microcontroller.

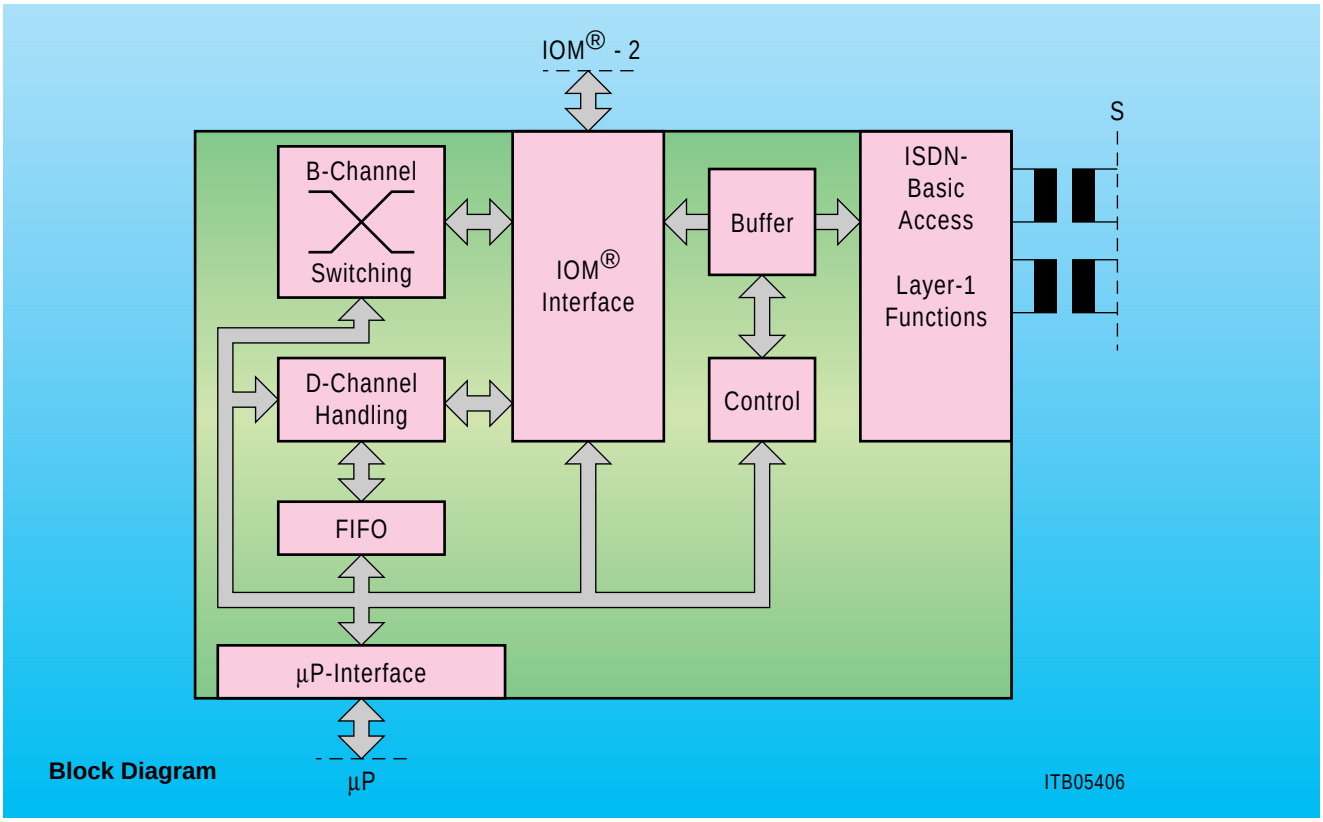
Applications

- Voice/Data Terminals
- ISDN PC Cards/Terminal Adapters
- Videophone
- Video PC Cards/Conferencing Systems
- G4 FAX
- Tele Control Systems
- Cash Register Internetworks
- Point-of-sales terminals

Type	Package
PSB 2186-H	P-MQFP-64-1 (SMD)
PSB 2186-N	P-LCC-44-1 (SMD)
PSB 2186-P	P-DIP-40-2

Features

- IOM-2 terminal specific version of the PEB 2086 (downward pin and SW compatibility)
- Full duplex 2B+D S_0-interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T interface and IOM-2
- D-channel access control; support of LAPD control
- FIFO buffer (2×64 bytes) for efficient transfer of D-channel packets
- 8-bit microprocessor interface, multiplexed or non-multiplexed
- Serial interface: IOM-2 interface including bit clock and strobe signal
- Implementation of IOM-2 MONITOR and C/I-channel protocol to control peripheral devices



Block Diagram

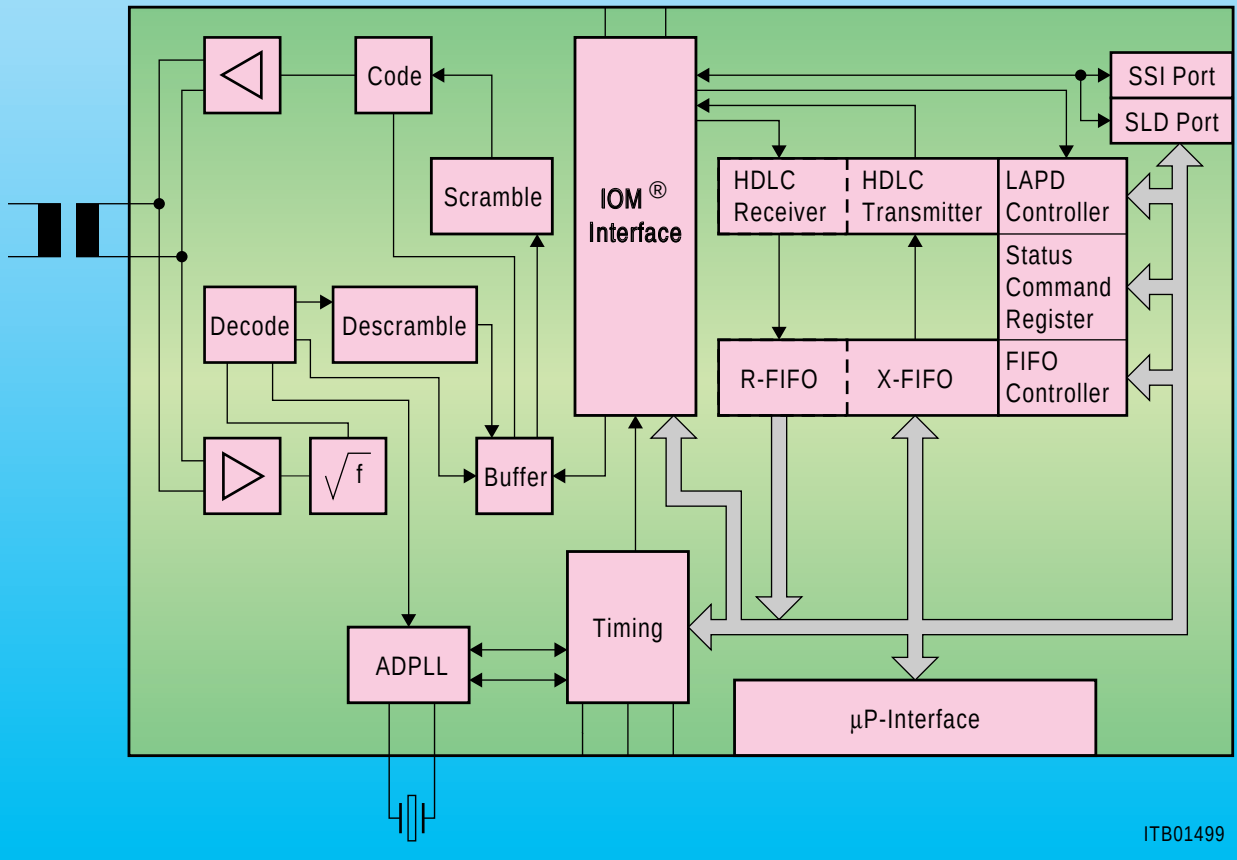
General Description

The ISAC-P PEB 20950 is a combination of transceiver and HDLC controller for ISDN terminals in a two-wire PBX environment. Transceiver functions are performed according to the two-wire PBX industry standard U_{P0}. This corresponds to all of the functions available on the IBC PEB 2095. Similarly the HDLC protocol is processed as described for the ICC PEB 2070. The ISAC-P represents both the IBC and ICC on a single IC.

Type	Package
PEB 20950-N	P-LCC-44-1 (SMD)
PEB 20950-P	P-DIP-40-2

Features

- Half-duplex burst-mode two-wire transceiver
- AMI-line code
- Adaptive line equalization
- High-level support of LAPD protocol
- FIFO-buffer (2 × 64 bytes) for efficient transfer of D-channel packets
- IOM interface to other ICs
- Switching of test loops
- 8-bit µP interface
- Advanced CMOS technology
- Low power consumption



Block Diagram

General Description

The PSB 2196, ISDN Subscriber Access Controller for U_{PN} interface ISAC-P TE, implements the subscriber access functions for a digital terminal to be connected to a two-wire U_{PN} interface.

The PSB 2196 ISAC-P TE is an optimized device for TE-applications, covering the complete layer-1 and -2 functions.

The PSB 2196 ISAC-P TE combines the functions of the U_{PN} transceiver with reduced loop length (one channel of the OCTAT-P PEB 2096) and the ISDN-Communications Controller (ICC, PEB 2070) onto one chip.

The microcontroller interface of the ISAC-P TE is compatible to standard multiplexed microcontrollers. In addition it provides the microcontroller clock signal as well as a supply voltage control and reset generation.

The terminal repeater function of the ISAC-P TE allows to cascade two telephones which are controlled by one U_{PN} interface from the line card.

The PSB 2196 ISAC-P TE interfaces to voice/data devices via the IOM-2 interface.

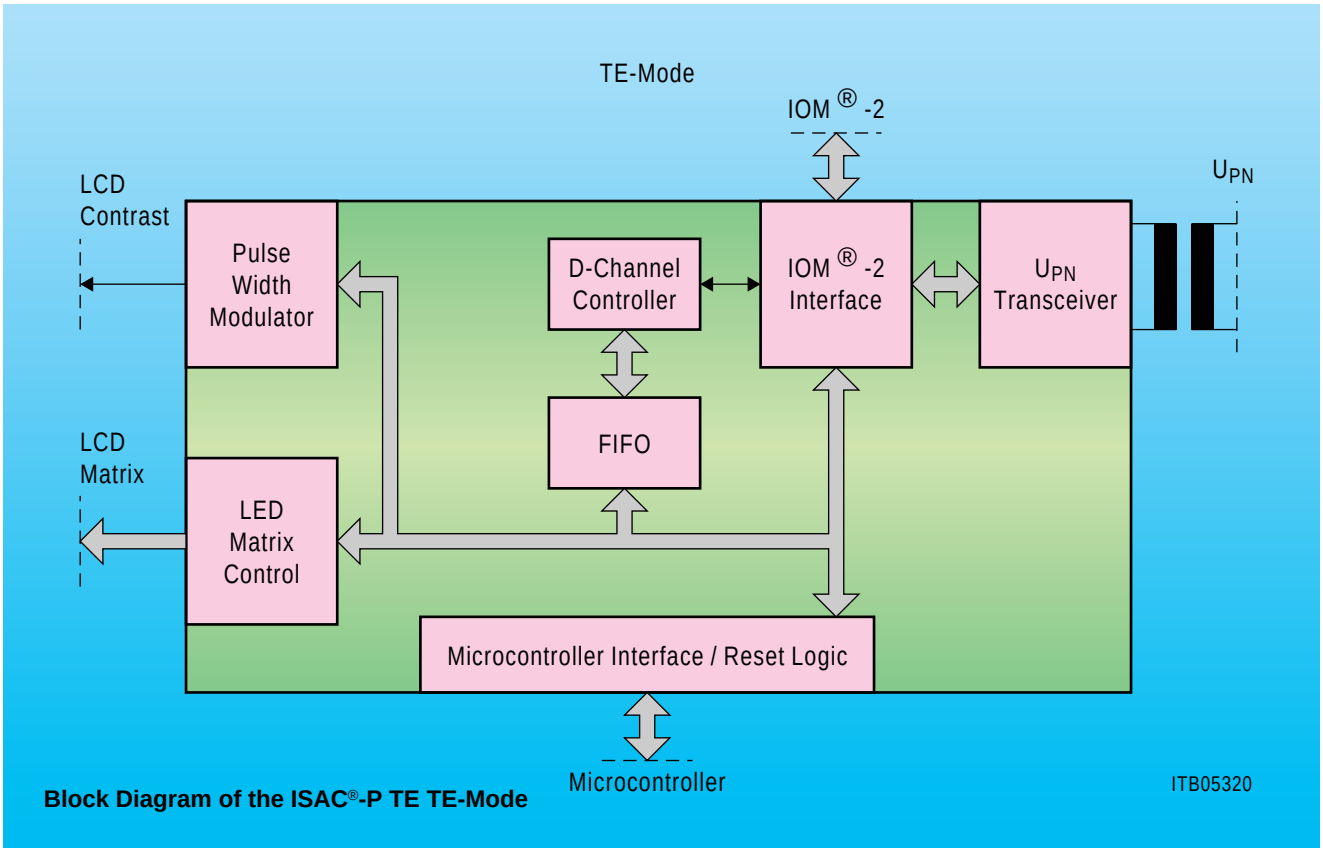
The PSB 2196 ISAC-P TE is a 1 micron CMOS device offered in a P-LCC-44 and P-MQFP-44 pin package. It operates from a single 5-V supply.

Note: U_{PN} in the document refers to a version of the U_{P0} standard with a reduced loop length.

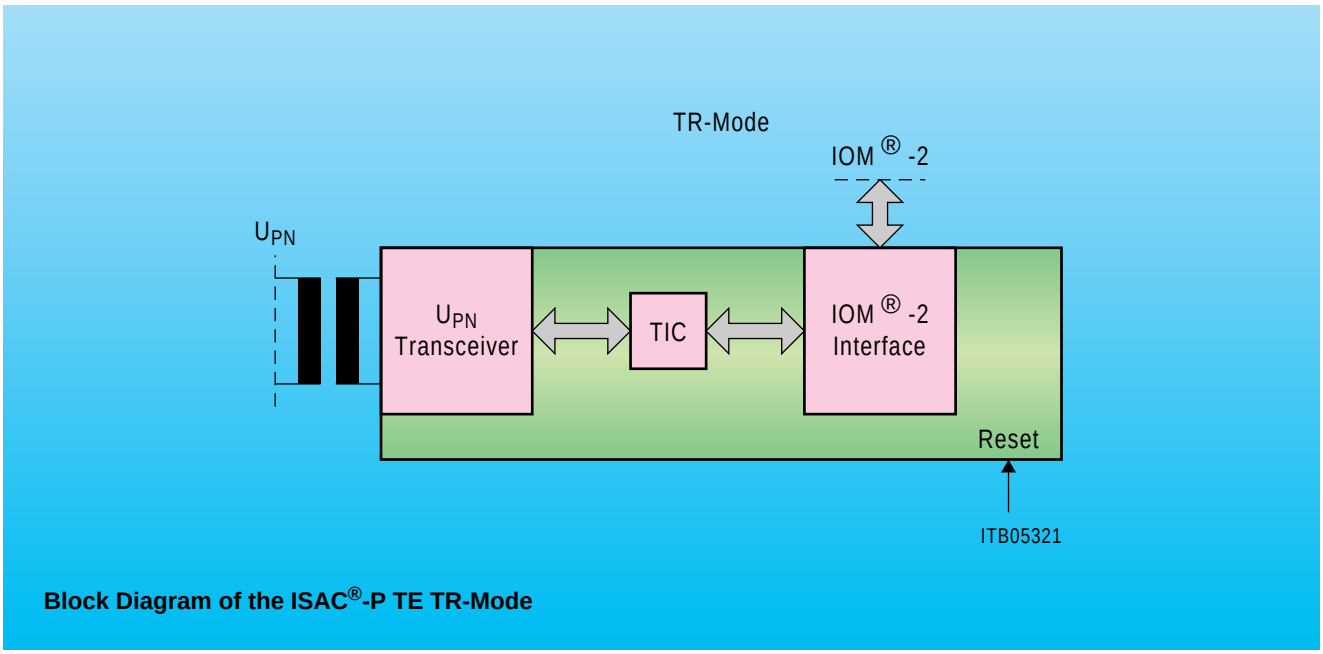
Type	Package
PSB 2196-H	P-MQFP-44-2 (SMD)
PSB 2196-N	P-LCC-44-1 (SMD)

Features

- Cost/performance-optimized U_{PN}-interface transceiver, compatible to PEB 2096 OCTAT-P
- HDLC controller with 2×32-byte FIFO per direction
- HDLC-address recognition and control field handling compatible to PEB 2070
- IOM-2 interface for terminal application compatible to PEB 2070 ICC
- 8-bit multiplexed microprocessor interface
- 4-wire serial programming interface
- CPU clock and reset outputs
- Test loops
- Advanced CMOS technology



Block Diagram of the ISAC®-P TE TE-Mode



Block Diagram of the ISAC®-P TE TR-Mode

General Description

The PSB 2197, SmartLink-P, implements the subscriber access functions for a digital terminal to be connected to a two-wire U_{PN} interface.

The PSB 2197 SmartLink-P is an optimized device for TE applications, covering the complete layer-1 and basic layer-2 functions for digital terminals.

The PSB 2197 SmartLink-P combines the functions of the U_{PN} transceiver with reduced loop length (one channel of the OCTAT-P PEB 2096) and a simple HDLC controller for signaling data onto one chip.

A pulse width modulator is included to provide an LCD-contrast control or a ring tone signal.

The serial control port of the SmartLink-P is compatible to most serial interfaces of microcontrollers. In addition it provides the microcontroller clock signal as well as an undervoltage detector and reset generation including a watchdog function.

The Terminal Repeater function of the SmartLink-P allows to cascade two telephones which are controlled by one U_{PN} interface from the line card or to extend the loop length by using an IEC-Q transceiver.

The SmartLink-P can also be used as a simple HDLC controller which provides the TIC-bus access procedure. In this mode, the U_{PN} transceiver is inactive.

The PSB 2197 SmartLink-P interfaces to voice/data devices via the IOM-2 interface and provides an additional bit clock and strobe signal for standard codecs. The upstream B-channel information may be muted or loop back the downstream data.

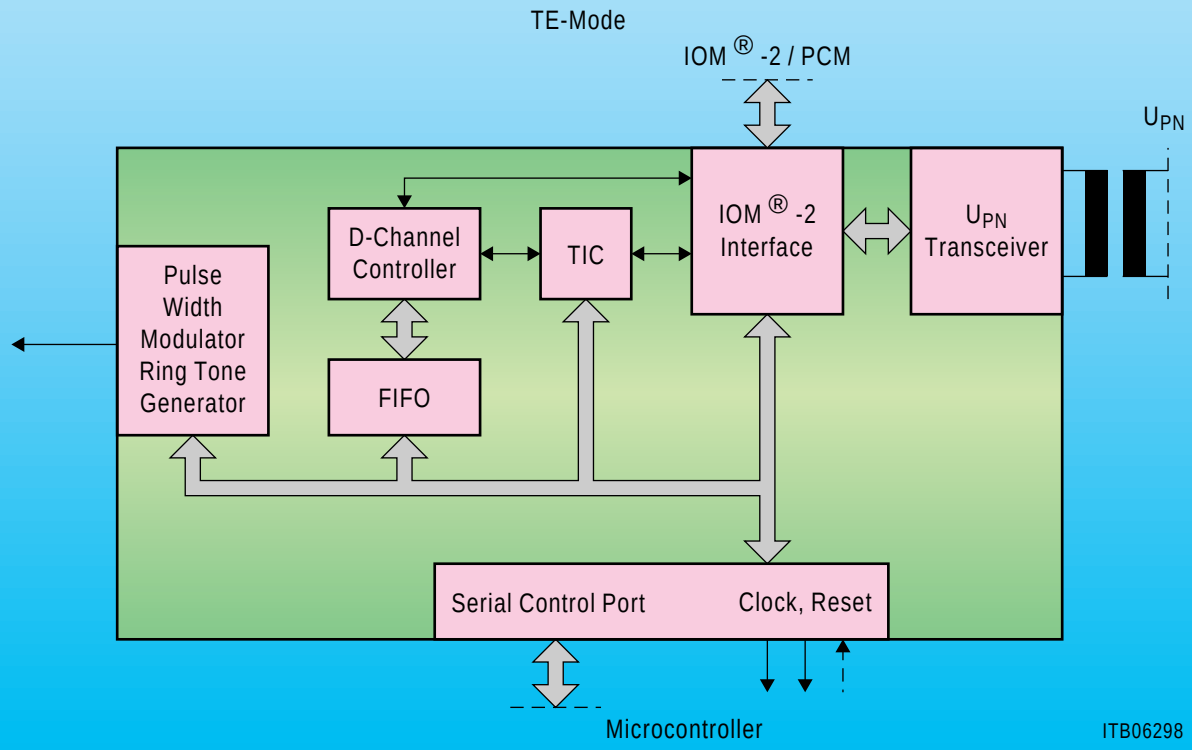
The PSB 2197 SmartLink-P is a 1-micron CMOS device offered in a P-DSO-28 package. It operates from a single 5-V supply.

Note: U_{PN} in the document refers to a version of the U_{P0} standard with a reduced loop length.

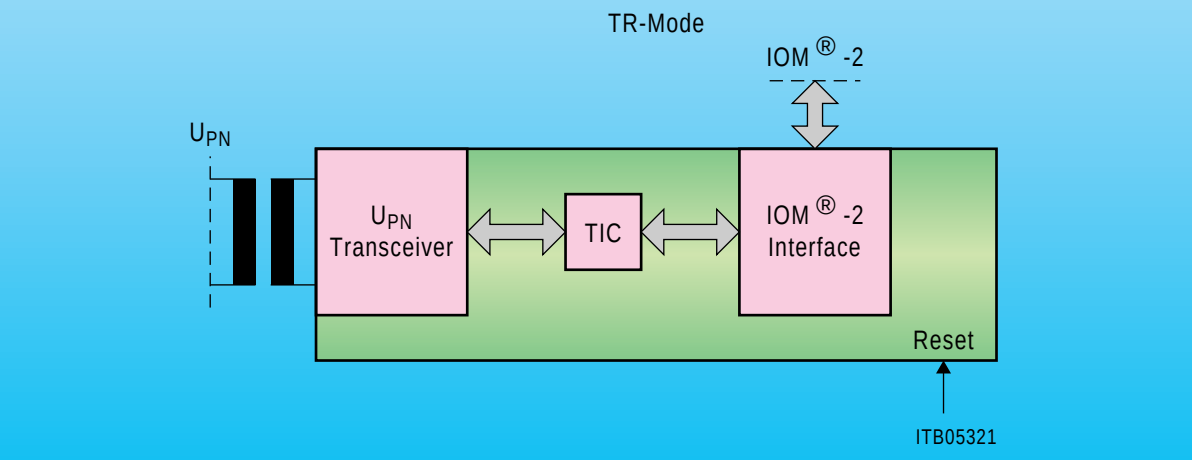
Type	Package
PSB 2197-T	P-DSO-28-1 (SMD)

Features

- Cost/performance-optimized U_{PN} interface tranceiver, compatible to PEB 2096 OCTAT-P or PSB 2196 ISAC-P TE
- HDLC controller with 2 × 4-byte FIFO per direction
- IOM-2 interface for terminal application including bit clock and strobe signal
- Uplink MUTE function
- Selective B-channel loop back
- Serial control port
- Pulse width output LCD-contrast control or ring tone generation
- CPU clock and reset output
- Watchdog timer
- Test loops
- Advanced CMOS technology
- Low power consumption: active: 100 mW max.



Block Diagram of the SmartLink-P TE-Mode



Block Diagram of the SmartLink-P TR-Mode

General Description

The PSB 2160 ARCOFI provides the subscriber with an optimized audio, ringing, codec, filter processor solution for a digital telephone. It fulfills all the necessary requirements for the completion of a low-cost digital telephone.

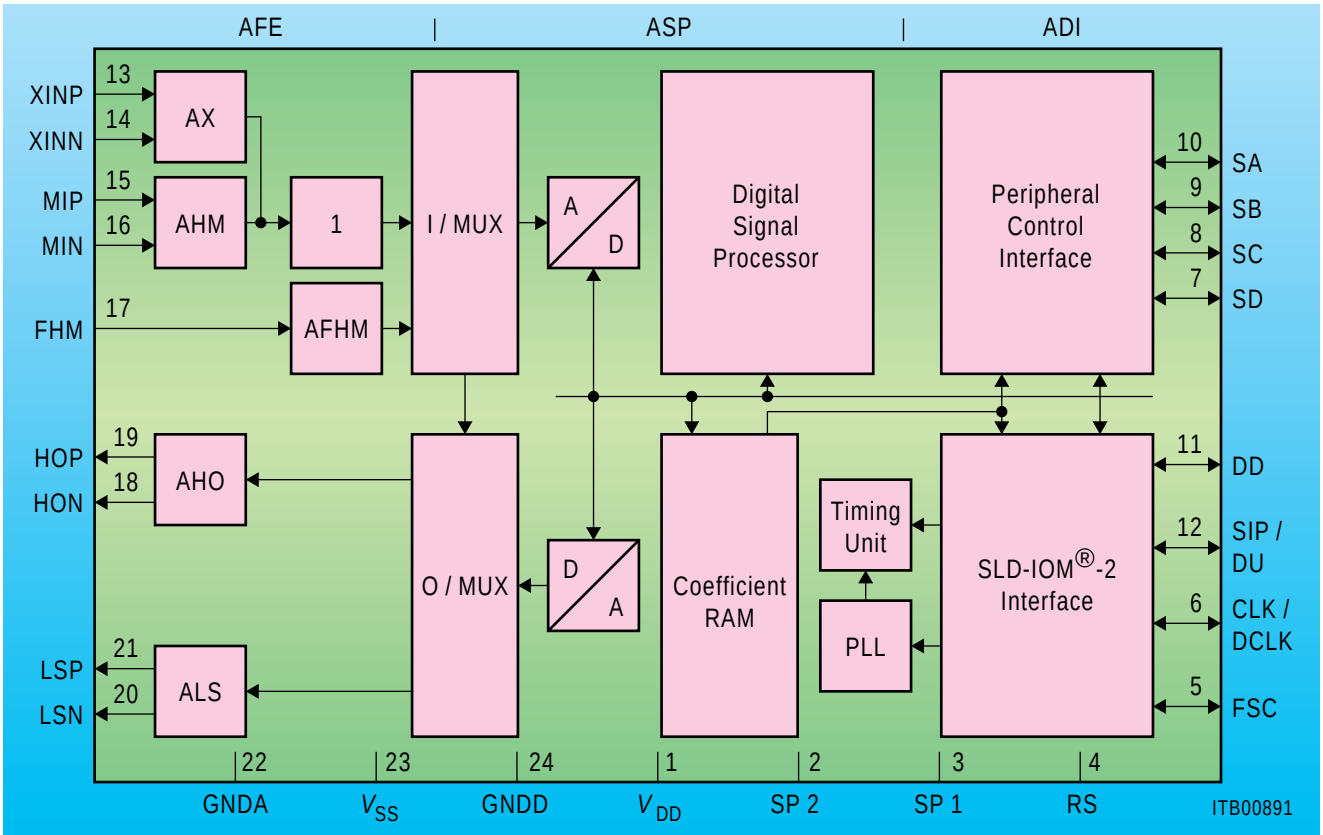
Applications

- Voice Terminals and Voice/Data Terminals
- Telephones with PC Interface
- Voice featured PC Cards
- Fax Machines and a/b Terminal Adapter

Type	Package
PSB 2160-N	P-LCC-28-1 (SMD)
PSB 2160-P	P-DIP-24-1

Features

- Applications in digital terminal equipment including a voice path
- Digital signal processing (DSP) performs all CODEC functions
- Fully compatible to the G.714/CCITT specifications
- PCM G.711/CCITT A-Law/µ-Law and 16-bit linear data
- IOM-2 or SLD serial interface bus
- DTMF, tone and ringing generators
- Separate output for a piezo ringer
- Dual analog inputs for handset and “hands-free” microphones plus an auxiliary differential analog input
- Two sets of differential outputs for a handset earpiece and a loudspeaker
- 100 mW (sine wave) loadspeaker driver capability
- Test and maintenance loopbacks in the analog front end and the digital processor
- Low power CMOS technology
- Power consumption active: 150 mW
  standby: 100 mW



Block Diagram

General Description

The PSB 2161 ARCOFI-BA provides the Design Engineer with a cost-optimized audio, ringing, codec, filter processor solution for simple digital terminals. It offers the minimum functions necessary to develop a low-cost telephone and thus with the high flexibility by the DSP technics.

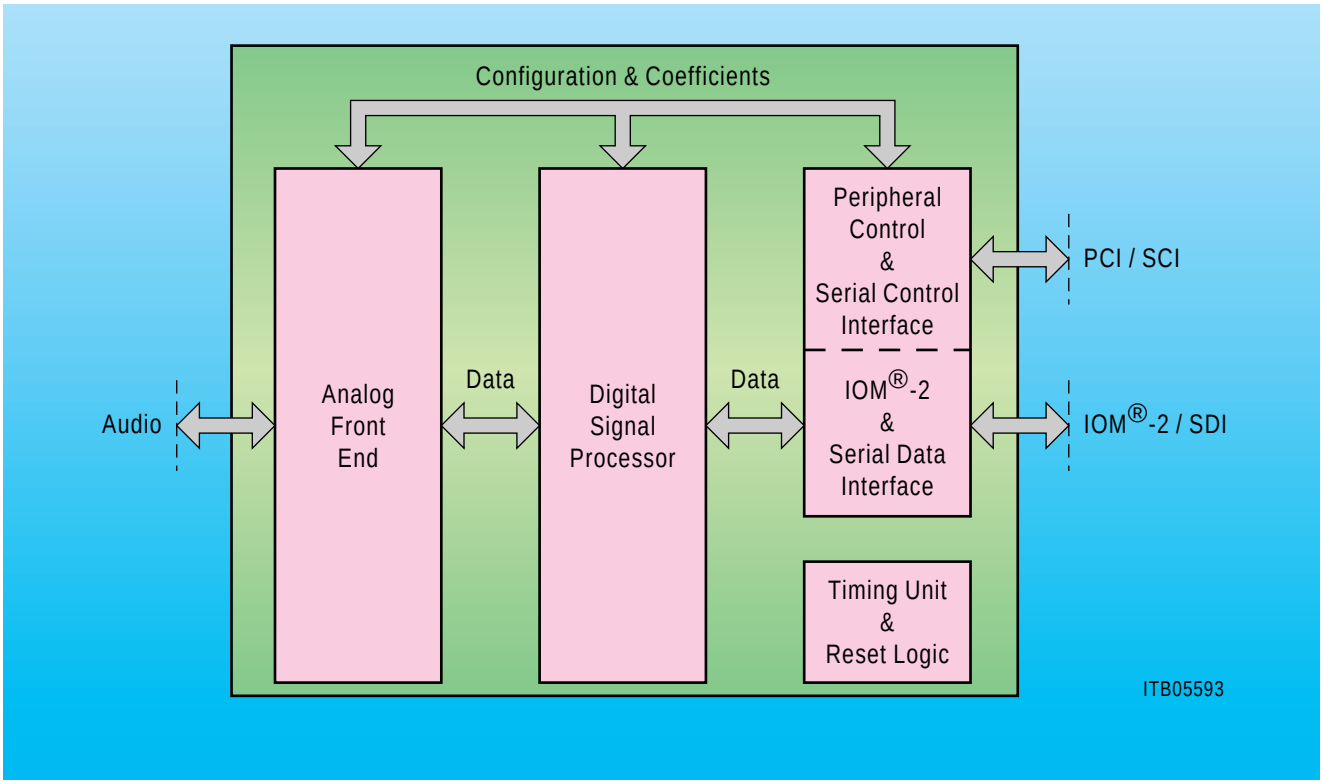
Applications

- Low-Cost Voice Terminals and Voice/Data Terminals
- Telephones with PC Interface
- Voice featured PC Cards
- Video Conference Terminals
- Fax Machines and a/b Terminal Adapter

Type	Package
PSB 2161	P-DSO-28-1 (SMD)

Features

- Programmable Analog Front End (AFE), enables direct connection of microphones, earpiece and loudspeaker
- Digital signal processing performs all CODEC functions
- Fully compatible to the G. 714 CCITT and ETSI (NET33) specification
- PCM A-Law/µ-Law (G. 711 CCITT) and 16-bit linear data
- IOM-2 interface (TE- and non-TE-mode), Serial Control Interface (SCI) and Serial Data Interface (SDI)
- Three analog inputs: two differential, high performance inputs for microphones plus a single-ended auxiliary input
- Two differential outputs for a handset earpiece (200 Ω) and a loudspeaker (50 Ω)
- 100-mW sine wave and 200-mW square wave loadspeaker driver capability
- Separate digital output for a piezo ringer
- Flexible Peripheral Control Interface (PCI) in IOM-2 TE-mode
- Flexible DTMF, tone and ringing generator
- Single 5-V power supply
- Low power consumption: standby < 1 mW



General Description

The PSB 2163 ARCOFI-SP provides the subscriber with an DSP-based audio, ringing, codec, filter-processor solution for a digital telephone. It fulfills all the necessary requirements for the completion of a low-cost digital telephone featuring digital speakerphone and controlled loudhearing.

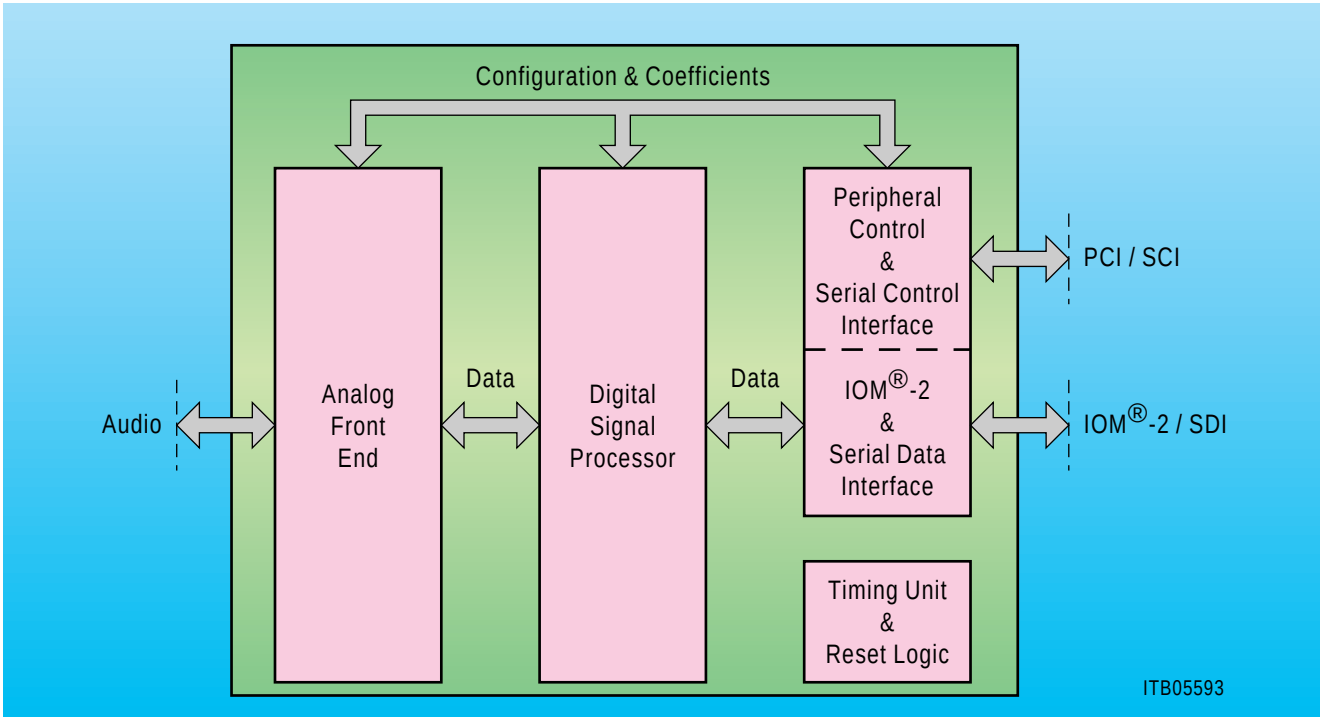
Applications

- Voice Terminals and Voice/Data Terminals
- Telephones with PC Interface
- Voice Featured PC Cards
- Video Conference Terminals
- Fax Machines and a/b Terminal Adapter

Type	Package
PSB 2163-N	P-LCC-28-1 (SMD)
PSB 2163-P	P-DIP-28-1
PSB 2163-T	P-DSO-28-1 (SMD)

Features

- Programmable Analog Front End (AFE), enables direct connection of microphones, earpiece and loudspeaker
- 42+3 dB transmit amplification on chip, allows the direct connection of the speakerphone microphone without external OpAmp
- Digital signal processing performs all CODEC functions Fully compatible to the G.714/CCITT and NET33/ETSI specifications
- PCM G.711/CCITT A-Law/µ-Law and 16-bit linear data
- IOM-2 TE, IOM-2 (4 MHz) and SCI/SDI serial data interfaces
- Enhanced digital speakerphone support without any external devices:
  “Stronger-Wins” Algorithm enables mode switching by just speaking louder
  Controlled monitoring (loudhearing) without any external devices
  Automatic Gain-Control (AGC) in transmit and receive direction
- 200 mW (square) / 100 mW (sine wave) loudspeaker driver capability
- Flexible DTMF, tone and ringing generator
- Low power consumption (standby < 1 mW)



Block Diagram

General Description

The PSB 2165 ARCOFI-SP provides the subscriber with an optimized Audio, Ringing, Codec, Filter processor solution for a digital telephone. It fulfills all the necessary requirements for the completion of a low-cost digital telephone.

The ARCOFI-SP performs all coding, decoding and filtering functions according to the CCITT and AT&T standard.

Full featured applications are possible without any external elements. All the necessary hardware and software is implemented. In addition, the ARCOFI-SP offers a speakerphone function as well as a controlled monitoring. These features are fully implemented in the chip. Two independent receive channels offer a more flexible use of the tone generator, the digital gain stages, and the frequency correction.

Two transducer correction filters (one for each direction) can be programmed to correct the analog transducer frequency characteristics.

The ARCOFI-SP provides an universal DTMF, tone and ringing generator. All the generated tone sequences are switchable to each output. This flexible tone generator concept fulfills all the current specifications.

The interfacing to a handset mouth and earpiece is facilitated by a flexible analog front end. A loudspeaker output has also been integrated on the chip as well as a secondary input for a speakerphone microphone. Further auxiliary differential analog input is available. All analog inputs and outputs are gain programmable through software.

Functional Description

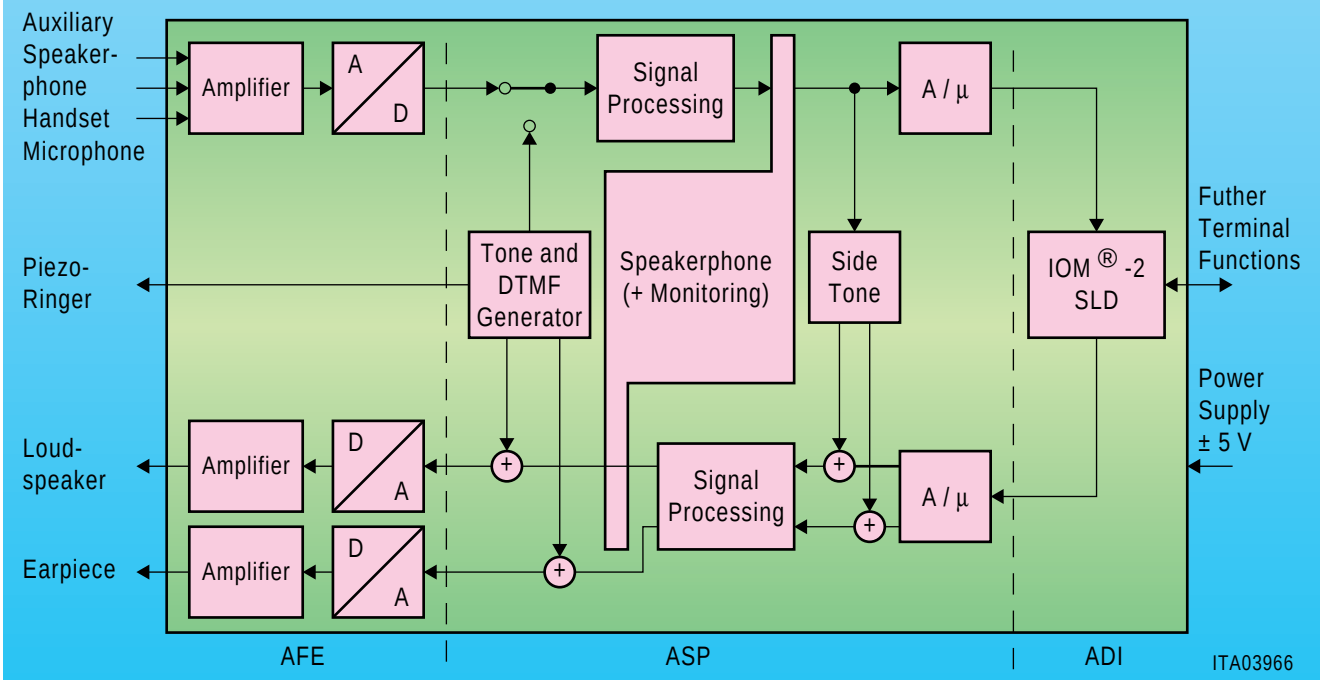
The ARCOFI-SP bridges the gap between the audio world of microphones, earphones, loudspeakers and the PCM digital world by providing a full PCM-CODEC with all the necessary transmit and receive filters as well as a speakerphone and monitoring function.

The ARCOFI-SP can be subdivided in three main blocks:
- The ARCOFI Analog Front End (AFE)
- The ARCOFI Signal Processor(ASP)
- The ARCOFI Digital Interface (ADI).

Type	Package
PSB 2165-N	P-LCC-28-1 (SMD)
PSB 2165-P	P-DIP-28-1

Features

- Applications in digital terminal equipment featuring voice functions
- Digital signal processing performs all CODEC functions
- Fully compatible to the G.714 CCITT specifications
- PCM A-Law/μ-Law and 16-bit linear data
- IOM-2 or SLD serial data interface
- Full digital speakerphone support without any external devices
- Automatic Gain Control (AGC) in transmit direction
- Controlled monitoring (loudhearing) without any external devices
- Dual analog input for the microphone in the handset and single-ended input the speakerphone plus an auxiliary differential analog input
- Two differential outputs for a handset earpiece and a loudspeaker
- 100-mW (sine wave) loudspeaker driver capability
- Independent gain programmable amplifiers for all analog inputs and outputs
- Flexible Peripheral Control Interface (PCI)
- Flexible test and maintenance loopbacks in the analog front end and the digital signal processor
- Flexible DTMF, tone and ringing generator
- Low power consumption (standby < 1 mW)
- Advanced CMOS technology, single 5-V power supply Hardware and software support by the Siemens ISDN PC Board SIPB 5000 and ARCOFI-SP coefficient program ARCOS SP Plus SIPO 2165



Signal Flow Diagram

General Description

The PSB 7110 ISAR has been designed as advanced solution for passive ISDN PC cards and stand alone terminal adapter boxes. It is an ISDN-data access controller, which supports data rate adaption, standard HDLC protocolling and communication with remote analog fax or modem applications.

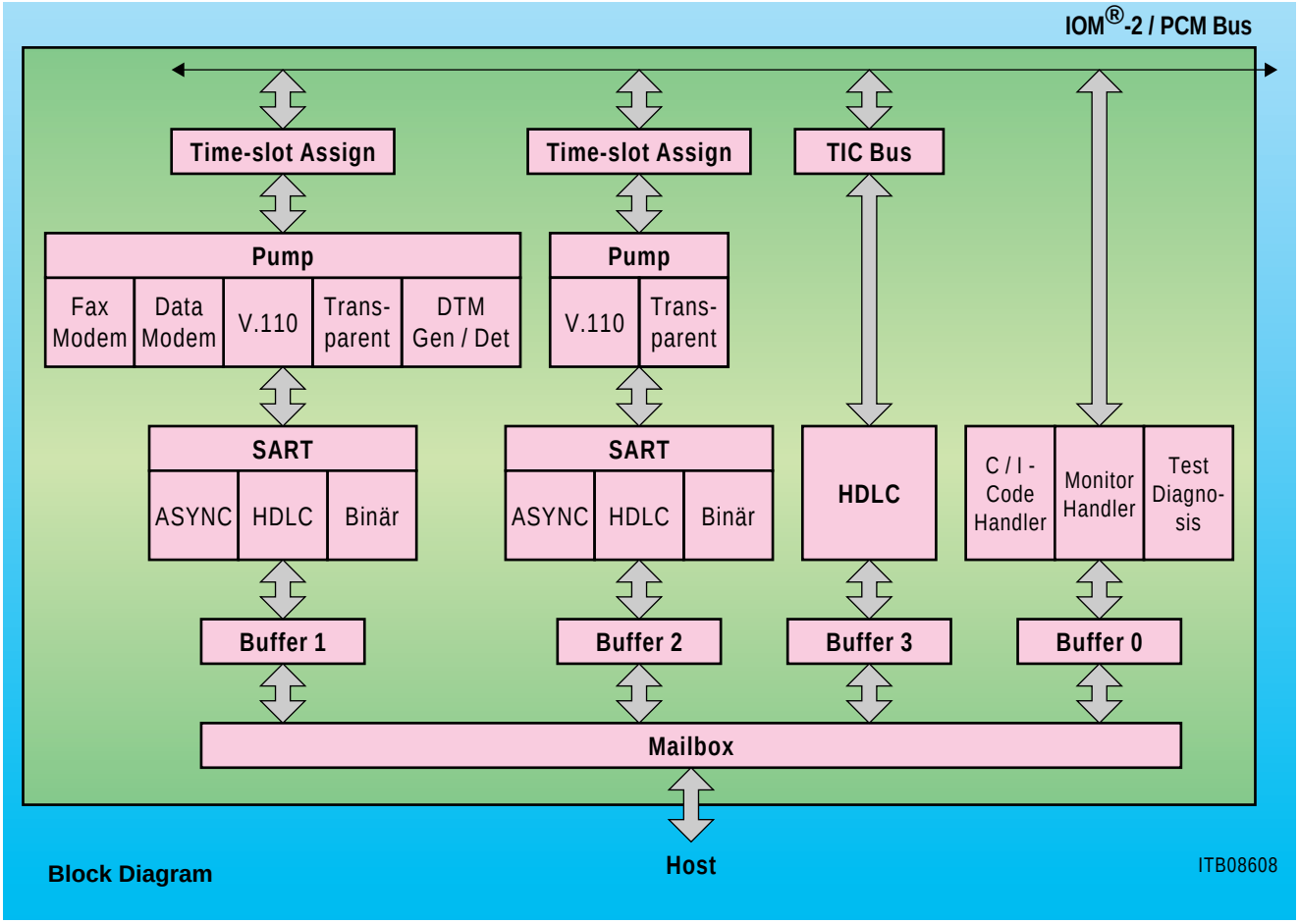
Applications

- ISDN PC Card /Standalone Box
- ISDN Data Terminals
- Modem
- Radio in the Loop
- Digital Terminal Manufacturers
- Computer Manufacturers
- Modem Producers

Type	Package
PSB 7110-F	P-TQFP-100-1 (SMD)

Features

- Two universal formatter supporting async, HDLC and binary framing of B-channel data
- One HDLC formatter with TIC-bus support for D-channel applications in terminal mode
- Fax/modem modulation up to 14.4 kbaud (V.32bis, V.17) including fall back modes
- DTMF generation / reception
- 8 Kbyte on-chip RAM for internal use and HDLC-frame buffering
- 256-byte FIFO per direction for host interface communication
- 8 Kbyte external SRAM interface for V.32bis support



Block Diagram

General Device Overview

The ISDN Terminal Adapter Circuit interfaces standard terminals and PCs to a circuit switched data network or an ISDN. It supports both bitstuffing (V.110) and flag-stuffing (V.120) adaption protocols. The on-chip communication controllers handle signaling between data equipment and the network.

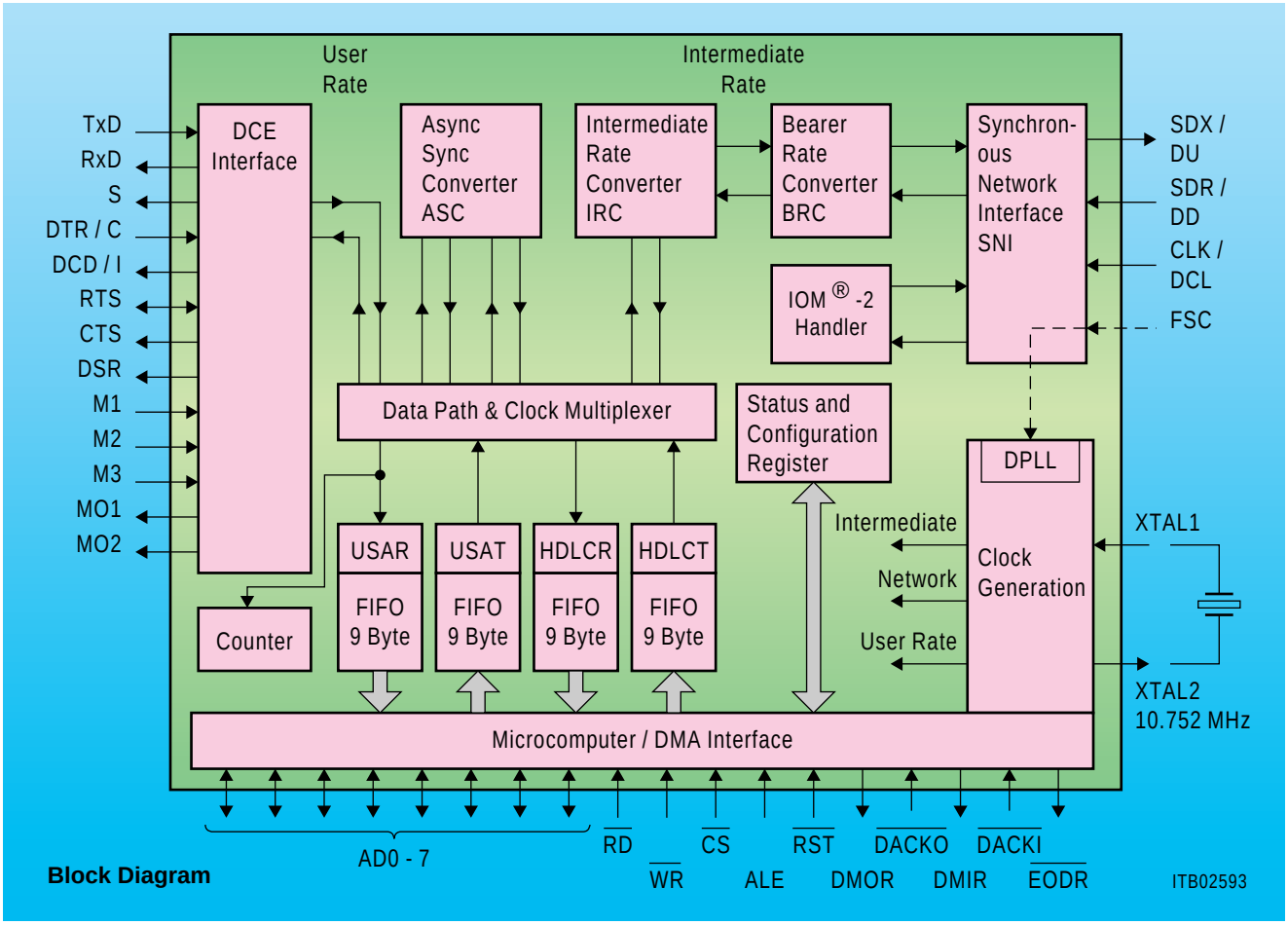
Applications

- Voice/Data Terminals
- ISDN PC Cards
- ISDN Terminal Adapters

Type	Package
PSB 2110-H	P-MQFP-44-1 (SMD)
PSB 2110-N	P-LCC-44-1 (SMD)
PSB 2110-P	P-DIP-40-1

Features

- Support of async and sync interfaces (X.21, X.21 bis V.24, RS232C, V.35)
- Modem control lines
- Programmable baud rates
- Bit rate adaption according to X.30, V.110, ECMA.102
- USART and HDLC controller to support V.120 and DMI applications
- In-band parameter exchange and signaling support
- Supports SSI- and IOM-2 interface for basic rate applications
- IOM-2 MONITOR channel controller
- Siemens/Intel multiplexed microprocessor interface
- Power-down (standby) mode



Block Diagram

General Description

The HSCX-TE is an optimized terminal version of the HSCX (SAB 82525). The HSCX-TE has been designed to implement high-speed communication links using HDLC protocols and to reduce the hardware and software overhead needed for serial synchronous communications.

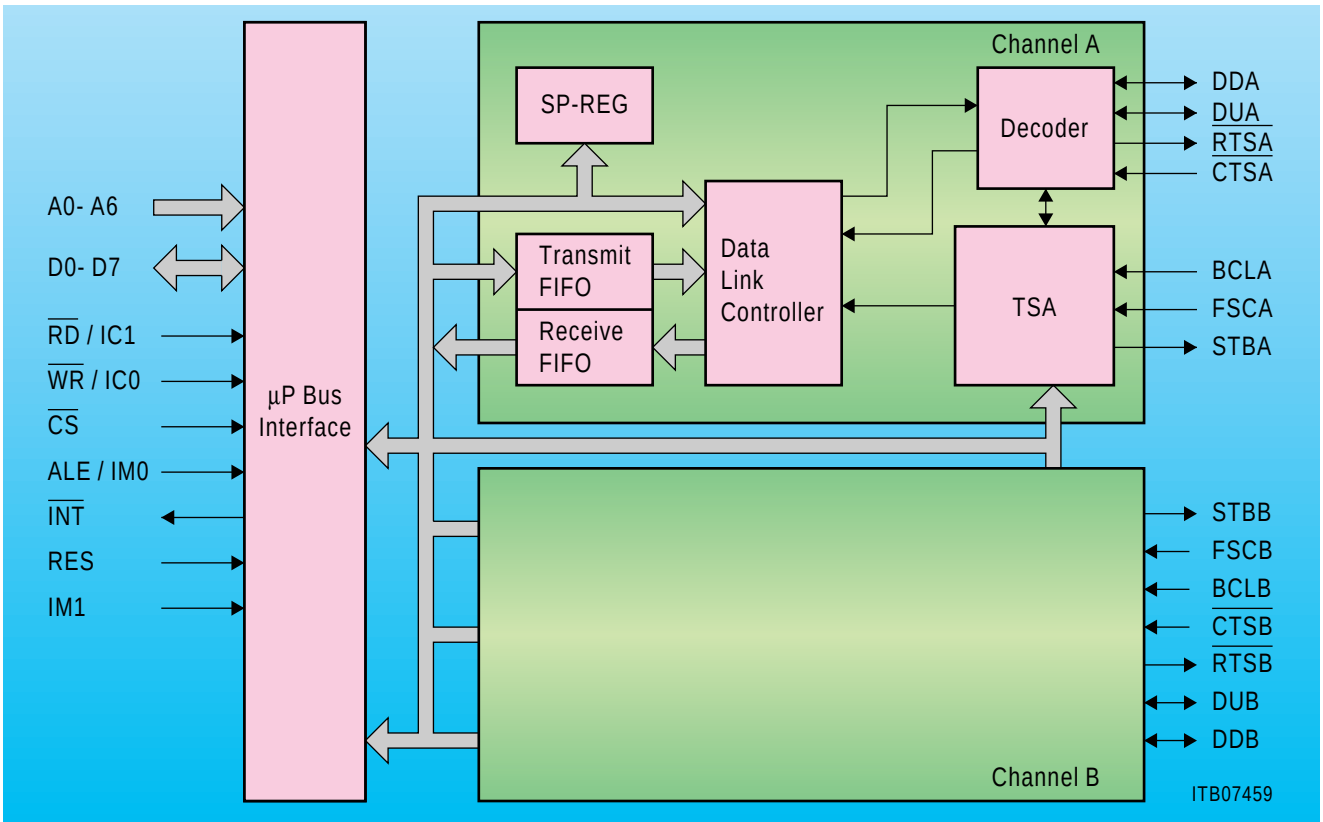
Applications

- ISDN PC Card/Standalone Box
- ISDN Data Terminal

Type	Package
PSB 21525-H	P-MQFP-44-2 (SMD)
PSB 21525-N	P-LCC-44-2 (SMD)

Features

- Optimized solution of HSCX (SAB) for terminal equipment
  Non-auto mode and transparent mode (no auto-mode)
  Clock mode 5 only
  Transfer of data blocks from/to system memory by interrupt request (no DMA mode)
- Two independent full-duplex HDLC channels
- Independent time-slot length (1-256 bit)
- Transparent receive/transmit of data bytes without HDLC framing
- Various types of protocol support depending on operating mode
- 64-byte FIFOs per channel and direction
- 8-bit demultiplexed or multiplexed bus interface



Block Diagram

General Description

The PSB 7280 is a device which implements voice compression algorithms defined in the ITU-TS G.711, G.722 and the G.728 Recommendation. It fits best into every application where audicompression is needed.

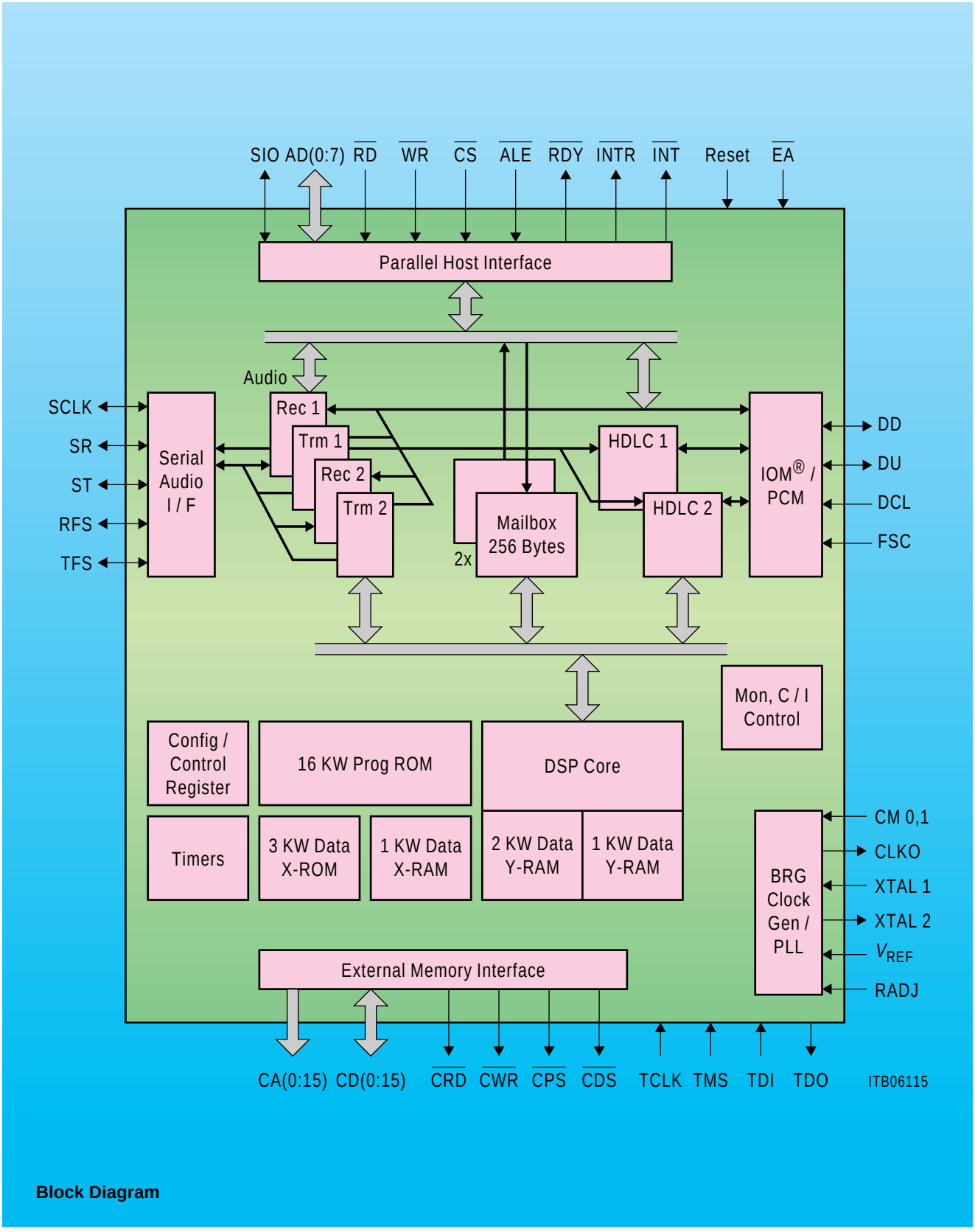
Applications

- ISDN videophones
- Video conference systems
- Corporate networks voice concentrators and gateways
- Data-over-voice and voice-over-data terminals
- Networks (e.g. LANs) for packetized voice
- Digital Added Main-Line (DAML) & Digital Circuit Multiplication (DCME) equipment
- Voice storage e.g. in PC based applications

Type	Package
PSB 7280-H	P-TQFP-100-1 (SMD)

Features

- G.711/G.722/G.728 compression/decompression for one audio channel
- Programmable G.711/G.722/G.728 modes with mixed modes of operation (e.g. G.722 in receive and G.728 in transmit direction)
- A/μ-Law recognition in G.711 mode (according to G.725 Appendix I)
- Fax modem signal recognition
- Accepts/outputs uncompressed audio in 8-bit PCM A/μ-Law, or linear 16-bit format
- Serial H.221 oriented audio protocol for direct connection to Videocodec (VCP of IIT Inc.)
- Two universal serial HDLC/transparent data controllers
- Programmable on-chip PLL for internal clock generation from ISDN low frequency clock
- All program and data memory on chip
- Flexible interfaces (e.g. IOM-2, serial audio interface, parallel 8-bit host interface, external memory interface)
- Supply voltage: 3.0 to 3.6 V
- 0.5-μm CMOS technology



Block Diagram

Subscriber Line Interface Codec Filter SLICOFI®; PEB 3065

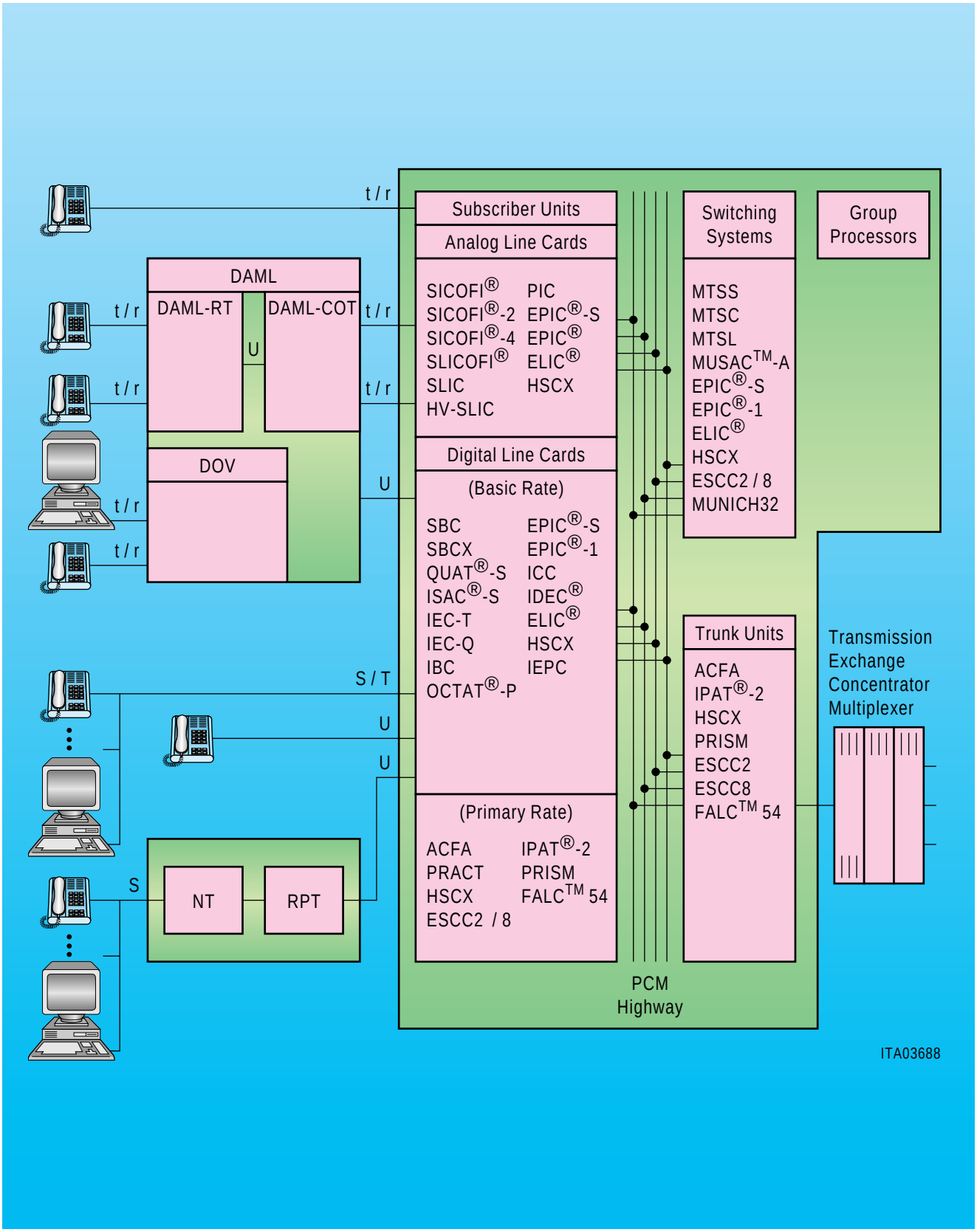
Digital Exchange System ICs

Positioning of the described products in different kinds of applications/segments:

Type	Analog Line Card	Digital Line Card	Digital Added Main Line (DAML)	Primary Rate Interface (PRI)	Data Over Voice (DOV)	Network Termination Remote Power Termination (NT/RP)	Trunk Units
PIC	•				•		
EPIC®-S	•	•					
EPIC®-1	•	•					
ELIC®	•	•					
SICOFI®	•		○		•		
SICOFI®-2	•		•		•		
SICOFI®-4	•		•		•		
SICOFI®-4µC	•		•		•		
ICC		•	○		○		
IDEC®		•					
SBC		•				•	
SBCX		•				•	
QUAT®-S		•					
IEC-Q		•	•		•	•	
IEC-T		•	•		•	•	
Quad IEC DFE-T		•					
Quad IEC AFE		•					
Quad IEC DFE-Q		•					
IBC		•					
OCTAT®-P		•					
IEPC		•					
ACFA				•			
IPAT®-2				•			
PRISM				•			•
FALC™54				•			•
ARCOFI®					•		
ARCOFI®-SP					•		
ITAC®					•		
IRPC		•	•			•	
GPPC		•				•○	
ISAC®-S		○					
ISAC®-P		○					
SLICOFI®	•		•		•		
HV-SLIC	•		•		•		
PRACT				•			
HSCX	•	•		•			•
ESCC2				•	•		•
ESCC8				•			•

• = Main application
○ = Optional

Digital Exchange System ICs
General Overview on Architecture and Devices



Analog Line Cards

Product Overview

Type	Short Title	Description	Page
PEB 2052	PIC	PCM Interface Controller	89
PEB 2054	EPIC®-S	Extended PCM Interface Controller-Small	90
PEB 2055	EPIC®-1	Extended PCM Interface Controller	91
SAB 82525 SAB 82526	HSCX HSCX1	High-Level Serial Communication Controller Extended	162
PEB 20550	ELIC®	Extended Line Card Interface Controller	92
PEB 2060	SICOFI®	Signal Processing Codec Filter	94
PEB 2260	SICOFI®-2	Dual Channel Codec Filter	96
PEB 2465	SICOFI®-4	Four Channel Codec Filter	97
PEB 2466	SICOFI®-4 µC	Four Channel Codec Filter with µC Interface	99
PEB 3065	SLICOFI®	Signal Processing with integrated low voltage SLIC Codec Filter	100
PEB 4065	HV-SLIC	Subscriber Line Interface Circuit (High Voltage Part)	101

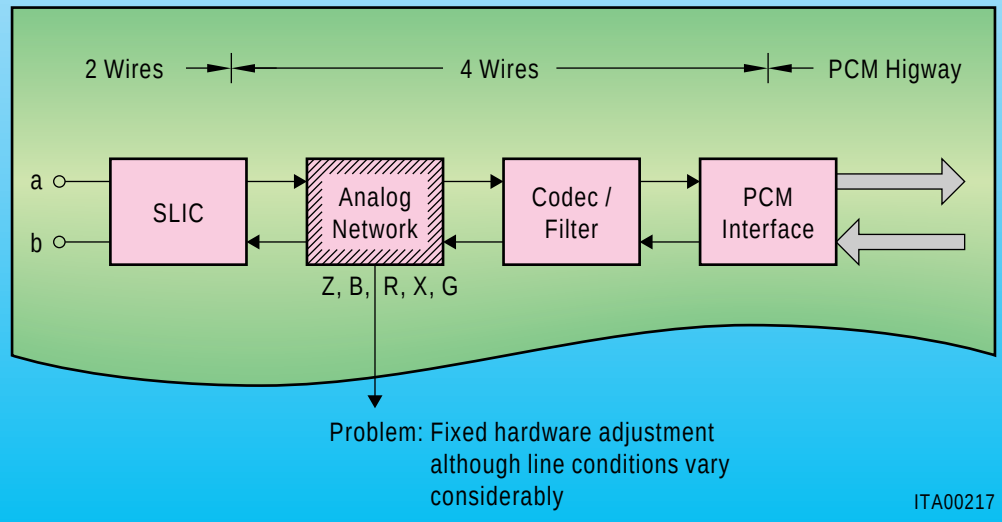
Analog Line Cards

In a digital exchange system the subscriber line boards provide the link between the subscriber and the switching network. The basic functions of analog line boards are known under acronym BORSHT (Battery, Overvoltage, Ringing, Supervision, Hybrid, Testing). Additional important tasks are voice frequency band limitation, analog to digital conversion into time discrete digital equivalents, time-slot assignment on the PCM highways and handling of signaling and control information.

The **conventional implementation** uses two PCM ports and one µP interface per subscriber line leading to a large amount of wiring and, thus, problems are as crosstalk and large board size.

The **conventional implementation** is also characterized by the fixed adjustment of line interface conditions although telephone line conditions vary considerably with national standards and even with subscriber line installations. Under adverse conditions telecommunication equipment must match the subscriber line and termination impedances while suppressing return echoes in the two to-four-wire hybrid network. Compensating for line attenuation is just as critical for balancing the voice signals in the transmission and reception paths. To improve voice quality, subscriber line boards have to be matched to different line conditions by means of interchangeable discrete components. This approach is very costly regarding line board design and manufacturing. Furthermore, the reliability of a board filled with parts, wires and connections will decrease rapidly.

The best solution to eliminate these line card trouble spots is the design of one standard line card, which can be customized for various line conditions and postal specifications through software control. The right choice of dedicate device allows the optimal line card design for each application in public switches, PBX systems as well as in all kinds of multiplexers and concentrators.



General Line Board Structure and Functions

General Line Card Function

Component		Function
SLIC (Subscriber line interface circuit)		Realization of the BORSHT function B Battery feed O Overvoltage Protection R Ringing S Supervision H Hybrid T Testing
Analog network	Z	Matching of input and line independence
	R, X	Frequency response correction
	B	Hybrid balancing
	G	Gain adjustment
CODEC/Filter		Coding, A/D and D/A conversion according to A-Law and µ-Law, voice Band limitation according to CCITT and LSSGR
PCM		Time-slot assignment, PCM-data rate

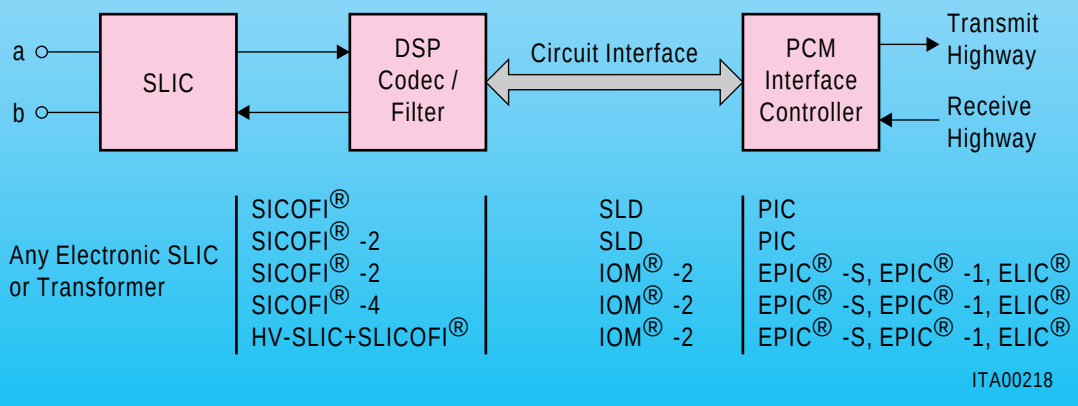
The Siemens Semiconductor concept is characterized by a centralized PCM interface controller device providing the variable Time-Slot Assignment (TSA), the communication with up to 64 subscriber line devices such as a signal processing codec/filter (SICOFI) or ISDN devices via the SLD (Subscriber Line Data) or IOM-2 (ISDN Oriented Modular) interface, and the interface with a microprocessor.

As a characteristic architectural feature, for test, monitoring, and control purposes, the device permits efficient switching of data streams between all these interfaces and, therefore, ensures transparency between the PCM channels and control or signaling data. This opens up attractive possibilities such as common-channel signaling and microprocessor access to PCM data.

The use of the signal processing codec/filter (SICOFI) avoids the analog network which has to be matched to different requirements by interchanging its discrete components. Based on Digital Signal Processing (DSP) methods the SICOFI allows the complete control of the line conditions by software.

The all-over flexibility and programmability of the unique device concept gives the user the capability for designing a standard line card which can be optimized for each application and can be matched to various line conditions.

The SLD/IOM-2 architecture leads to a highly modular line board configuration with low wiring, reduced board area, and, dependent on the SLIC being used, very few external discrete components.

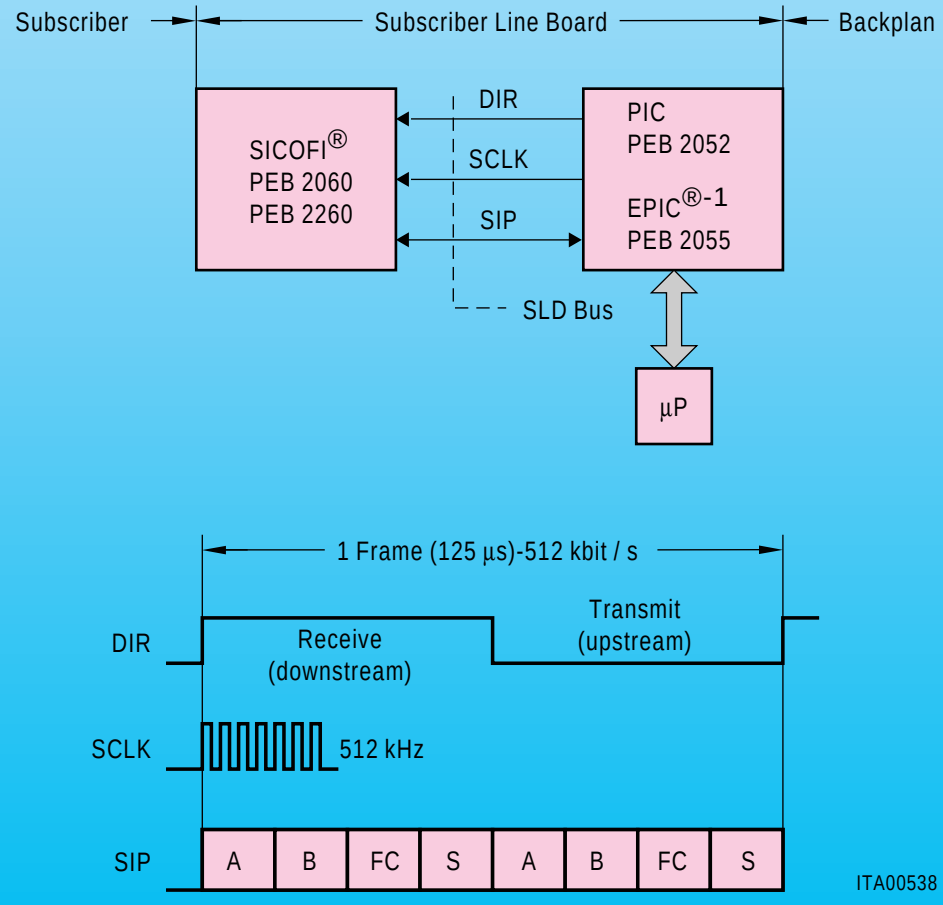


Siemens ICs for Analog Subscriber Lines, Configurations and Interfaces

The **SLD-bus** is used by the PIC (PCM Interface Controller) to interface with the subscriber line devices. A **S**erial **I**nterface **P**ort (SIP) is used for the transfer of all digital voice and data, feature control and signaling information between the individual subscriber line devices, the PCM highways and the control backplane. The SLD approach provides a common interface for analog or digital per-line components. Through the PIC, which is the key device in the SLD-architecture, the PCM data is transparently switched onto the PCM highways. The PBC (Peripheral Board Controller) will make analog and digital subscriber line boards plug-compatible in a line equipment rack.

There are three wires connecting each subscriber line device and the PIC: two common clock signals shared among all devices, and a unique bidirectional data link for each of the eight SIP lines. The **Dir**ection signal (DIR) is an 8-kHz clock output from the PIC (master) that serves as a frame sync to the subscriber line devices (slave) as well as a transfer indicator. The data are transferred at a 512-kHz rate, clocked by the **S**ubscriber **Cl**oc**k** (SCLK). When DIR is high (first half of the SLD 125 µs frame), four bytes of digital data are transmitted on the SLD-bus from the PIC to the slave (receive direction). During the second half of the frame when DIR is low, four bytes of data are transferred from the slave back to the PIC (transmit direction).

Channel A and B are 64-kbit/s channels reserved for voice or data to be routed to and from the PCM highways. In an application where one SICOFI is connected to a SIP, voice is received on channel A and transmitted on channel A and B. For a three-party conference, channel B is the third-party voice channel. If two SICOFIs are connected to one SIP, channel A is assigned to one and channel B to the other SICOFI. Conferencing is not possible in this configuration. With digital subscriber line devices the two bytes can be used to carry 64-kbit/s data channels. The third and sixth byte locations are used to transmit and receive control information for programming the slave devices. The last byte in each direction is reserved for signaling data.



Frame Structure of the SLD Interface

The **IOM®-Revision-2 (IOM®-2)** standard defines an industry standard serial bus for interconnecting telecommunication ICs. The standard covers line card, NT1, and terminal architectures for ISDN and analog loop applications.

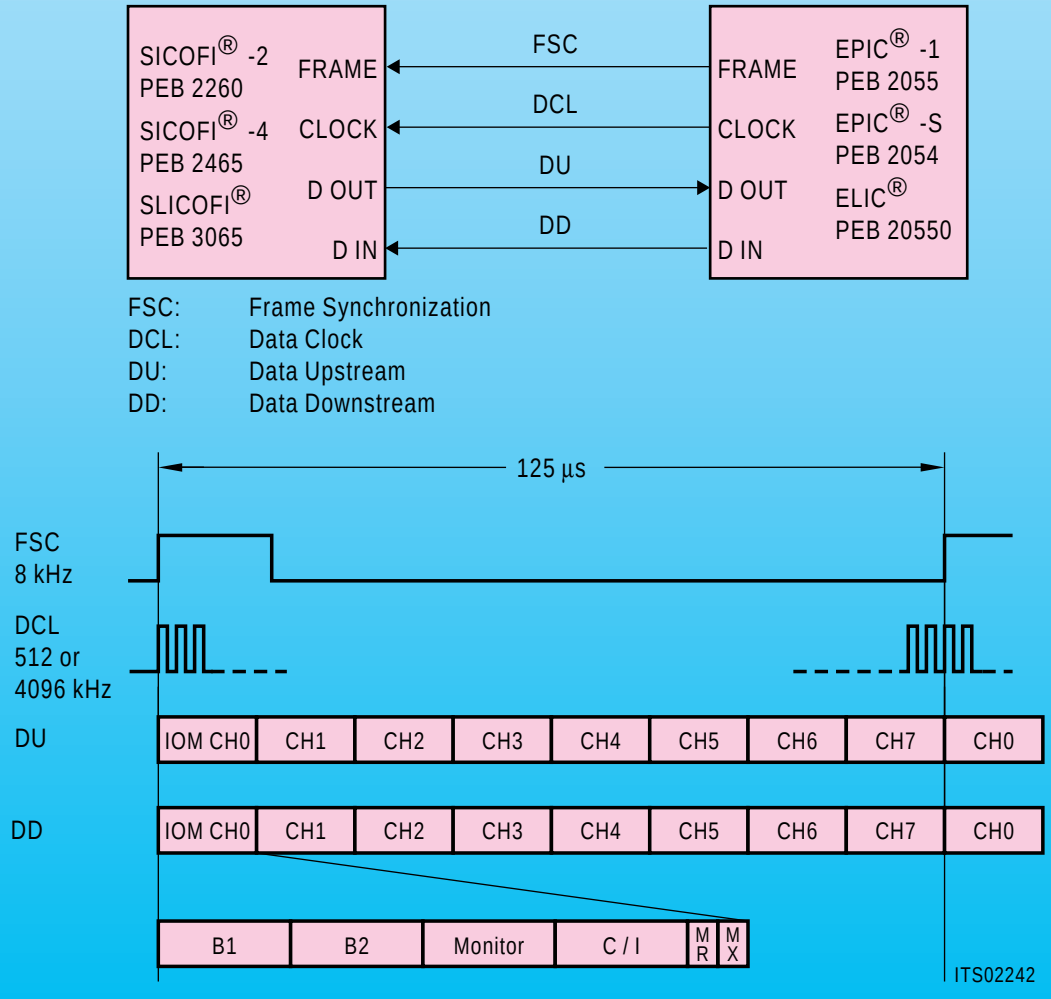
The line-card mode of IOM-2 provides a connection path between line transceivers (ISDN) and codecs (analog), and the line-card controller; the line card controller provides the connection to the switch backbone. The IOM-2 bus time multiplexes data, control, and status information for up to eight ISDN transceivers or up to 16 codec/filters over a single full-duplex interface.

By providing data, control, and status information over a serial channel, the IOM-2 bus eliminates the need to have a microprocessor interface on the transceiver or codec. This reduces pin count and simplifies line-card layout, thus reducing cost.

Information is multiplexed into frames, which are transmitted at an 8-kHz rate. The frames are subdivided into from one to eight subframes, with one subframe being dedicated to each transceiver or pair of codecs. The subframes provide channels for data, programming, and status information for a single transceiver or a codec pair.

The channel structure of the IOM-2 interface is as follows:

- The first two octets constitute the two 64-bit/s B-channels.
- The third octet is the monitor channel. It is used for the exchange of data between devices using the IOM-2 monitor channel protocol.
- The fourth octet (control channel) contains
  – two bits for the 16-kbit/s D-channel
  – a four-bit command/indication channel, in ISDN applications or
  a six bit command/indication channel for analog subscriber applications
  – two bits MR and MX for supporting the monitor channel protocol.



Multiplexed Frame Structure of the IOM®-2 Interface

General Description

The PCM Interface Controller (PIC) PEB 2052 is a device for the control of voice, data and signaling paths of up to 16 subscribers on peripheral component boards in digital communication systems. In combination with the highly flexible Signal Processing Codec Filter (SICOFI) PEB 2060/2260 it forms an optimized, analog subscriber line board architecture. Its flexibility enables its operation as a general-purpose controller for data switching and MUX/DEMUX applications.

The PIC controls space and time switching functions between subscriber line devices and time division multiplex highways. Furthermore, it controls the flow of information between the subscriber inferface ports and a line card local processor.

To meet different requirements the PIC PEB 2052 provides the following interfaces:

- Eight serial, bidirectional I/O ports for the transfer of voice, data, control and signaling information between the PBC and codec filters (e.g. SICOFI PEB 2060/2260), digital interface circuits or signal processors.
- Double constructed PCM interface for a redundant system configuration with load sharing operation.
- Bit-parallel interface for the connection of a standard 8-bit microcomputer such as SAB 8051.

Type	Package
PEB 2052-N	P-LCC-44-1 (SMD)

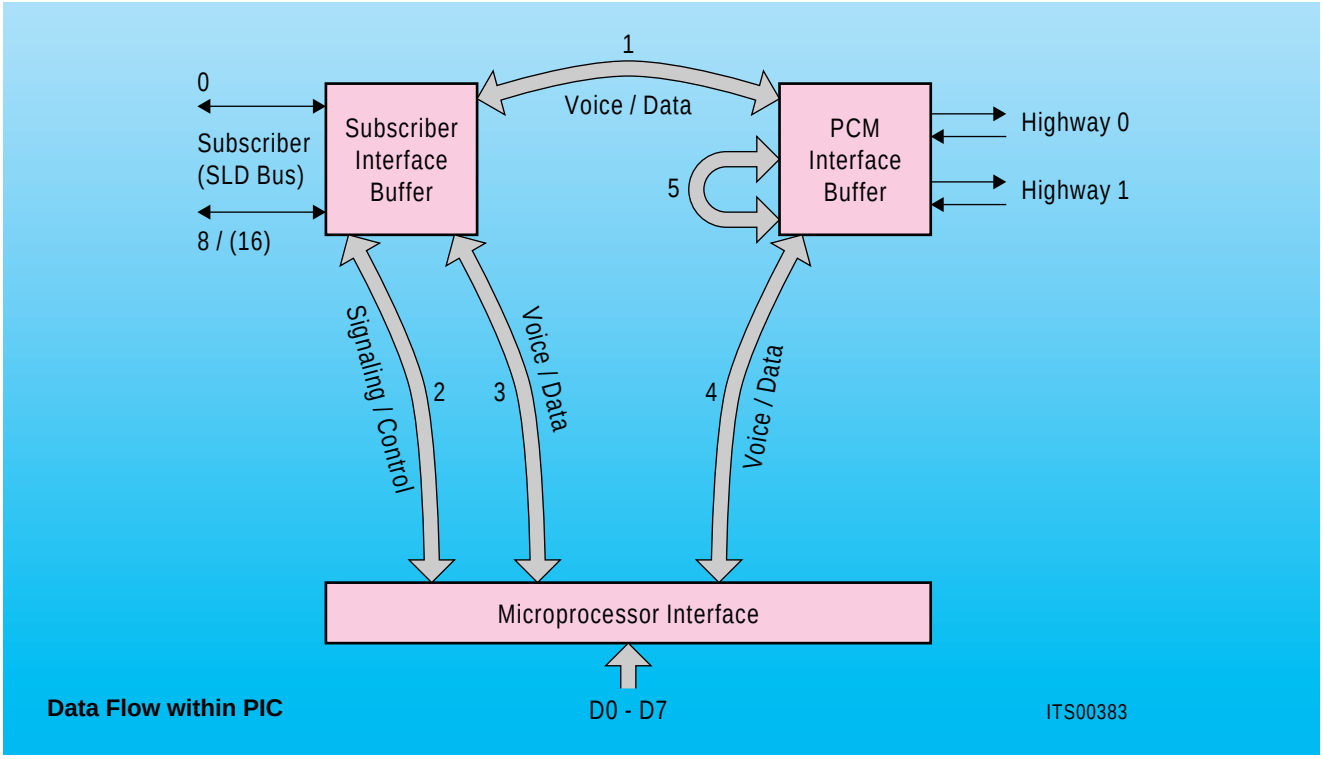
Features

- Board controller for up to 16 subscribers of a digital switching system
- Suitable for all PCM systems (24/32/48/64 time-slots) according to European and US standards
- SLD-bus to peripheral circuits, e.g. codec filter devices or ISDN components
- Time-slot assignment freely programmable for all connected subscribers
- µP access to all internal data streams including time-slot oriented data streams
- All functions software-programmable via a standard µP interface
- TTL-compatible inputs and outputs, including clock input
- Single + 5 V power supply
- Advanced low power CMOS technology

Applications

Telecommunication subscriber board interface controller IC for digital exchange PCM systems performing:

- digital exchange functions
- digital concentrator functions
- signaling and interface control functions
- multiplex functions



Data Flow within PIC

General Description

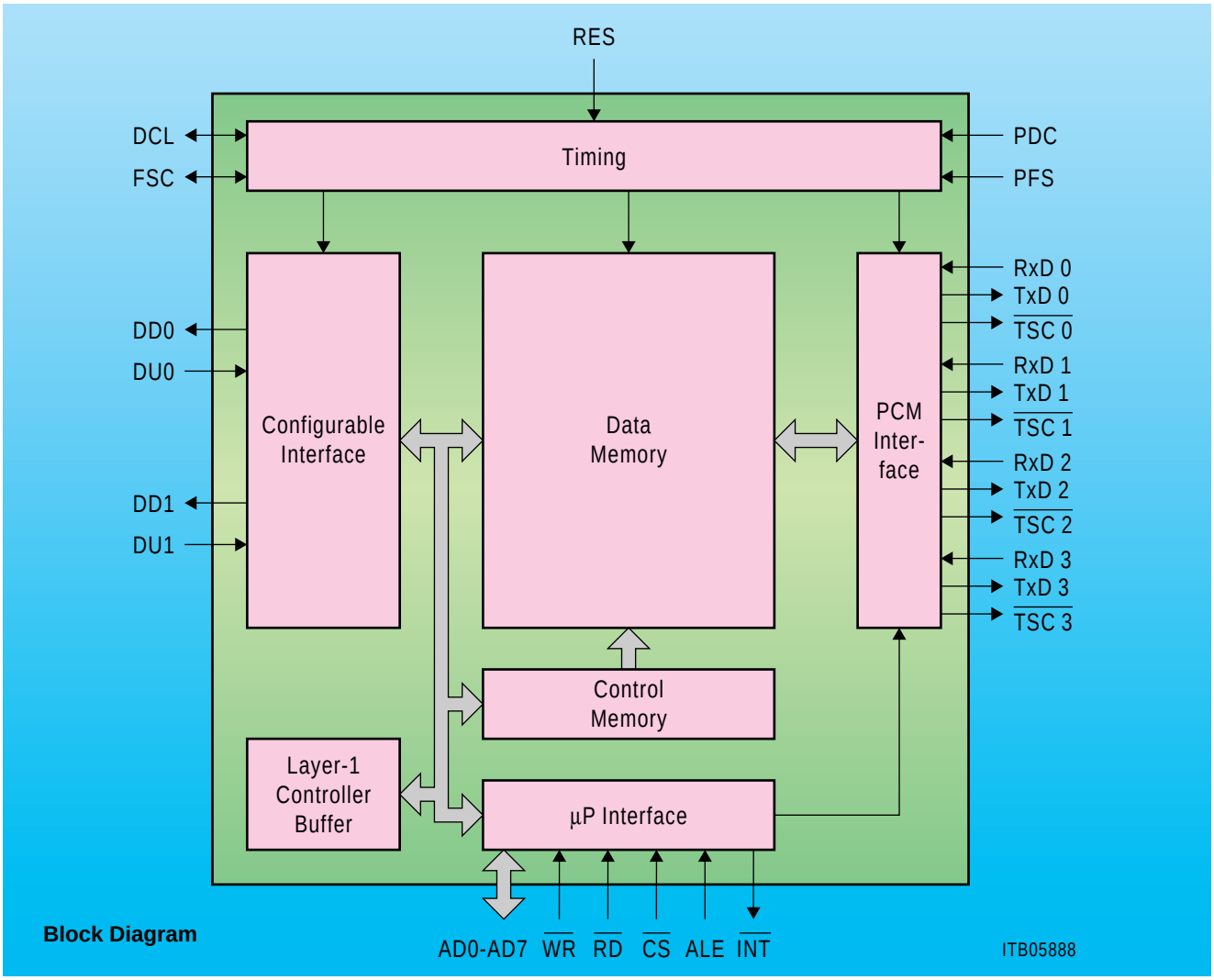
Information from subscriber lines needs to be transferred to time-slots on system internal PCM communication highways. The EPIC-S concentrates the circuitry necessary to do this interfacing for a large number of transmission lines on a single IC. Therefore, it is not necessary to repeat this PCM interface circuitry for every line. Applications of the EPIC-S include communications multiplexers, concentrators, central switches, PBXs, as well as peripheral ISDN and analog line cards.

Features

- PCM interface controller for up to 16 ISDN or 32 analog subscribers
- Time-slot assignment freely programmable for all subscribers
- Non-blocking switch for 64 channels
- Switching of 16-, 32-, 64-kbit/s channels (128 kbit/s via two consecutive 64-kbit/s channels)

Type	Package
PEB 2054-N	P-LCC-44-1 (SMD)
PEF 2054-N	P-LCC-44-1 (SMD)

- Two serial interfaces: PCM and configurable
- Programmable for a wide range of data rates (PCM up to 8 Mbit/s, configurable up to 4 Mbit/s)
- Data rates of PCM and configurable interfaces independent of each other (data rate adaption)
- Change detection (“last look”) logic for C/I or signaling channels
- 16-byte FIFO for monitor or feature control channels
- Standard µP interface with multiplexed address/data bus or separate address and data busses
- Advanced low power CMOS technology
- Also available with extended temperature range – 40 to 85 °C (PEF 2054-N)
- Pin compatible with PEB 2055



Block Diagram

General Description

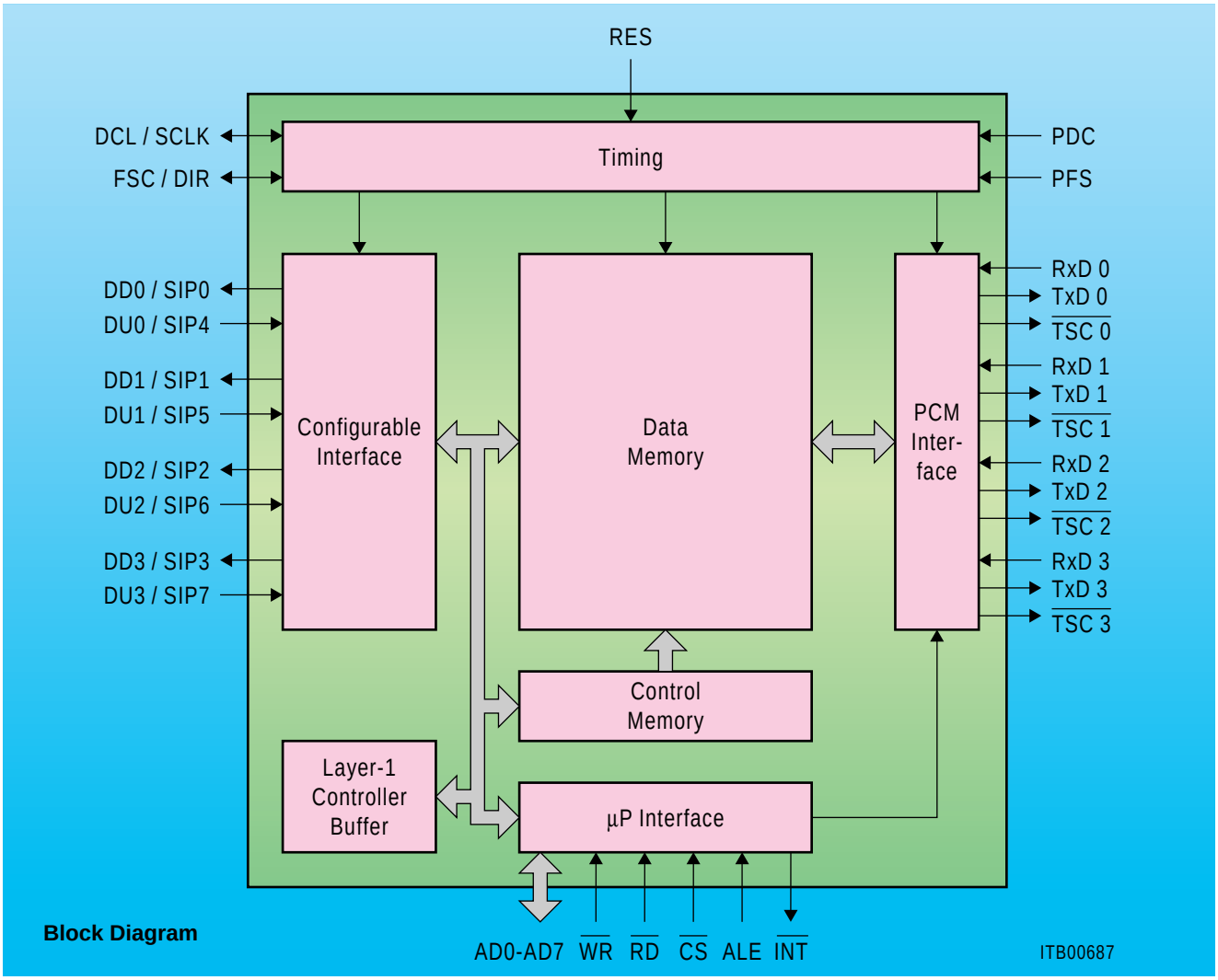
Information from subscriber lines needs to be transferred to time-slots on system internal PCM communication highways. The EPIC-1 concentrates the circuitry necessary to do this interfacing for a large number of transmission lines on a single IC. Therefore, it is not necessary to repeat this PCM interface circuitry for every line. Since the system cost of the EPIC-1 is divided by the number of lines it controls, powerful and comfortable functions can be economically performed.

Features

- PCM interface controller for up to 32 ISDN or 64 analog subscribers
- Time-slot assignment freely programmable for all subscribers
- Non-blocking switch for 128 channels
- Switching of 16-, 32-, 64-kbit/s channels (128 kbit/s via two consecutive 64 kbit/s channels)
- Two serial interfaces: PCM and configurable (IOM-2, IOM-1, SLD, PCM).

Type	Package
PEB 2055-N	P-LCC-44-1 (SMD)
PEF 2055-N	P-LCC-44-1 (SMD)

- Interfacing with four full-duplex PCM highways (up to 8 Mbit/s)
- Data rates of PCM and configurable interfaces independent of each other
- Change detection (“last look”) logic for C/I or signaling channels
- 16-byte FIFO for monitor or feature control channels
- Standard µP interface with multiplexed or demultiplexed address/data bus or separate address and data busses
- Advanced low power CMOS technology
- Also available with extended temperature range – 40 to 85 °C (PEF 2055-N)



Block Diagram

General Description

The Extended Line Card Controller (ELIC) PEB 20550-H is a device to allow the control, supervision and processing of voice, data and signaling information. It also provides access for the microcontroller to write/read data to/from the IOM and PCM interfaces and gives control over layer-1 devices. Revolutionary is the multiplexing concept allowing to use only one implemented HDLC controller to process the signaling information for up to 32 digital subscribers.

The switching part of the ELIC controls space and times switching functions between subscriber line devices and time division multiplex highways. Furthermore it controls the flow of information between the subscriber interface ports and a processor.

For processing signaling information two different HDLC controllers are implemented. The **SACCO A** is a Serial Access Communication Controller (HDLC) which allows extracting D-Channel information transported on the IOM interface. The data is then passed to the microcontroller. In the downstream direction, the SACCO A passes data, packed in the HDLC protocol, from the microcontroller to the IOM interface.

With 4 IOM interfaces, and 8 digital subscribers possible per interface, former designs needed 32 HDLC controllers (one for the D-channel of every subscriber). The SACCO A of the ELIC can serve all 32 channels in a time-multiplexing manner. This process is controlled by the **BUS ARBITER.** This part of the ELIC monitors all D-channels of the IOM interface and locks the SACCO A onto one D-channel as soon as the start of a HDLC frame is detected. After the end-flag of the HDLC frame has been received, the SACCO A is released again and can lock onto the next D-channel as soon as a new request is detected. During the assignment of the HDLC controller to a certain channel the other subscribers are not allowed to send information on their D-channels. To assure this a blocking mechanism is implemented which indicates to corresponding terminals that they may not use the D-channel. This mechanism works as well for the standard ISDN S_0 as for the proprietary U_P interface, a two wire ISDN capable interface for PBXs. Any ISDN Telephone can be connected to a PBX because the standard arbitration mechanism is used for blocking the phones.

This concept saves the space and the costs of up to 32 HDLC controllers. Due to the bursty characteristic of the signaling data, one HDLC controller is sufficient to process this data flow. For central office applications the ELIC is not recommended when the arbiter is used, as PTTs require transparent D-channels. In this case the SACCO A can be used as an independent HDLC controller.

If the design needs higher D-channel data rates additional HDLC controllers (IDEC, PEB 2075) can be connected. This can either be done on the IOM interface and is than fixed for a certain subscriber or via the PCM interface which makes this extra HDLC controller flexibly assignable.

Type	Package
PEB 20550-H	P-MQFP-80-1 (SMD)

The **SACCO B** is a second integrated HDLC controller behaving like an external device. It is mainly intended for signaling information between the line card and the group processor on the main board. This can be done either via a dedicated signaling highway or via the PCM highway. The SACCO B can also be used for music on hold, conferencing access and other features. The HDLC information handling between SACCO A and SACCO B always has to go via a microprocessor.

Features

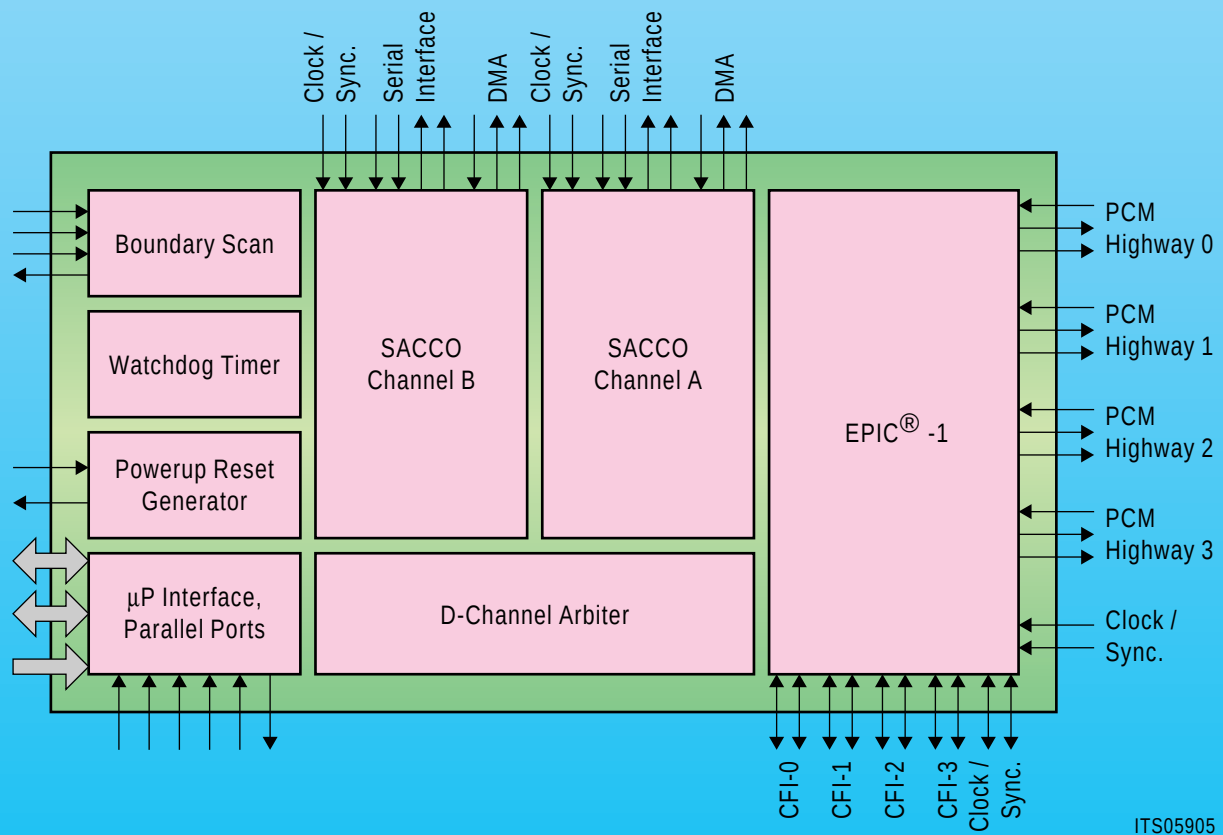
- Configurable interface (CFI) programmable for IOM-2, IOM-1, SLD or PCM
- Switching between configurable interface (e.g. lOM-2) and PCM ports
- Switching of 64 B-channels (32 digital or 64 analog subscribers) without blocking (128 × 128 matrix)
- Two HDLC controllers with 64-byte FlFOs implemented
- Arbiter logic to use one of the HDLC-controllers time multiplexed for a maximum of 32 digital subscribers
- Full-duplex signaling protocols (LAPD or proprietary)
- HDLC broadcast messages
- DMA access to HDLC data
- Boundary scan

Application Areas

- PBX:
  – analog line cards
  – digital line cards
- CO:
  – analog line cards (with disabled arbiter)
  – digital line cards (with disabled arbiter)

Interfaces

- 4 configurable interfaces (individually programmable for IOM, SLD, PCM)
- 4 PCM interfaces (maximum combined data rate of 8 Mbit/s)
- µP interface (Siemens/lntel and Motorola interface, multiplexed and demultiplexed address/data bus)
- Boundary scan (for on-board tests)
- DMA interface



Block Diagram

General Description

The Signal Processing Codec Filter (SICOFI) PEB 2060 is a fully integrated PCM codec (coder-decoder) and transmit/ receive filter produced in advanced CMOS technology for applications in digital exchange telecommunication systems. Based on a digital filter concept the PEB 2060 provides improved transmission performance and high flexibility. It enables the control of the device's analog behavior by digital signal processing, including attractive features such as programmable trans-hybrid balancing, impedance matching, level control and frequency response correction. The device is optimized for working in conjunction with the PCM Interface Controller PEB 2052/55.

The analog input signal is A/D converted, digitally filtered and transmitted either PCM-encoded or linear. Antialiasing is done with a 2nd order Sallen-Key Prefilter (PREFI). The A/D Converter (ADC) is a modified slope adaptive interpolative coder with a sampling rate of 128 kHz. Digital downsampling to 8 kHz is done by subsequent decimation filters D1 and D2 together with the PCM bandpass filter (BP).

The digital input signal is received PCM encoded or linear, digitally filtered and D/A converted to generate the analog output signal. Digital interpolation up to 128 kHz is done by the PCM lowpass filter (LP) and the interpolation filters I1 and I2. The D/A Converter (DAC) output is fed to the 2nd order Sallen-Key Postfilter (POFI).

The high flexibility of the SICOFI is based on a variety of user programmable filter, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the trans-hybrid balancing filter B.

The SICOFI bridges the gap between analog and digital voice signal transmission in modern telecommunication systems.

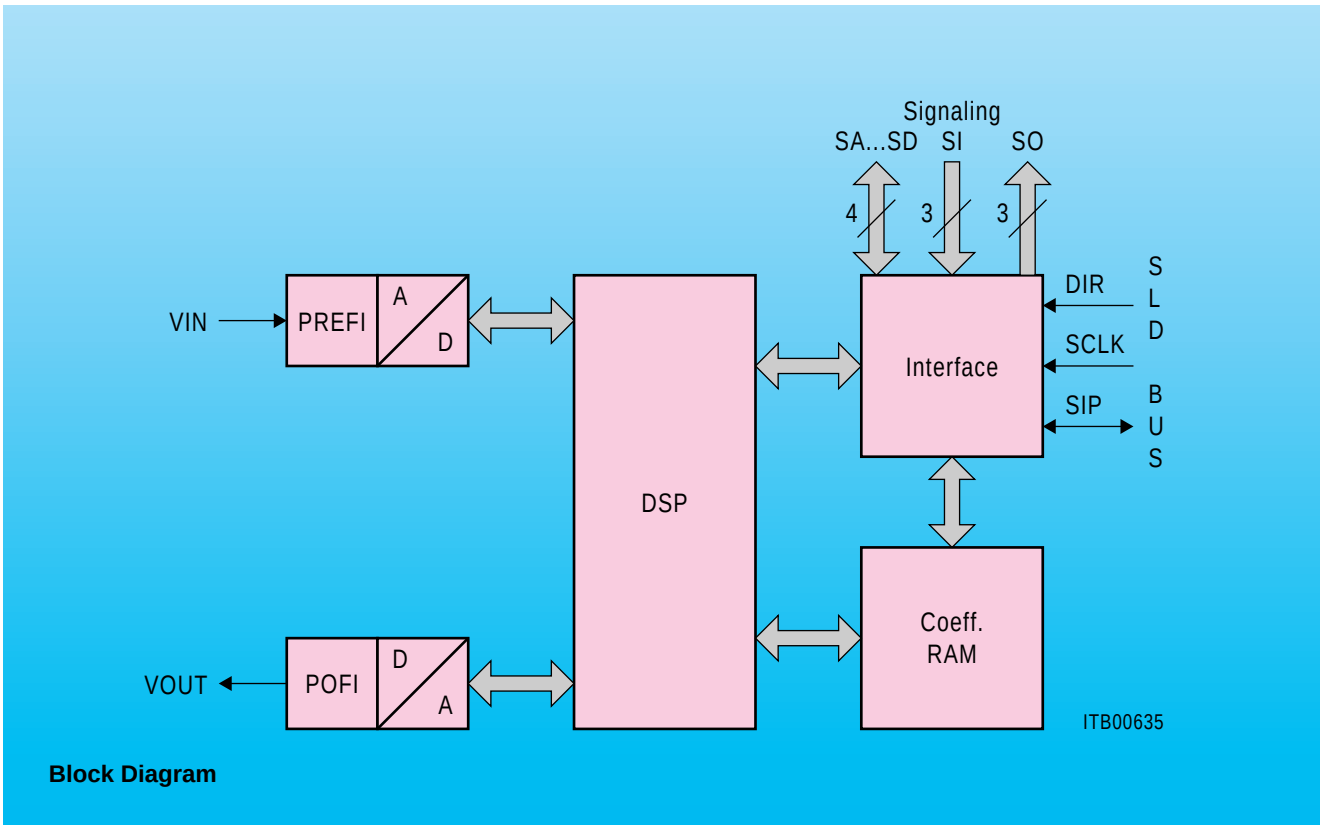
High performance oversampling Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) provide the conversion accuracy required. An analog antialiasing Prefilter (PREFI) and smoothing Postfilter (POFI) is included. The dedicated on-chip Digital Signal Processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM comparing. The 3-pin serial SLD-Bus interface handles digital voice transmission and SICOFI feature control. Specific filter programming is done by downloading coefficients to the Coefficient RAM (CRAM).

The 10-pin parallel signaling interface provides for a powerful per line SLIC control.

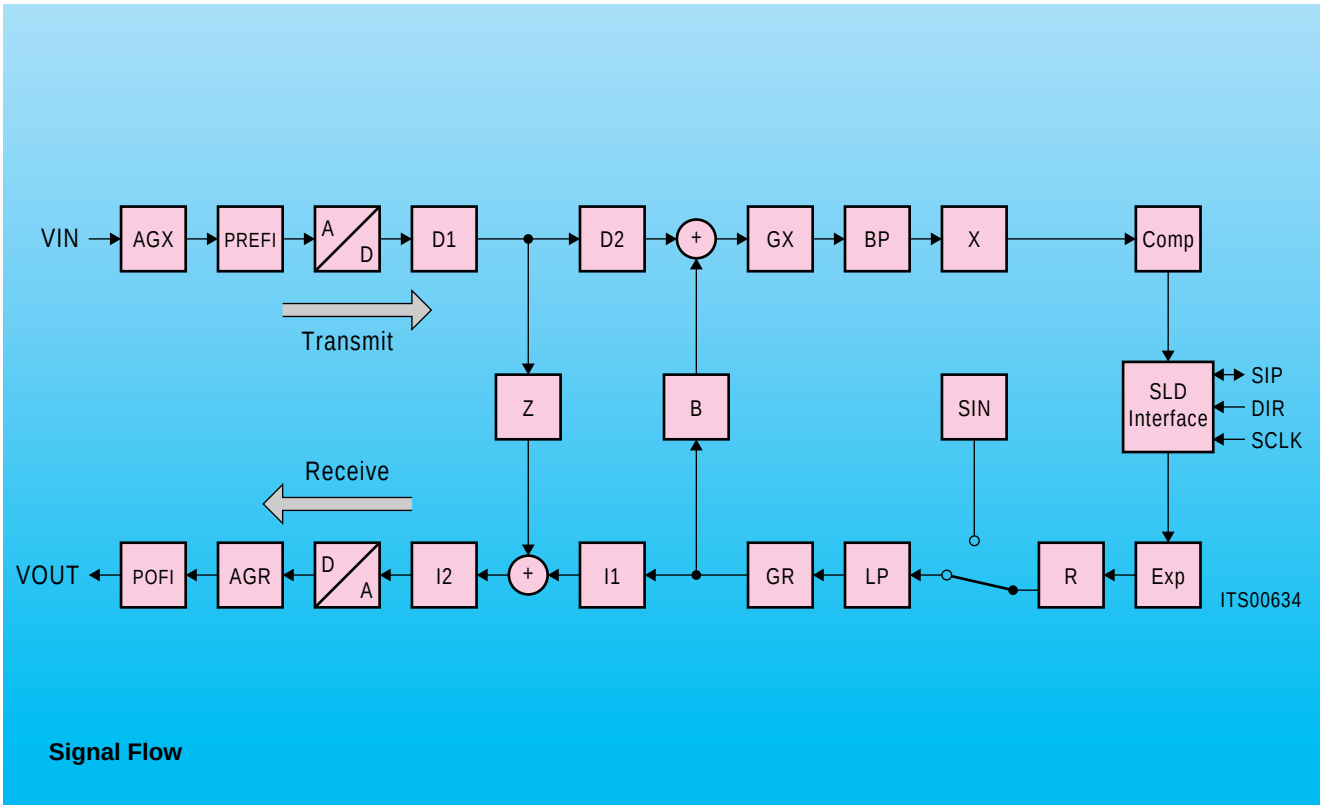
Type	Package
PEB 2060-N	P-LCC-28-1 (SMD)
PEB 2060-P	P-DIP-22-1 (not for new development)

Features

- Single-chip codec and filter
- Band limitation according to CCITT and LSSGR recommendations
- Digital signal processing techniques
- Digital voice transmission
  – PCM encoded (A-Law or μ-Law)
  – linear (16-bit 2s complement)
- Programmable digital filters for
  – impedance matching
  – transhybrid balancing
  – gain
  – frequency-response correction
- Configurable 3-pin serial interface
  – 512-kHz SLD-Bus (e.g. to PEB 2052/55)
  – burst mode with bit rates up to 8 MHz
- Programmable signaling interface with peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain
- Advanced test capabilities
  – three digital loopback modes
  – two analog loopback modes
  – on-chip sinewave generation
- No trimming or adjustment
- No external components
- Variable SICOFI master clock selection
- Signaling expansion possible
- Prepared for three-party conferencing
- Advanced low power CMOS technology



Block Diagram



Signal Flow

General Description

The Dual Channel Codec Filter PEB 2260 (SICOFI-2) is a fully integrated PCM codec and filter fabricated in low power CMOS technology for applications in digital communication systems. Based on an advanced digital filter concept, the PEB 2260 provides excellent transmission performance and high flexibility. The digital signal processing approach includes attractive programmable features such as trans-hybrid balancing, impedance matching, gain and frequency response correction.

The SICOFI-2 can be programmed to communicate either with SLD or with IOM-2 compatible PCM-interface controllers (e.g. PEB 2052/54/55).

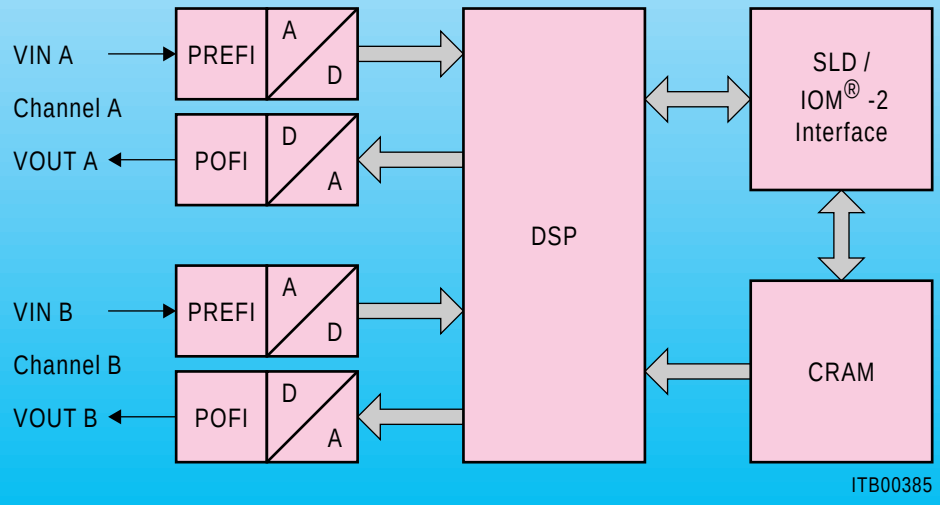
The device bridges the gap between analog and digital voice signal transmission in modern telecommunication systems.

A high performance oversampling Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) provide the conversion accuracy required. Analog antialiasing Prefilters (PREFI) and smoothing Postfilters (POFI) are included. The dedicated on-chip Digital Signal Processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The SLD/IOM-2 interface handles digital voice transmission, SICOFI-2 feature control and access to the SICOFI-2 signaling pins. Specific filter programming is done by downloading coefficients to the Coefficient RAM (CRAM).

Type	Package
PEB 2260-N	P-LCC-28-1 (SMD)
PEF 2260-N	P-LCC-28-1 (SMD)

Features

- Dual channel single chip codec and filter
- Band limitation according to CCITT and LSSGR recommendations
- Digital signal processing techniques
- PCM encoded digital voice transmission (A-Law or µ-Law)
- Programmable digital filters for
  – impedance matching
  – transhybrid balancing
  – gain
  – frequency response correction
- SLD- and IOM -2 interface
- Programmable signaling interface to peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain
- Advanced test capabilities
  – three digital loopback modes
  – two analog loopback modes
  – two programmable tone generators
- No trimming or adjustments
- No external components
- Advanced low power CMOS technology
- Also available with extended temperature range – 40 °C to 85 °C (PEF 2260-N)



Block Diagram

General Description

The Signal Processing Codec Filter (PEB 2465-H), SICOFI-4 is the interface between four analog subscribers and the digital switch. The chip combines all the circuitry needed for encoding, decoding and PCM filtering of 4 speech channels on CMOS chip. An integrated digital signal processor (DSP) allows the analog line card to be adapted to the widest variety of national specifications and applications by programming the individual digital filter functions. A wide variety of SLICs (subscriber line interface circuits) can be employed and simply adapted.

The SICOFI-4 can be used in both, PBXs and public switches. The external configuration does not vary – only decoupling capacitors are needed. Widely differing national specifications can be met with a single hardware by just changing the filter coefficients: Signal level, terminating impedance, equivalent impedance, frequency response correction and the required coding procedure (A- or µ-Law) are simple to program. Siemens provides well proven software for calculating the required coefficients.

The SICOFI-4, together with standard SLICs, also fulfills the new specification for idle channel noise in the out-of band range, already demanded by Japan and Great Britain.

A flexible test concept operating at component level as well as at system level is provided to support users in designing and manufacturing their systems. The following test options are integrated into the SICOFI-4:

- BIST (built-in self test) in the digital part
- Boundary scan as per IEEE 1149.1
- Functional testing with various test loops
- Simple stimulation by two built-in DTMF (Dual Tone Multifrequency) tone generators
- Function self test using what is known as the “level metering function” with which not only the chip but also the SLIC connected to it can be tested (system test).

The powerful, modular IOM-2 interface implemented on the allows minimal wiring to be used on the board and thereby a low-cost design. A suitable controller (e.g. the ELIC, PEB 20550-H) is used to direct the relevant coefficients for filter programming and the required control signals as well as the voice signals to the SICOFI-4. Signals from the SLIC can be issued by the SICOFI-4 to the IOM-2 interface and read out under interrupt control. This significantly reduces the load on the microcontroller.

Type	Package
PEB 2465-H	P-MQFP-64-1 (SMD)

Features

- Codec for four analog subscribers (public switch and PBX) usable towards the trunk and the subscriber
- Specification according to relevant CCITT, EIA and LSSGR
- IOM-2 interface
- Usable with transformer and electronic SLICs
- DSP technology
- Adaption to different country specifications with following programmable filters
  – AC impedance matching (return loss better than 30 dB)
  – transhybrid balancing (better than 30 dB)
  – frequency response
  – gain (steps of 0.05 dB)
- Advanced test capabilities
- DTMF generator
- Level metering function
- Boundary scan
- Single 5-V power supply

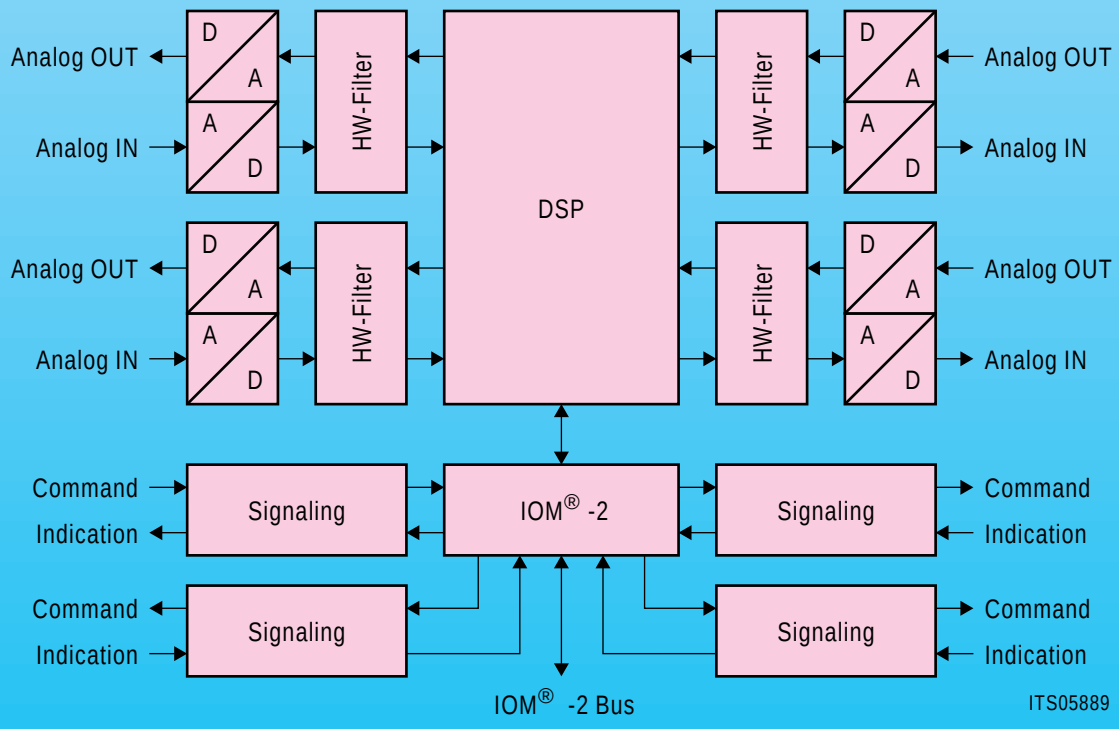
Applications

PBXs:
- 4 analog lines for subscribers and trunks

CO:
- Interface for four analog subscribers

Interfaces

- 4 × t/r interface
- IOM-2 interface
- Eight I/O signaling pins per channel
- Boundary scan



Block Diagram

General Description

The PEB 2466 SICOFI-4 µC, is a programmable codec with filter functions for four channels. Due to an advanced digital filter concept based on a DSP, analog line cards can be easily adopted to different country specifications and SLICs. The device can be directly connected to two PCM highways at flexible data rates. The coefficients to modify gain, frequency response, transhybrid loss and impedance matching are calculated via a specific software (QSICOS) and send to the codec, for each channel individually, via the microcontroller interface.

Applications

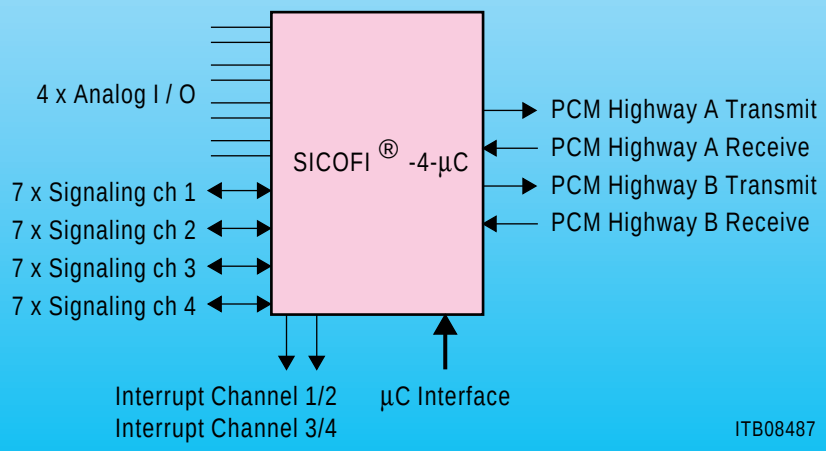
- Analog line cards for CO and PBXs
- Fiber to the curb applications
- Access networks and multiplexers
- Set-top-boxes
- PCM4/PCM8 systems
- Intelligent NTs

.

Type	Package
PEB 2466-H	P-MQFP-64-1 (SMD)

Features

- Four channel single chip codec and filter
- Specifications according to the relevant CCITT, EIA and LSSGR recommendations
- Programmable digital filters for adapting transmission behaviour according to different country specifications
  - AC impedance matching
  - Transhybrid balancing
  - Frequency response
  - Gain
  - a/µ-Law expansion/compression
- Programmable interface to electronic SLICs and transformer solutions
- Two flexible programmable PCM interfaces (data rate from 128 kbit/s up to 8192 kbit/s)
- Serial microcontroller interface
- High analog driver capability (300 Ω, 50 pF)
- Very low power dissipation (typ. 35 mW/channel)
- Two programmable tone generators (DTMF possible)
- Level metering function for testing of analog input signals
- 7 SLIC-signaling interfaces per channel (programmable debouncing)
- Single power supply of 5 V (allows to get rid of the – 5 V supply)
- P-MQFP-64 package



Block Diagram

PEB 3065 (SLICOFI®) General Description

The Signal Processing Subscriber Line Interface Codec Filter SLICOFI is a logic continuation of the well established family of the Siemens DSP Codec-Filter ICs with the vertical integration of all DC-feeding, supervision and PL meterpulse injection features on-chip as well. Fabricated in a standard 1 µm BiCMOS technology the SLICOFI is tailored for very flexible solutions in digital communication systems. For the first time the SLICOFI uses the benefits of a DSP not only for the voice channel but even for line feeding and supervision which leads to a very high flexibility without the need for external components.

Based on an advanced digital filter concept, the PEB 3065 provides excellent transmission performance. The new filter concept leads to a maximum of independence between the different filter blocks. Each filter block can be seen as a one to one representative of the corresponding network element. Together with the software package SLICOS, filter optimizing to different applications can be done in a clear and straight forward procedure. The AC frequency behaviour is mainly determined by the digital filters. Using the new oversampling 1-bit ΣΔ-AD/DA converter, linearity is only limited by second order parasitic effects.

The new – digital – solution of line feeding offers free programmability of feeding current and voltage as well as very fast settling of the DC operating point after transitions. A 0.4-Hz lowpass filter in the DC loop is mainly responsible for the system stability.

Additionally telefax generation and filtering is implemented as well as free programmable (balanced) ring generation with zero crossing injection. Offhook detection with programmable thresholds is possible in all operating modes. To reduce overall power consumption of the line card, the SLICOFI provides a special mode called Power Denial where offhook is done via two high voltage inputs (VLINE) directly connected to the line since the HV-SLIC is switched off.

Type	Package
PEB 3065-N	P-LCC-44-1 (SMD)
PEF 3065-N	P-LCC-44-1 (SMD)

PEB 3065 (SLICOFI®) Features

- Single chip CODEC and FILTER including all LOW VOLTAGE SLIC functions
- Only few external components required
- No trimming or adjustments required
- Specification according to relevant CCITT, LSSGR and DBP recommendations
- Digital signal processing technique
- Advanced low power 1 µm BiCMOS technology
- PCM encoded digital voice transmission (A-Law or µ-Law)
- Four pin serial IOM-2 interface
- High performance A/D and D/A conversion
- Programmable digital filters for
  – impedance matching
  – transhybrid balancing
  – frequency response
  – gain
- Advanced test capabilities
  – integrated line and circuit tests
  – 6 digital loops
  – 5 analog loops
  – two programmable tone generators
- Optimized HV-SLIC interface
- Fully digital programmable DC characteristic
  – programmable constant current from 0 – 70 mA
  – programmable resistive values from 0 – 2 × 500 Ω
- Programmable integrated Teletax injection and filtering during conversation and onhook
  – programmable up to 125 mVrms (5 Vrms at a/b wire) programmable frequency 12/16 kHz
- Polarity reversal (programmable soft or hard)
- Integrated (balanced) ringing generation with zero crossing injection
  – programmable frequency between 16.6 and 70 Hz
  – Programmable amplitude up to 2.125 Vrms (85 Vrms at a/b wire)
- Four operating modes: power-denial, power-down, active and ringing
- Offhook detection with programmable thresholds for all operating modes
- Integrated ring trip detection with zero crossing turn off function
- Ground start and loop start possible
- Integrated checksum calculation for CRAM
- Line card identification
- Also available with extended temperature range – 40 °C to 85 °C (PEF 3065-N)

PEB 4065 (HV-SLIC) General Description

The High Voltage Subscriber Line IC PEB 4065 is a rugged and reliable interface between the telephone line and the SLICOFI, a low voltage Subscriber Line Interface and Codec Filter IC. The PEB 4065 is fabricated in a Smart Power Technology offering a breakthrough voltage of at least 170 V.

The PEB 4065 provides battery feeding between – 24 V and – 80 V and internal ringing injection with a differential ring voltage up to 85 Vrms. In order to achieve these high amplitudes an auxiliary positive battery voltage is used during ringing. This voltage can also be applied in order to drive very long telephone lines.

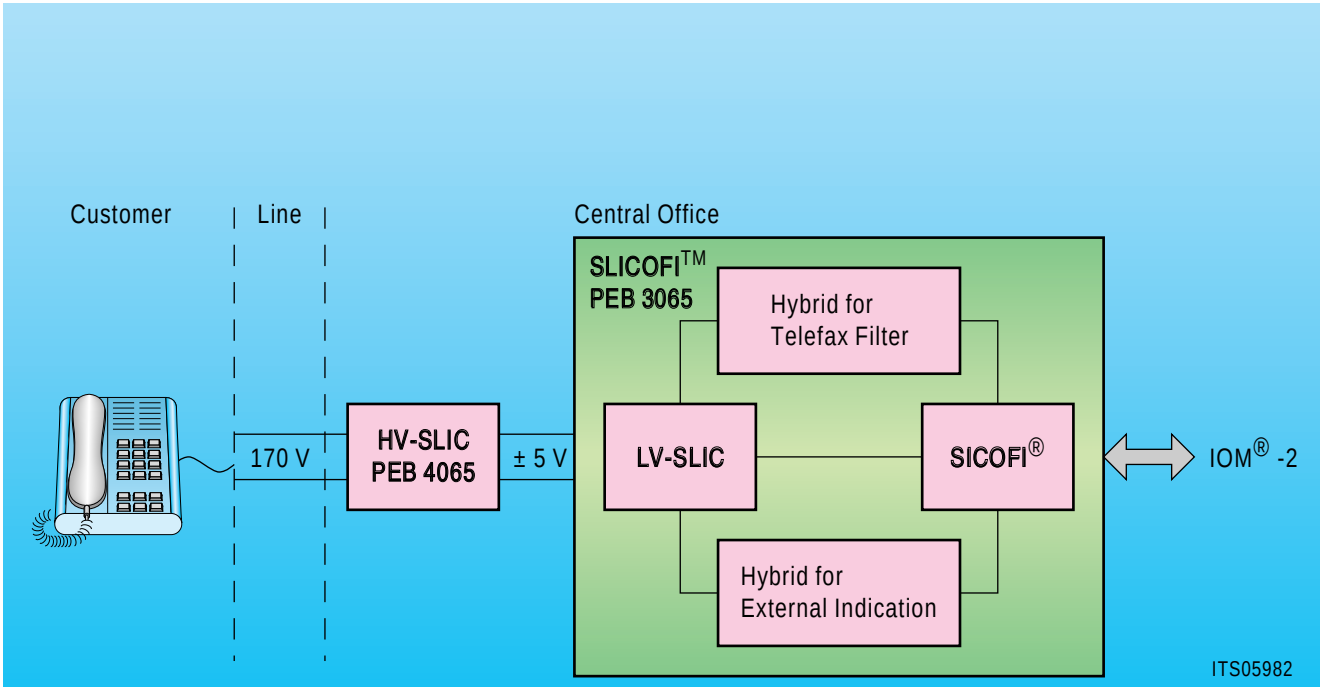
The HV-SLIC is designed for a voltage feeding current sensing line interface concept and provides sensing of transversal and longitudinal current on both wires.

There is a power-down mode reducing power consumption while providing all supervision functions and a power-denial mode where the device is switched off turning the line outputs to a high impedance state.

Type	Package
PEB 4065-T	P-DSO-20-5 (SMD)
PEF 4065-T	P-DSO-20-5 (SMD)

PEB 4065 (HV-SLIC) Features

- High voltage line feeding
- Internal ring and metering signal injection
- Sensing of transversal and longitudinal line current
- Reliable 170 V Smart Power Technology
- Battery voltage – 24 V…– 80 V
- Boosted battery mode for long telephone lines and up to 85 Vrms balanced ringing
- Polarity reversal
- Small P-DSO-20-5 power package
- Also available with extended temperature range – 40 °C to 85 °C (PEF 4065-T)



Block Diagram

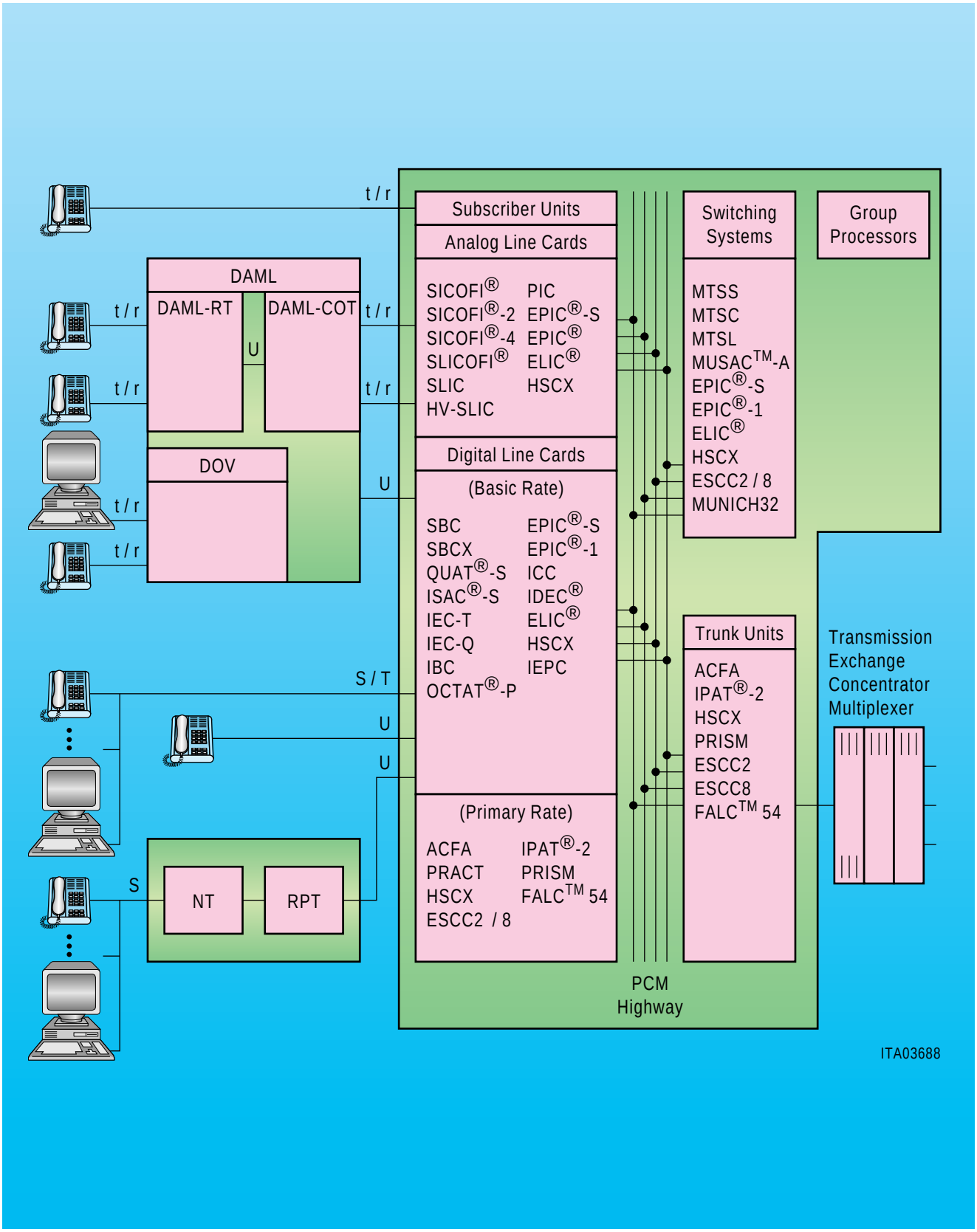
ISDN Echo Cancellation Circuit
IEC-Q; PEB 2091

Digital Line Cards

Product Overview

Type	Short Title	Function	Page
PEB 2026 PEF 2026	IHPC	ISDN High Voltage Power Controller	106
PEB 2070	ICC	ISDN Communications Controller	107
PEB 2075	IDEC®	ISDN D-Channel Exchange Controller (4 channel)	109
PEB 2080	SBC	S-Bus Interface Circuit	110
PEB 2081	SBCX	S/T-Bus Interface Circuit Extended	111
PEB 2084	QUAT®-S	Quadruple Transceiver for S/T Interfaces	112
PEB 2091	IEC-Q	ISDN Echo Cancellation Circuit (2B1Q-line code)	113
PEB 20901 PEB 20902	IEC-T	ISDN Echo Cancellation Circuit (4B3T-line code)	114
PEB 24901	Quad IEC DFE-T	Quad ISDN Echo-Cancellation Digital Front End (4B3T)	116
PEB 24902 PEF 24902	Quad IEC AFE	Quad ISDN Echo-Cancellation Circuit Analog Front End	117
PEB 24911 PEF 24911	Quad IEC DFE-Q	Quad ISDN Echo-Cancellation Digital Front End (2B1Q)	118
PEB 2095	IBC	ISDN Burst Transceiver Circuit	119
PEB 2096	OCTAT®-P	Octal Transceiver for U_{PN} interfaces	120
PEB 2025	IEPC	ISDN Exchange Power Controller	121
PEB 20560	DOC	DSP Oriented PBX Controller	122
PEB 2054	EPIC®-1	Extended PCM Interface Controller	90
PEB 2055	EPIC®-S	Extended PCM Interface Controller-Small	91
PEB 20550	ELIC®	Extended Line Card Interface Controller	92
SAB 82525 SAB 82526	HSCX HSCX1	High-Level Serial Communication Controller Extended	162
PEB 2085 PEB 2086	ISAC®-S	ISDN Subscriber Access Controller	61

Digital Exchange Systems
General Overview on Architecture and Devices



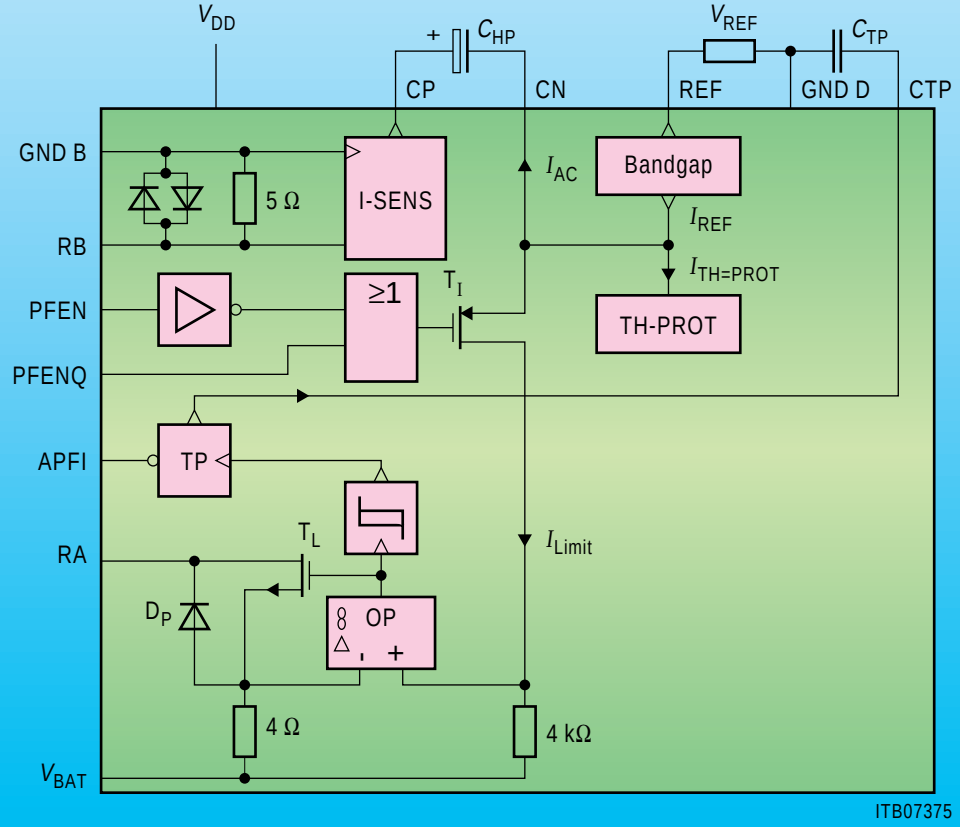
General Description

The IHPC is an integrated power controller especially designed for feeding two-wire ISDN-transmission lines. One line can be powered by one IHPC. An external resistor defines the value of the current-limit for the line. Powering can be switched on or off by the logic inputs “PFEN” and “PFENQ”. With a logic low at the “APFI” output the IHPC signals that current-limiting is active; this signal is low-pass filtered. An external capacitor defines the corner frequency of this low-pass filter and the resulting delay time respectively. A second external capacitor is needed to make sure that longitudinal disturbance (AC) will not produce a current limiting effect. Line current-limiting and reducing this limiting level in case of overtemperature guards the IHPC against overloads.

Type	Package
PEB 2026T-P	P-DSO-20-10 (SMD)
PEB 2026T-S	P-DSO-20-6 (SMD)
PEF 2026T-P	P-DSO-20-10 (SMD)
PEF 2026T-S	P-DSO-20-6 (SMD)

Features

- Battery voltage up to 130 V
- Supplies power for one transmission line
- Current limiting and chip temperature control
- Limiting current can be programmed by an external resistor
- Automatically reduced feeding current in case of overtemperature
- Reliable 170 V Smart Power Technology (SPT 170)
- Small P-DSO-20 package



Block Diagram

General Description

While the IOM structure supports high flexibility with respect to layer-1 of data transmission, the ISDN communications controller can be used in all applications for link access protocol control. This is of great importance regarding production volume, software continuity and engineering effort necessary for the use of the complex circuit. For further reduction of software, high-level layer-2 support has been a main target of circuit definition.

D-channel protocol handling is the main task of the ICC. Its characteristic features are determined by an on-chip LAPD controller and a sophisticated FIFO-structure. The LAPD controller performs multiframe operation largely autonomously with a window size of 1. All S- and I-frames, including the address and control fields, are evaluated in the ICC. Depending on the status of the controller, positive or negative acknowledgements are generated without interrupting the CPU. When the procedure is terminated, an interrupt status is generated to inform the CPU of the status of the procedure. To enable the ICC device to be used in complex protocol applications with window size of up to 7, a transparent mode is implemented. In this mode the layer-2 headers are transferred transparently to the CPU.

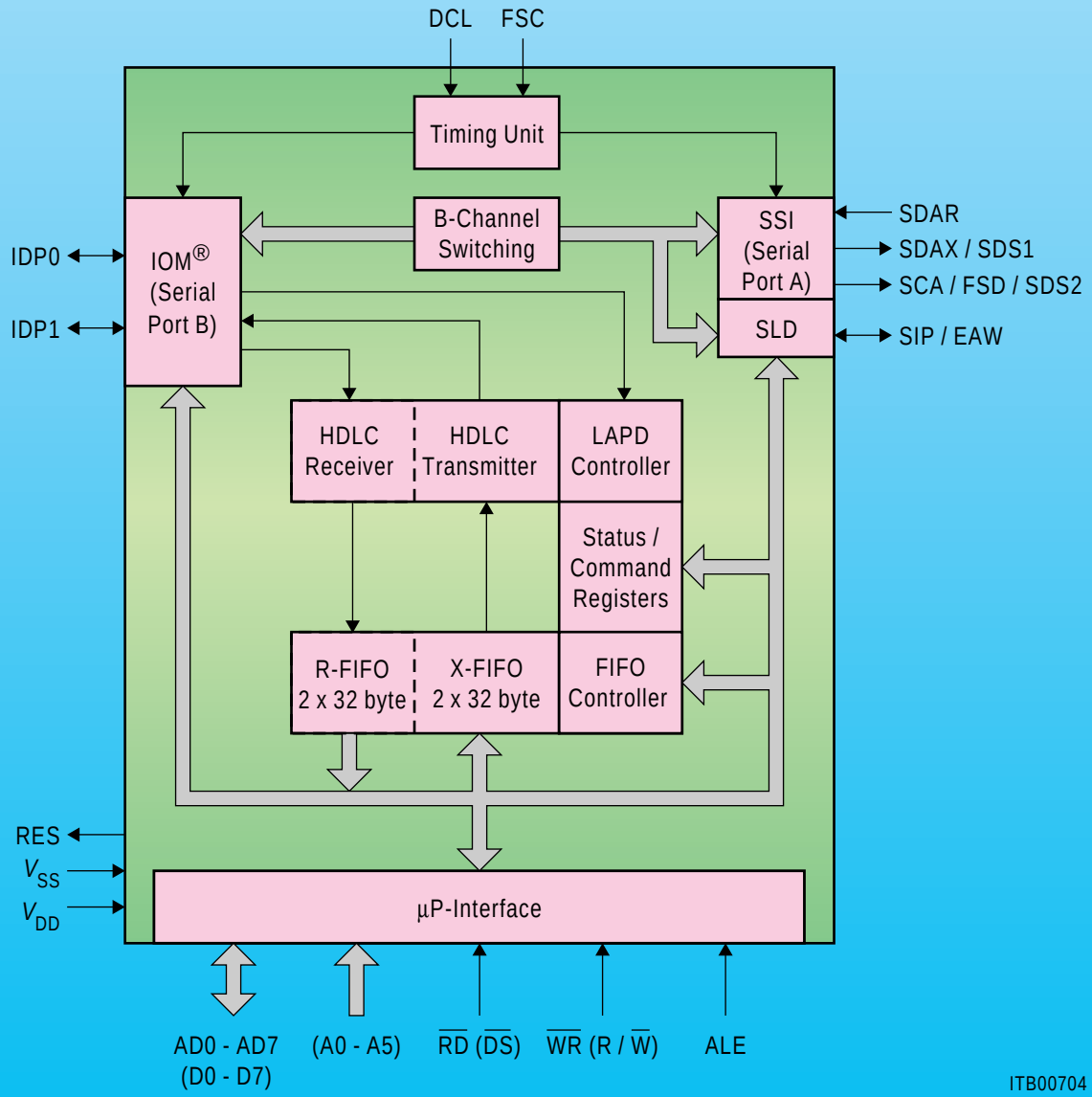
The synchronization of the 16-kbit/s D-channel with the CPU-bus is performed by buffers with a capacity of 64 bytes per direction. Sophisticated buffer controllers allow overlapping input/output operation, which ensures that the maximum packet length is not limited by the buffer size.

This feature greatly reduces the dynamic load of the microprocessor system.

Type	Package
PEB 2070-N	P-LCC-28-1 (SMD)
PEB 2070-P	P-DIP-24-1 (not for new designs)
PEF 2070-N	P-LCC-28-1 (SMD)

Features

- High-level support of LAPD-protocol
- FIFO-buffer (64 bytes per direction) for efficient transfer of D-channel messages
- IOM interface compatible (IOM-1 or IOM-2)
- Standard parallel microprocessor interface
- Support of activation/deactivation procedure
- Variety of operating modes
- µP access to B-channels and IOM-intercommunication channels
- Control of peripheral devices via IOM Monitor and C/I-channel protocols
- 2-µm CMOS technology and low power consumption:
  Standby: 2 mW
  Active: 4 mW at 512 kHz



Block Diagram

General Description

With the IOM-2 interface, designers have more flexibility with respect to handling of D-channel information. Layer-1 transceivers are connected over the IOM-2 interface directly to either the PEB 2055 (EPIC-1) or the PEB 2054 (EPIC-S).

These devices are capable of switching not only the B-channels but also the D-channel. Thus, the designer can decide whether he wants to process D-channel signaling information decentralized, on the line card, or pass it through to be processed centrally.

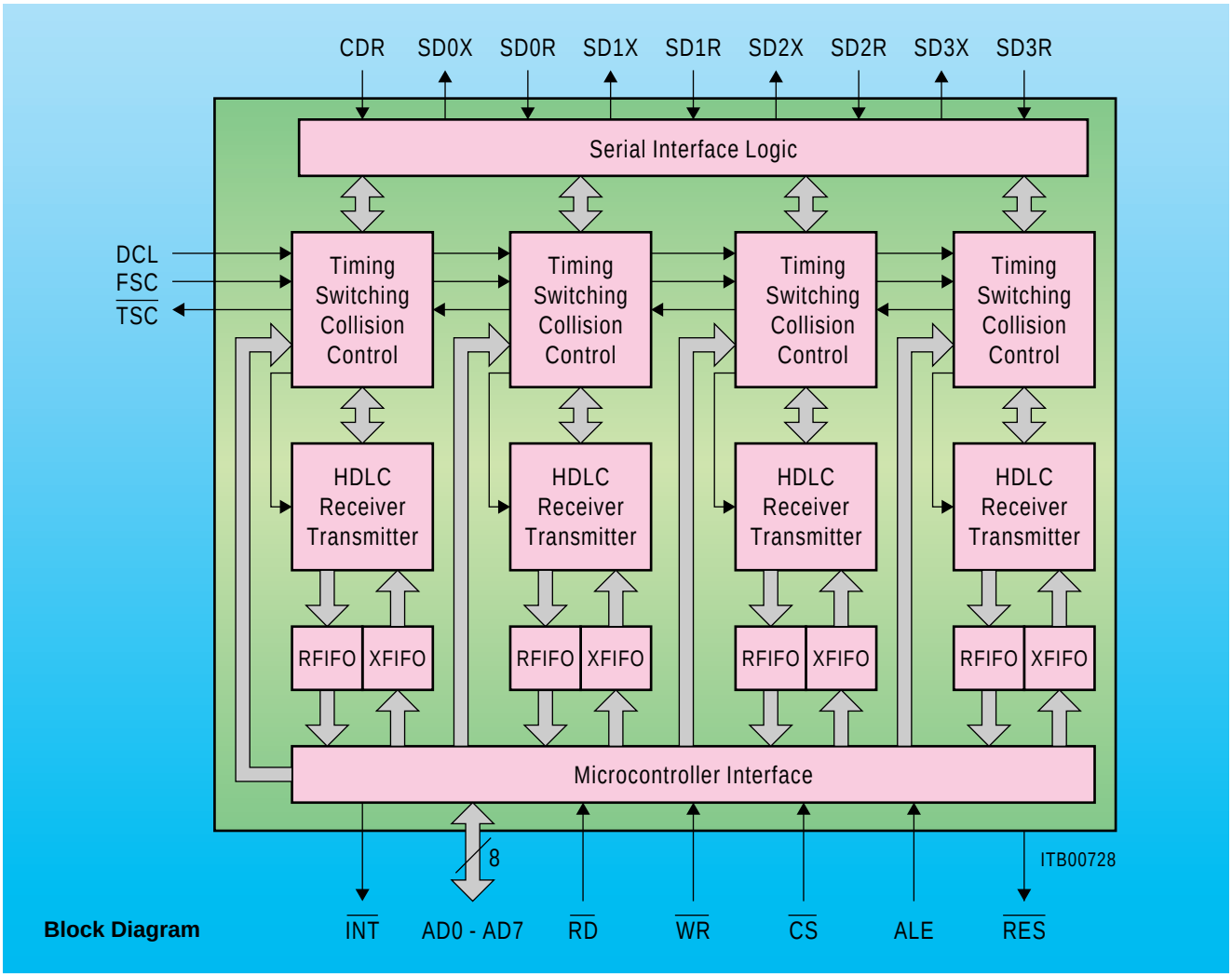
The IDEC has been optimized for processing the D-channel signaling information on digital exchange line cards. Four independent HDLC controllers have been implemented on a single IC. Thus, one IDEC can handle the D-channels of up to four subscriber lines.

The IDEC is based on the same core architecture as the PEB 2070 ICC, but has been optimized for exchange line cards and then repeated four times.

Type	Package
PEB 2075-N	P-LCC-44-1 (SMD)
PEB 2075-P	P-DIP-28-1 (not for new designs)
PEF 2075-N	P-LCC-44-1 (SMD)

Features

- Four independent HDLC channels
- 64-byte FIFO buffering per channel and direction
- Handling of basic HDLC functions
- Single or quad connection to serial transmission lines
- IOM- or PCM interfaces
- Programmable time-slots and channel data rates (up to 4 Mbit/s)
- Collision detection and resolution circuitry for shared time-slots
- 8-bit parallel µP interface with vector interrupt
- Advanced low power CMOS technology: 50 mW



Block Diagram

ISDN Layer-1 Transceivers

S-Bus Interface Circuit (SBC)

General Description

The four-wire S-interface between subscriber terminals and network termination has been standardized by CCITT recommendation I.430. Making use of a passive bus which provides separate receiver and transmit loops operating at 192-kbit/s, up to eight terminals can be connected to the network termination. In case more than one terminal want to access the bus at the same time, a procedure is provided for resolving the collision problem. Since all layer-1 functions such as frame structure, data rate, power feeding, transceiver characteristics, activation/deactivation and subscriber access procedure are well defined, the S-bus can be considered an important tool for standardization of data communication equipment. It supports connections with a maximum length of 1 km in a point to-point and 150 m in a point-to-multipoint bus configuration.

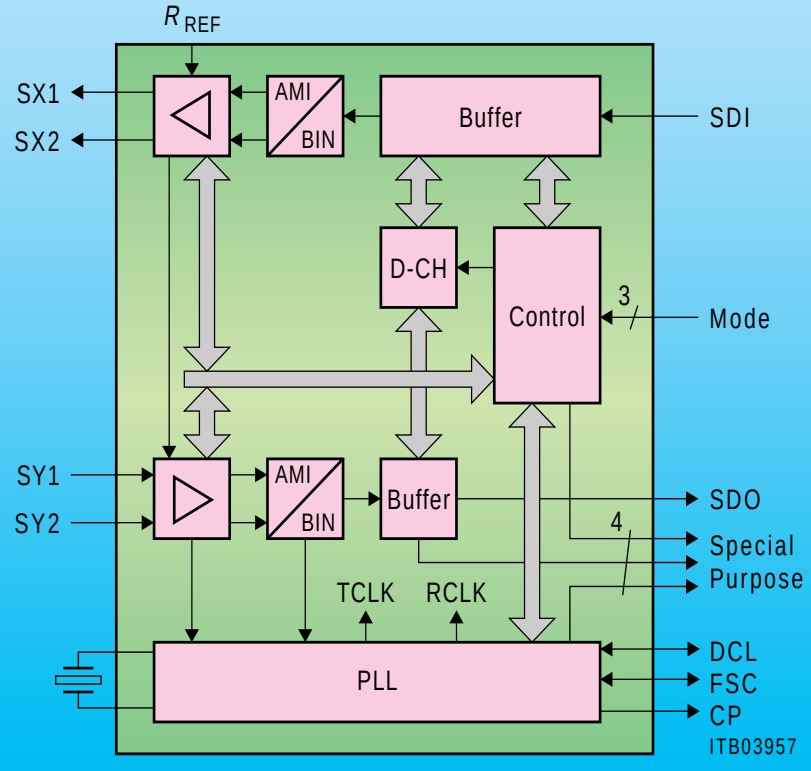
The SBC is designed to meet all CCITT requirements, and, moreover, implements additional features necessary in specific applications. The device contains the transceiver function, timing recovery for the different modes of operation, circuitry for the collision resolution function and a state control block to handle the activation/deactivation procedures autonomously without the support of a microprocessor. A flexible buffer structure performs the frame-alignment function in PBX-trunk applications, where the system clock deviates from the central office clock derived from the line. Matching of the actual line attenuation is supported by receiver circuitry which contains adaptively adjustable thresholds.

Type	Package
PEB 2080-N	P-LCC-28-1 (SMD)
PEB 2080-P	P-DIP-22-1 (not for new designs)
PEF 2080-N	P-LCC-28-1 (SMD)

Not for new development.
For new development use the SBCX (PEB 2081)

Features

- S-bus transceiver according to CCITT I.430
- Recovery of clock and frame signals in different modes of application.
- Frame alignment for trunk module application
- IOM interface compatible (IOM-1)
- Handling of command/indication information during the activation/deactivation procedure
- Switching of test loops
- Control of bus access by echo-bit handling
- Wake-up unit for activation from power-down state
- Several operating modes including trunk applications with frame alignment
- 2-µm CMOS technology and low power consumption:
  Standby: 4 mW
  Active: max. 60 mW at 512 kHz



Block Diagram

General Description

The PEB 2081 S/T-Bus Interface Circuit Extended (SBCX) implements the four-wire S/T interface used to link voice/data ISDN terminals, network terminators (NT) and PBX-trunk lines to a Central Office exchange. The components switches B- and D-channels between the S/T and the ISDN Oriented Modular (IOM-2) interfaces, the latter being a standard backplane interface for the ISDN-basic access. The SBCX exceeds both the electrical and functional requirements of the S/T interface in order to provide high flexibility to the user.

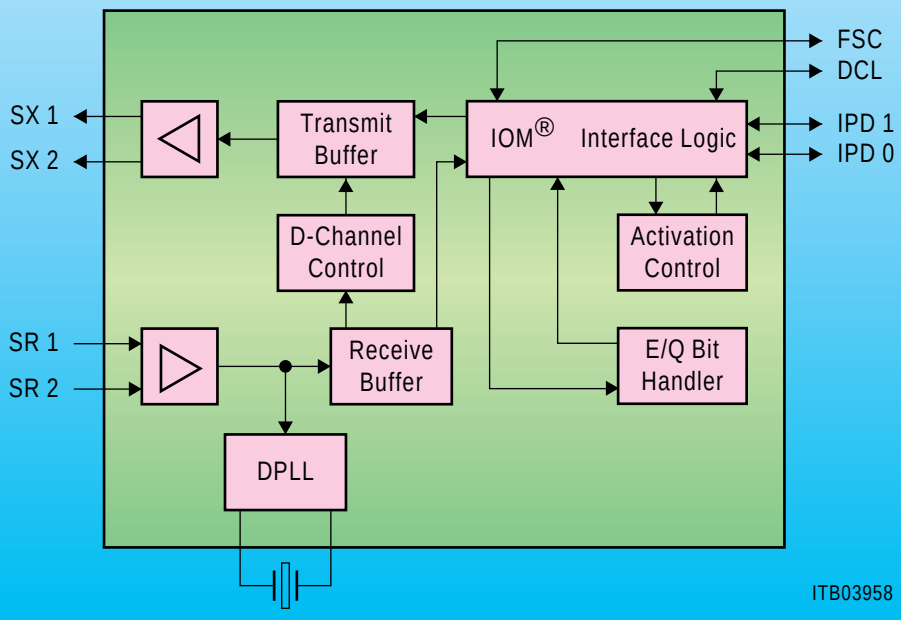
Applications

- Network terminators (NT and NT2)
- S_0 multiplexer cards
- S_0 line cards for ISDN-trunk lines
- Voice/Data Terminals, ISDN-PC Cards

Type	Package
PEB 2081-N	P-LCC-28-1 (SMD)

Features

- 1-channel S/T transceiver
- Full duplex 2+D S/T transceiver according to CCITT I.430
- Extended loop length up to 2 km
- Activation and deactivation procedures according to CCITT I.430
- Fully compliant NT2 trunk mode including multipoint operation
- Frame alignment with absorption of phase wander in NT2 network side applications
- Receive timing recovery for point-to-point, passive bus and extended passive bus configuration
- Access to S- and Q-bits of S/T interface (S1-, S2- and Q-channel)
- D-channel access control also in trunk applications
- Execution of test loops
- Conversion of frame structure between S/T interface and IOM-2
- Advanced CMOS technology with low power consumption (standby < 6 mW, active 80 mW)



Block Diagram

General Description

The PEB 2084, QUAT-S, implements 4 × four-wire S/T interfaces used to link ISDN terminals to PBXs or PBX to NTs. The component switches B- and D-channels between the S/T and the ISDN Oriented Modular (IOM-2) interfaces, the latter being a standard backplane interface for the ISDN-basic access. Each of the four S/T-channels implemented in the device can be individually assigned for S_0- or T interface.

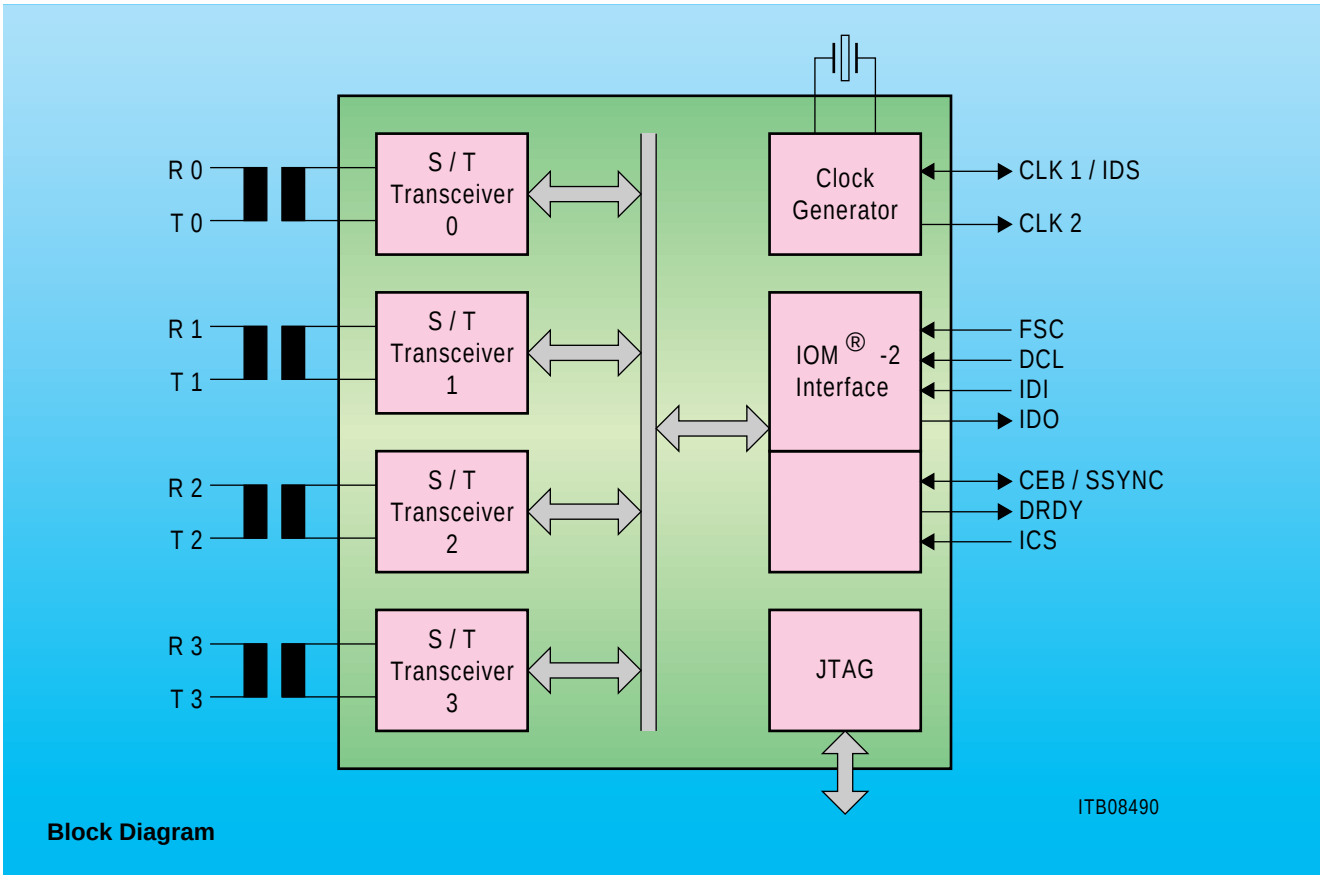
Applications

- Digital line cards for ISDN subscribers
- Digital line cards for ISDN-trunk lines
- Multiplexers
- Set-top-boxes

Type	Package
PEB 2084-H	P-MQFP-44-1 (SMD)

Features

- 4-channel S/T transceiver
- Full duplex 2B+D S/T transceiver according to CCITT I.430, ETSI 300.012 and ANSI T1.605
- Receive timing recovery according to selected operating mode
- Conversion of frame structure between S/T interface and IOM-2
- Access to S- and Q-bits of S/T interface
- Execution of test loops
- Support of star configurations (external common echo bit)
- Support of D-channel collision resolution in trunk mode
- Full support of arbiter concept of the ELIC (PEB 20550)
- Support of synchronization of cordless applications
- Low power consumption (< 100 mW)
- Loop length > 1.5 km
- JTAG-boundary scan test interface
- P-MQFP-44 package



Block Diagram

General Description

The PEB 2091, IEC-Q, is a single chip full-duplex U-transceiver device meeting the latest American- (ANSI) and European (ETSI) specifications. It is based on a coding scheme reducing two binary information into a single quaternary code. This coding requires a reduced transmission rate of only 80 kbaud on a twisted copper pair, minimizing signal attenuation and guaranteeing the highest transmission rate of all defined U-interface standards.

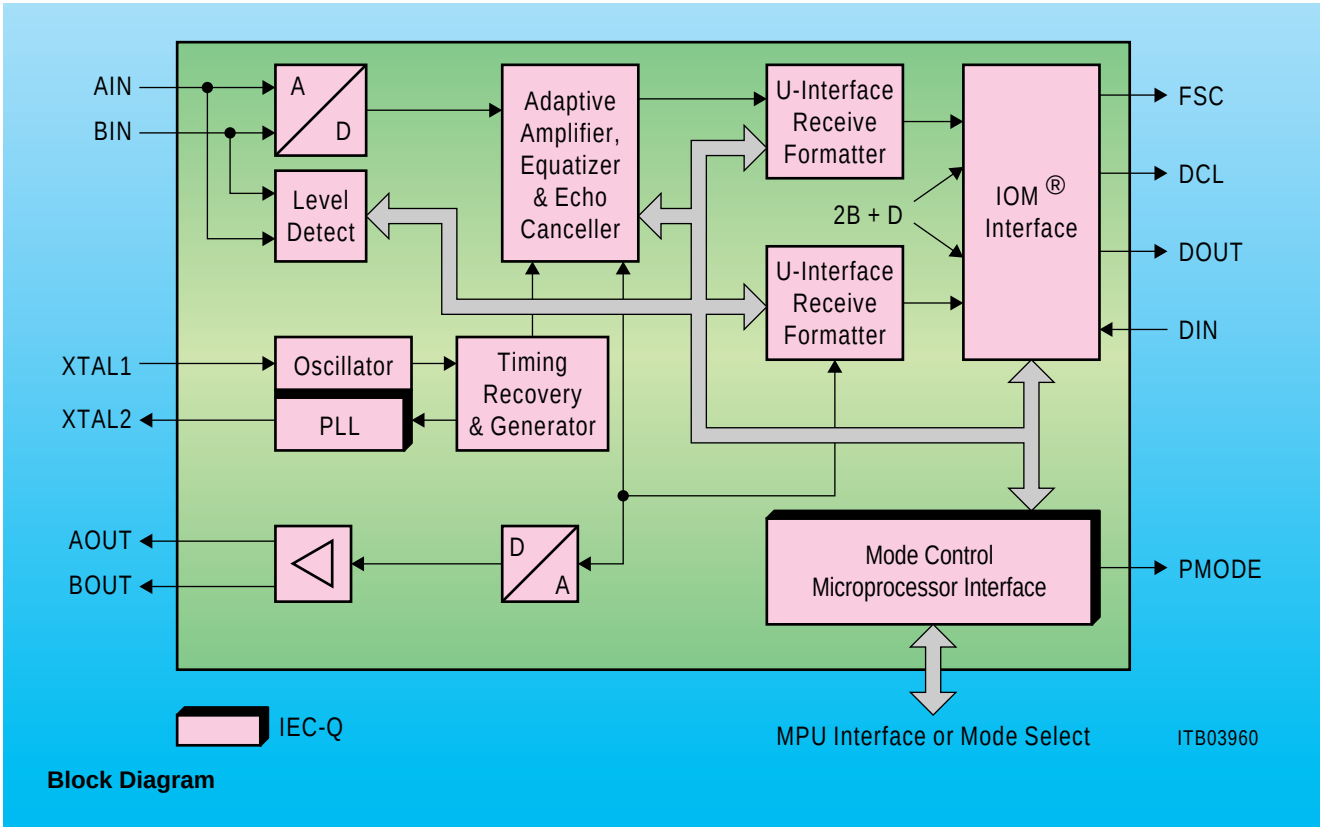
The PEB 2091 was defined to operate in all ISDN (Line cards, Network Terminators, Terminals, PBXs and Repeaters) and non-ISDN (DAML) applications.

Features

- Full-duplex two-wire U-transceiver meeting the following layer-1 specifications:
  ANSI T1.601-1991
  CNET ST/LAA/ELR/DNP/822
  ETSI DTR/TM 3002
  Recommendation CCITT, G961
- 144-kbit/s user bit rate (2B+D)
- 160-kbit/s total bit rate including maintenance and synchronization
- Low transmission frequency of 80 kbaud by using the 2B1Q-block line code
- IOM interface compatible
- Adaptive echo cancellation and equalization using digital filtering

Type	Package
PEB 2091-N	P-LCC-44-1 (SMD)
PEF 2091-N	P-LCC-44-1 (SMD)

- Recovery of clock and frame signals from
- the data stream
- Handling of command/indication information during activation/deactivation procedure
- Switching of test loops
- Wake-up unit for activation from power-down state
- Several operating modes including trunk applications with frame alignment (LT, NT, TE, Repeater)
- Transmission range of 5.5 km (18 kft) with 0.4 mm (26 AWG) wire
- U-only activation
- Power feeding control
- Repeater mode
- Echo overload compensation to match ETSI and ANSI test loops
- Dynamic phase adaptation
- 1-µm CMOS technology standby: 70 mW
  active: 350 mW



Block Diagram

General Description

The most challenging requirement in ISDN is full-duplex transmission at a data rate of 144 kbit/s over the existing twisted-pair telephone cables (U-interface). Among several approaches for solving this problem, ping-pong time-compression multiplexing and echo cancellation have been proposed as most suitable for VLSI implementation. Moreover, echo cancellation has proven to be the best method for public lines which typically reach lengths in the range of 8 km.

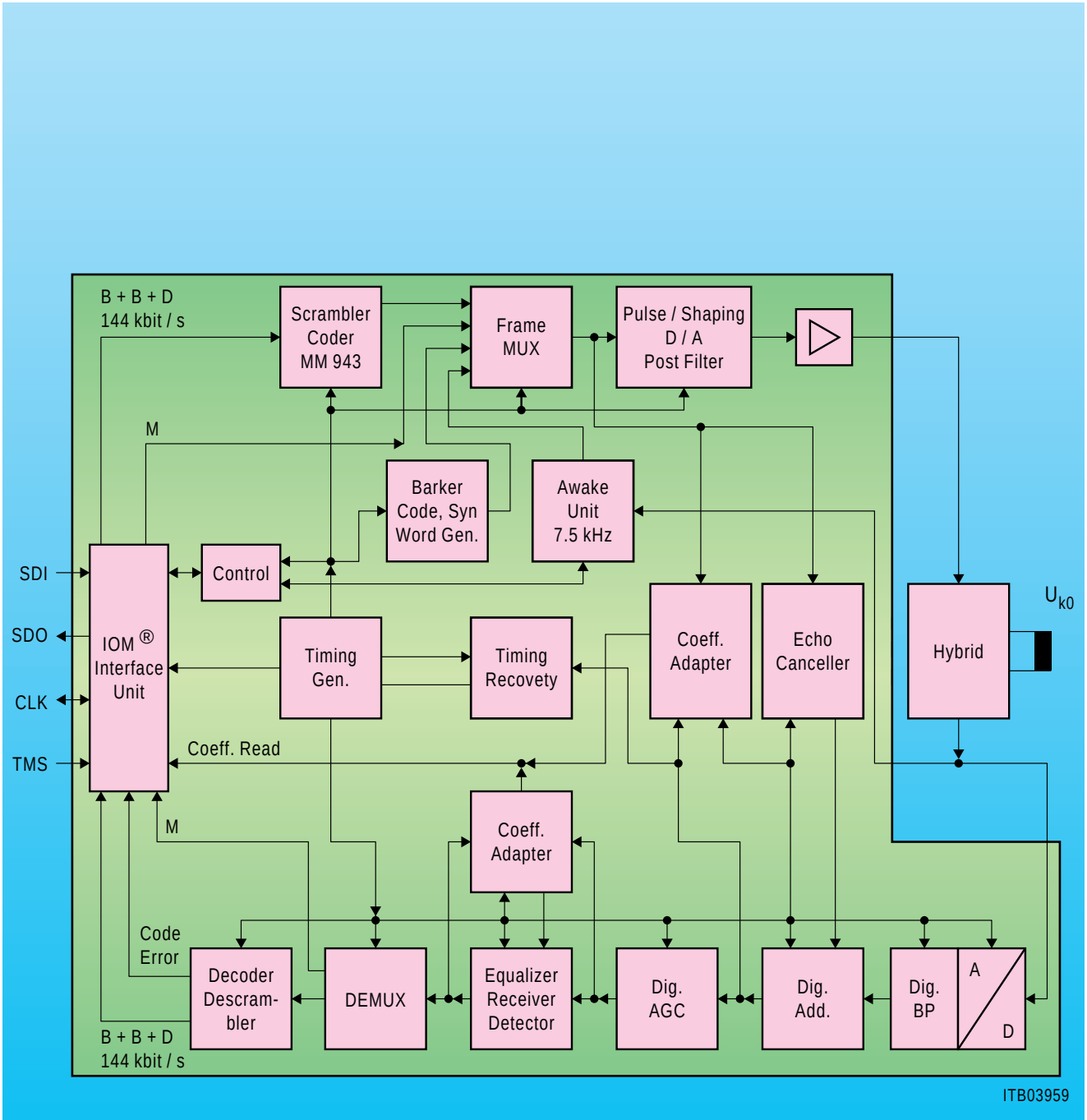
After a careful study of different transmission codes, a 4B3T block code was chosen for the IEC-T which make use of ternary coding of the binary information. A particular advantage of this code is its low frequency, DC-free performance spectrum with its energy peak at about 40 kHz. In this context, for a bit rate of 160 kbit/s the required baud rate is as low as 120 kHz. As a result transmission systems benefit from, low line attenuation low crosstalk distortion and high possible signal levels without causing EMI-problems.

The IEC-T is offered as a two chip solution consisting of:
- Digital part, called PEB 20901
- Analog part, called PEB 20902

Type	Package
PEB 20901-N	P-LCC-44-1 (SMD)
PEB 20901-P	P-DIP-40-1 (not for new designs)
PEF 20902-N	P-LCC-28-2 (SMD)
PEB 20902-P	P-DIP-24-1 (not for new designs)
PEF 20901-N	P-LCC-28-2 (SMD)
PEF 20902-N	P-LCC-28-2 (SMD)

Features

- Full-duplex two-wire U-transceiver
- 144-kbit/s user bit rate (2B+D)
- 160-kbit/s total bit rate including maintenance and synchronization
- Low transmission frequency of 120 kbaud by using the 4B3T-ternary block code
- Adaptive echo cancellation and equalization using digital filtering (DSP)
- Recovery of clock and frame signals from the data stream
- IOM-1 interface compatible
- Transmission range up to 8 km with 0.6-mm wires
- Handling of command/indication information during activation/deactivation procedure
- Switching of test loops
- Wake-up unit for activation from power-down state
- Several operating modes including trunk applications with frame alignment
- 2-µm CMOS technology for PEB 20902, 1-µ technology for PEB 20901
- 320-mW power consumption
- Repeater mode with no external devices



Block Diagram

Advanced Information

General Description

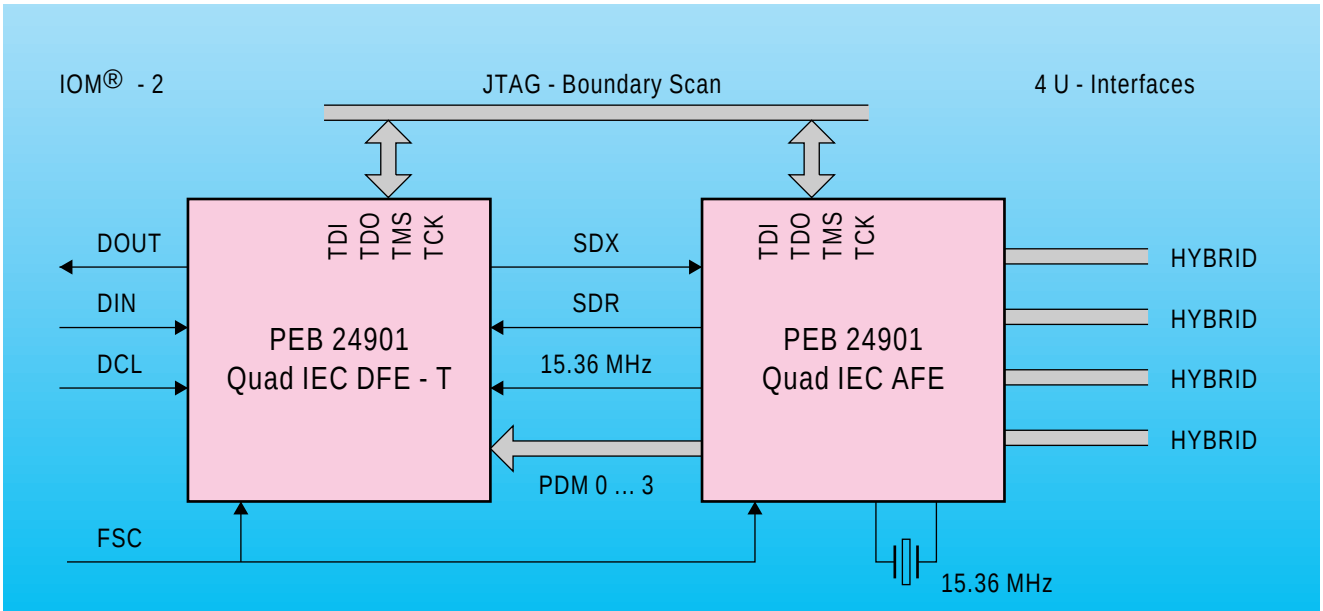
The PEB 24901 4 Channel ISDN Echocancellation Digital Front End (Quad IEC DFE-T) is the digital part of an optimized ISDN 4B3T U-interface line card chip set. It features 4 independent digital signal processors providing, in conjunction with the PEB 24902 ISDN Quad Analog Front End (Quad IEC AFE), full duplex data transmission at the U_{k0}-reference point according to FTZ Guideline 1TR 220, ETSI ETR80 and CCITT I.430 standards. The PEB 24901/ 24902 chip set is based on the PEB 20901/20902 IEC-T ISDN U-transceiver chip set. The PEB 24901 comes in a P-MQFP-64 package.

Features

- Full duplex transmission and reception of the U_{k0}-interface signals according to the FTZ Guideline 1 TR 220 of the Deutsche Bundespost Telekom (DBPT).
  - 144-kbit/s user bit rate over standard local telephone loops
  - 1-kbit/s maintenance channel for transmission of data loop back commands and detected transmission errors
  - 4B3T-ternary block code (subscriber line symbol rate 120 kbaud)
  - Monitoring of transmission errors
  - Subscriber loop length without repeater:
    up to 4.2 km on 0.4 mm wire
    up to 8.0 km on 0.6 mm wire
- Adaptive echo-cancellation
- Adaptive equalization
- Automatic polarity adaption

Type	Package
PEB 24901	P-MQFP-64-1 (SMD)

- Clock recovery (frame and bit synchronization)
- Transposition of ternary to binary data and vice versa (coding, decoding, scrambling, descrambling, phase adaption)
- Built-in wake-up unit for activation from power-down state
- Acvtivation and deactivation procedure according to CCITT I.430 and to FTZ Guideline 1 TR 210 of the DBPT
- Optimized for working in conjunction with telecom ICs as the IDEC (PEB 2075), EPIC (PEB 2055) and ELIC (PEB 20550) via IOM-2 interface
- Data speed conversion between the U_{k0} frames and the IOM-2 frames. Absorption of received phase-wander of up to 18 µs peak-to-peak (CCITT Rec. Q.512)
- Handling of commands and indications contained in the IOM-2 C/I-channel for activation, deactivation, supervision of power supply unit and equipment for wire testing
- IOM-2 system interface
- Data availability via the Monitor channel:
  - Accumulated RDS-transmission errors for the whole U_{k0} link
  - Echo canceller coefficients and status values, which can be used to indicate the state of the U_{k0} interface
- Switching of an analog test loop at the U_{k0} interface for testing (loop in LT)
- Remote control of test loop switching via maintenance channel
- 4 relay driver pins per port addressable by Monitor command
- 2 status pin per port reporting to the Monitor channel
- JTAG-boundary scan path



Four Channel LT Application

Advanced Information

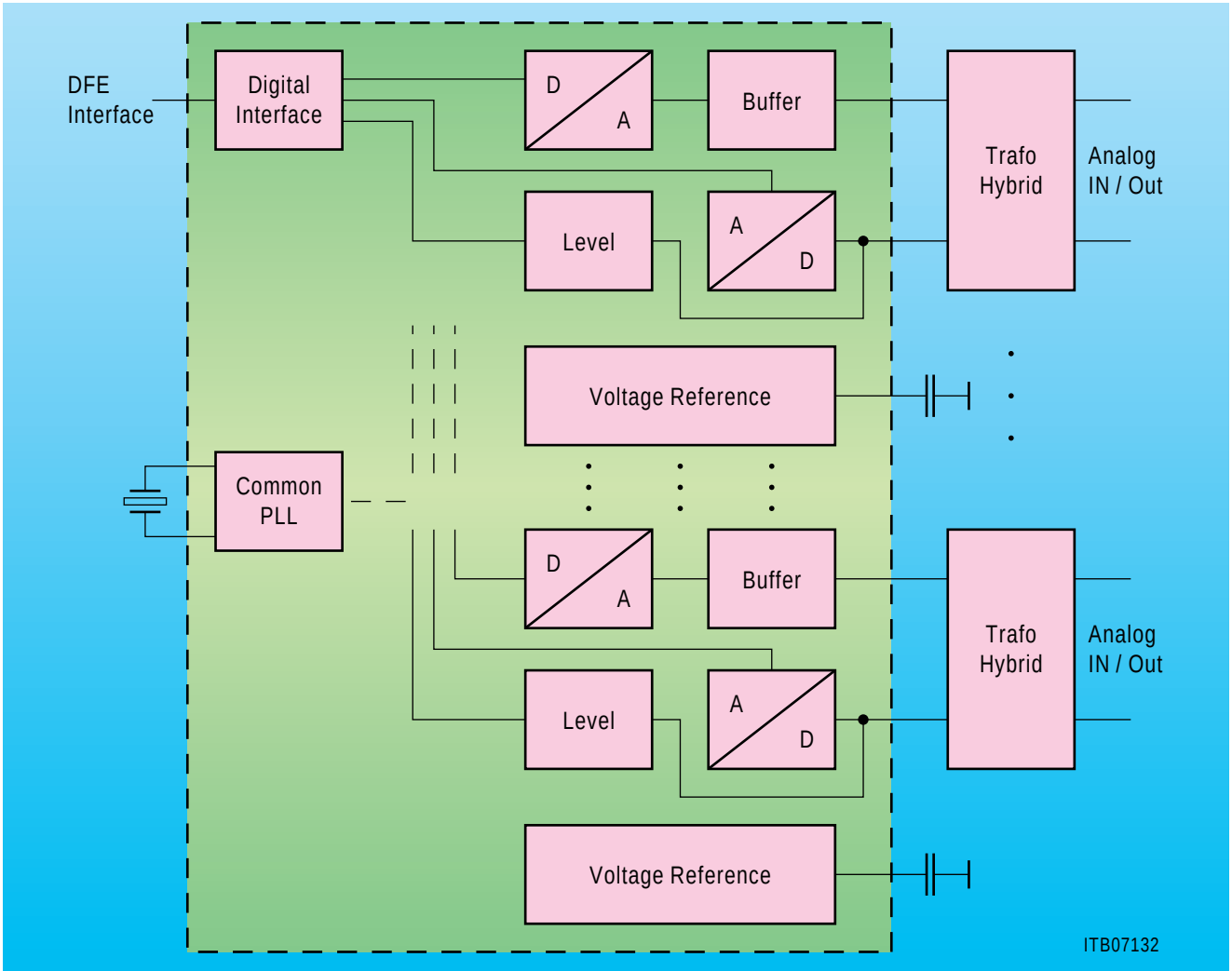
General Description

The PEB 24902 Quad IEC AFE (Quadruple ISDN Echocancellation Circuit Analog Front End) is part of a 2B1Q or 4B3T ISDN U-transceiver chip set. Up to four lines can be accessed simultaneously by the Quad IEC AFE. The Quad IEC AFE is optimized to work in conjunction with the PEB 24901 Quad IEC DFE-T and the PEB 24911 Quad IEC DFE-Q. An integrated PLL synchronizes the 15.36-MHz master clock onto the 8-kHz or 2048-kHz PTT clock. This specification describes the functionallity for 2B1Q and 4B3T interfaces.

Type	Package
PEB 24902	P-MQFP-64-1 (SMD)
PEF 24902	P-MQFP-64-1 (SMD)

Features

- Digital to analog conversion (transmit pulse)
- Output buffering
- Analog to digital conversion
- Detection of signal on the line
- Master clock generation by PLL
- P-MQFP-64 package
- Compliant to ANSI T1.601 (1992), ETSI ETR 080 (1995)
- JTAG-boundary scan path compliant to IEEE 1149.1
- Extended temperature range – 40 °C to 85 °C available (PEF 24902)



Block Diagram

Advanced Information

General Description

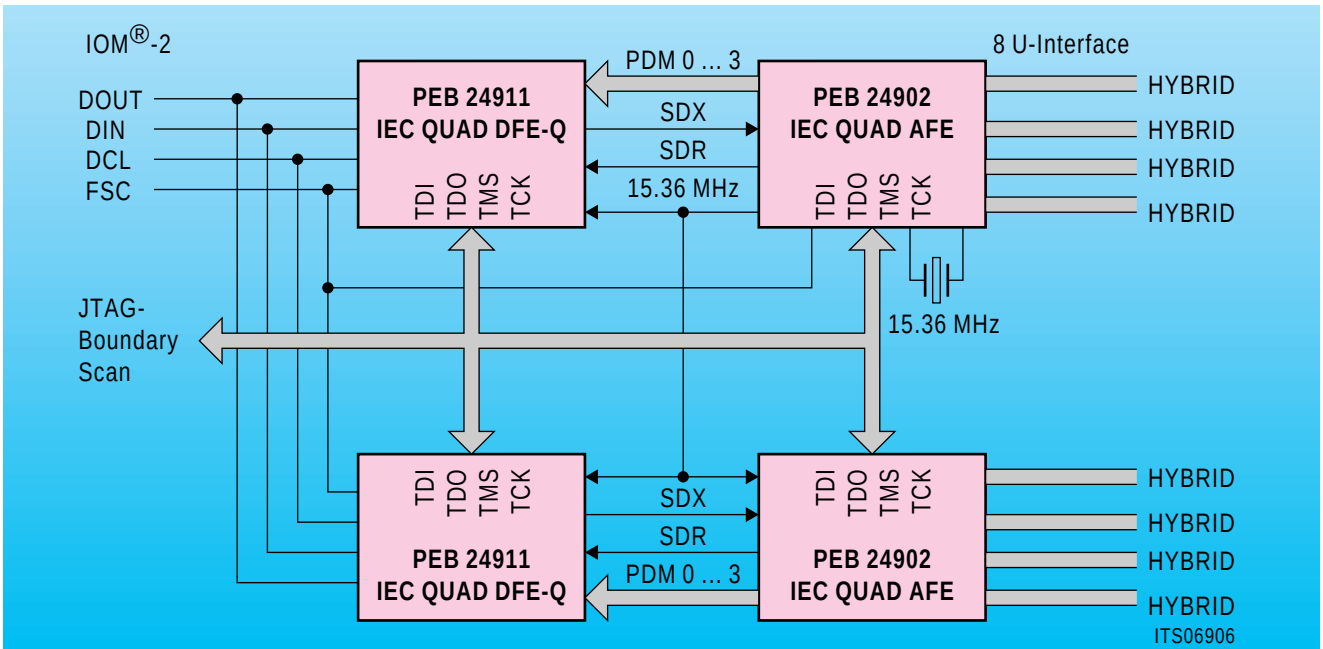
The PEB 24911 Quad ISDN 2B1Q Echocanceller Digital Front End (Quad IEC DFE-Q) is the digital part of an optimized ISDN 2B1Q U-interface line card chip set. It features 4 independent digital signal processors providing, in conjunction with the PEB 24902 ISDN Quad Analog Front End, full duplex data transmission at the U_{k0}-reference point according to ANSI T1.601, ETSI ETR80, CCITT G.961 and CNET ST/LAA/ELR/DNP/822 standards. The PEB 24911/ PEB 24902 chip set is based on the PEB 2091 IEC-Q V4.4 single chip ISDN U-transceiver. The IEC-Q V4.4 is approved by Bellcore. The PEB 24911 comes in a P-MQFP-64 package.

Features

- Full duplex transmission and reception at the U-reference point compliant to:
  ANSI T1.601-1992,
  CNET ST/LAA/ELR/DNP/822,
  ETSI ETR 080 1993.
- Recommendation CCITT, G.961
- 144-kbit/s user bit rate over a two-wire subsriber loop
- 2B1Q-block code (2 binary, 1 quaternary)
- 80-kHz symbol rate
- Activation and deactivation procedure
- Meets transmission requirements for loop #1 through loop #15 of ANSI‘s 15 telephone plant test loops
- Meets transmission requirements for loop #1 through #6 of CNET’s 6 telephone plant test loops

Type	Package
PEB 24911	P-MQFP-64-1 (SMD)
PEF 24911	P-MQFP-64-1 (SMD)

- Meets transmission requirements for loop #1 through #8 of ETSI’s 8 telephone plant test loops
- Built-in wake-up unit for activation from power-down state
- Adaptive echo-cancellation
- Adaptive equalization
- Automatic polarity adaption
- Clock recovery (frame and bit synchronization) in all applications
- Automatic gain control
- Low power consumption
- Extended temperature range – 40 °C to 85 °C available (PEF 24911)
- U-interface propagation delay measurement with better than ± 300-ns resolution
- LT-PBX mode allowing D-channel arbitration and synchronization of DECT-base stations
- IOM-2 system interface
- 4 relay driver pins per port addressable by Monitor command
- 2 status pins per port reporting to the Monitor channel
- Activation procedure with the 15 s limit disabled to cope with regenerators
- JTAG-boundary scan path



8 Channel LT Application

General Description

In addition to four-wire S-interface terminals, the IOM architecture also supports two-wire terminals for PBX applications. A survey of PBX-loop conditions demonstrates that typically 95% of the subscriber loops show line lengths below 2 km. Therefore, a more economical solution which is optimized to these shorter loop lengths is required.

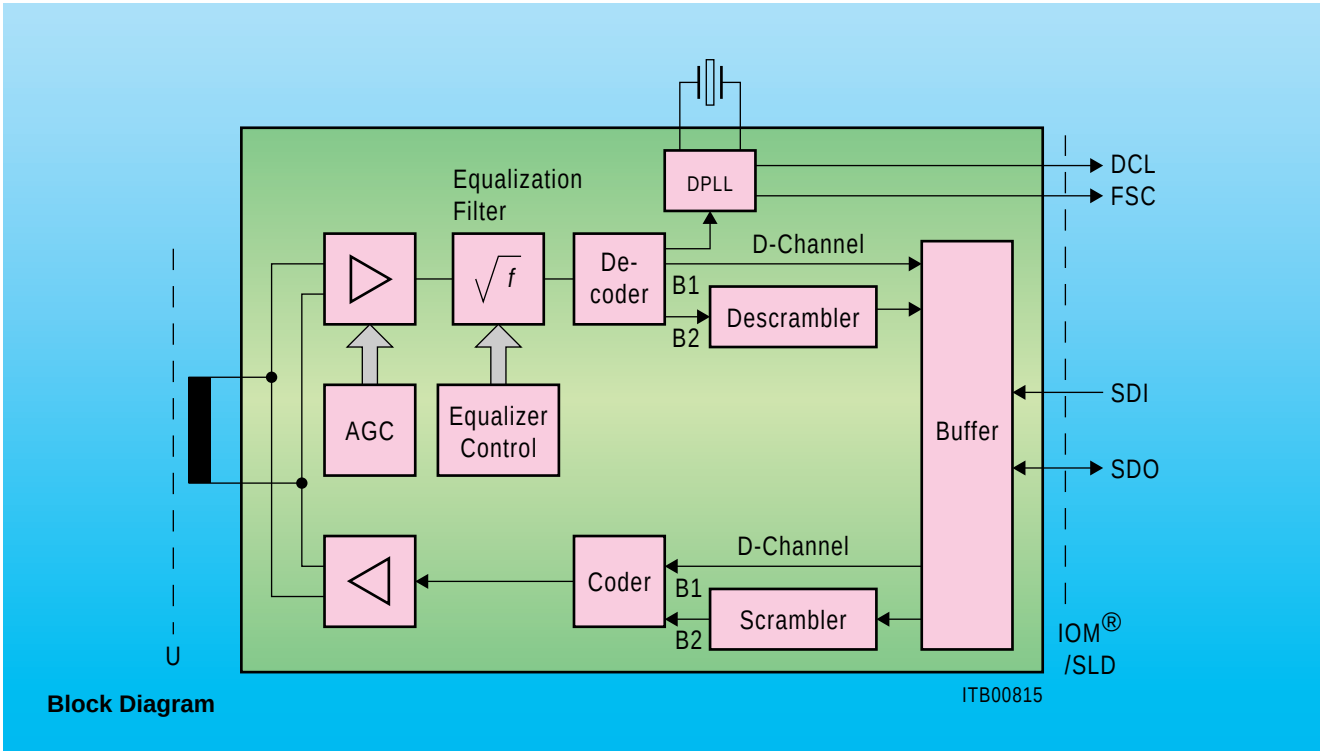
A time-compression multiplex concept has been chosen which – for separation of direction – divides the framing into a transmit and receive section. Taking synchronization bits and line conditions into account, a clock rate of 384 kbit/s, twice as high as for the S-bus, has been found to be optimal with respect to time compression, interference line attenuation and delay. The transceiver uses AMI coding, scrambling, automatic gain control and $\sqrt{f}$-equalizing to obtain excellent transmission quality.

From a system point of view, the IOM-compatible IBC is compatible with the IEC or SBC/SBCX as well as with the EPIC/ELIC and the IDEC on digital line card applications. Similar to the other components, the device is designed in 2-µm CMOS technology resulting in low power consumption of less than 80 mW in the active state.

Type	Package
PEB 2095-N	P-LCC-28-2 (SMD)
PEB 2095-P	P-DIP-24-1 (not for new designs)

Features

- Half-duplex burst-mode two-wire transceiver
- 144-bit/s user bit rate (B+B+D)
- 384-kHz line clock rate including maintenance and synchronization
- U_{P0} interface, industry standard for 2-wire PBXs (AMI-line code)
- IOM-interface compatible (IOM-1 or IOM-2)
- Adaptive line equalization (SC filter)
- Recovery of clock and frame signals from data stream
- Activation/deactivation procedure according to CCITT recommendation
- Awake in power-down mode
- Switching of test loops
- Transmission range up to 3.5 km with 0.6-mm wire
- 2-µm CMOS technology
- Low power consumption
  Active: 80 mW (typ.)
  Power-down: 6 mW (typ.)



Block Diagram

General Description

The PEB 2096, OCAT-P, performs the layer-1 functions of the ISDN basic access for eight U_{PN} interfaces at the LT side of the PBX.

Applications

PBXs

$8 \times U_{PN}$ interfaces

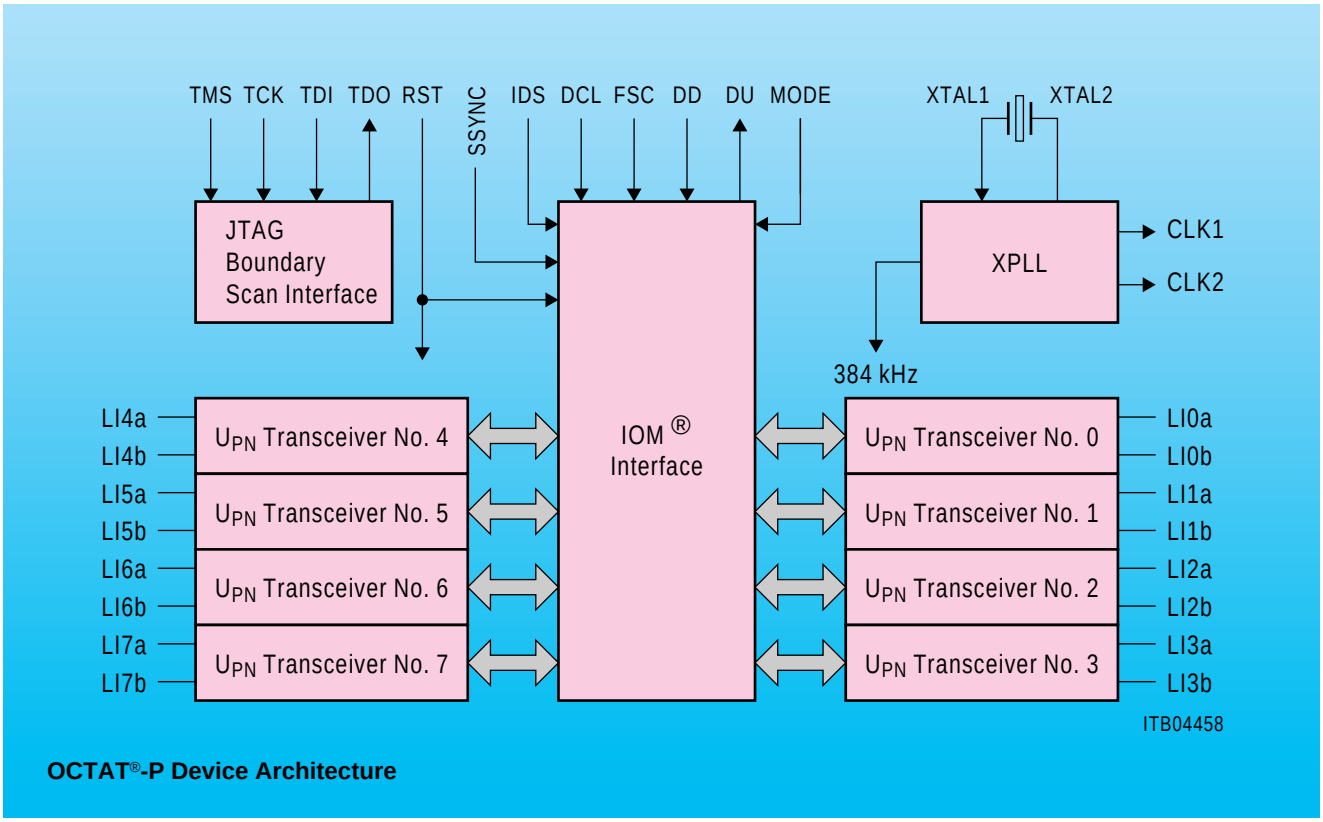
Interfaces

- IOM-2 interface
- $8 \times U_{PN}$ interface
- Boundary scan (for on-board tests)

Type	Package
PEB 2096	P-MQFP-44-1 (SMD)

Features

- Eight full duplex 2B+D U_{PN}-interface transceivers, each equipped with the following functions:
  - Conversion from/to binary to/from pseudo-ternary code
  - Receive timing recovery
  - Activation/deactivation procedures, triggered by primitives received over the IOM interface or by INFO received from the line (e.g. detection of INFO1)
  - Execution of test loops
  - Analog line transceiver for up to 16-dB line attenuation
  - U_{PN}-interface functions compatible to PEB 2095, IBC, and PEB 20950, ISAC-P (except for looplength)
  - U_{PN} interface fully compatible to PSB 2196, ISAC-P TE, and PSB 2197, SmartLink-P
- IOM-2 interface
- Support for JTAG-boundary scan test
- 1-µ CMOS technology with low power consumption
- P-MQFP-44 package



OCTAT®-P Device Architecture

Subscriber Line Power Feeding

PEB 2025

ISDN Exchange Power Controller (IEPC)

General Description

The PEB 2025 is an integrated power controller especially designed for ISDN environments and for the use in a digital exchange. High-voltage CMOS technology 60 V ensures variety of applications:

- Two- and four-wire transmission lines
- Point-to-point configurations
- Point-to-multipoint configurations

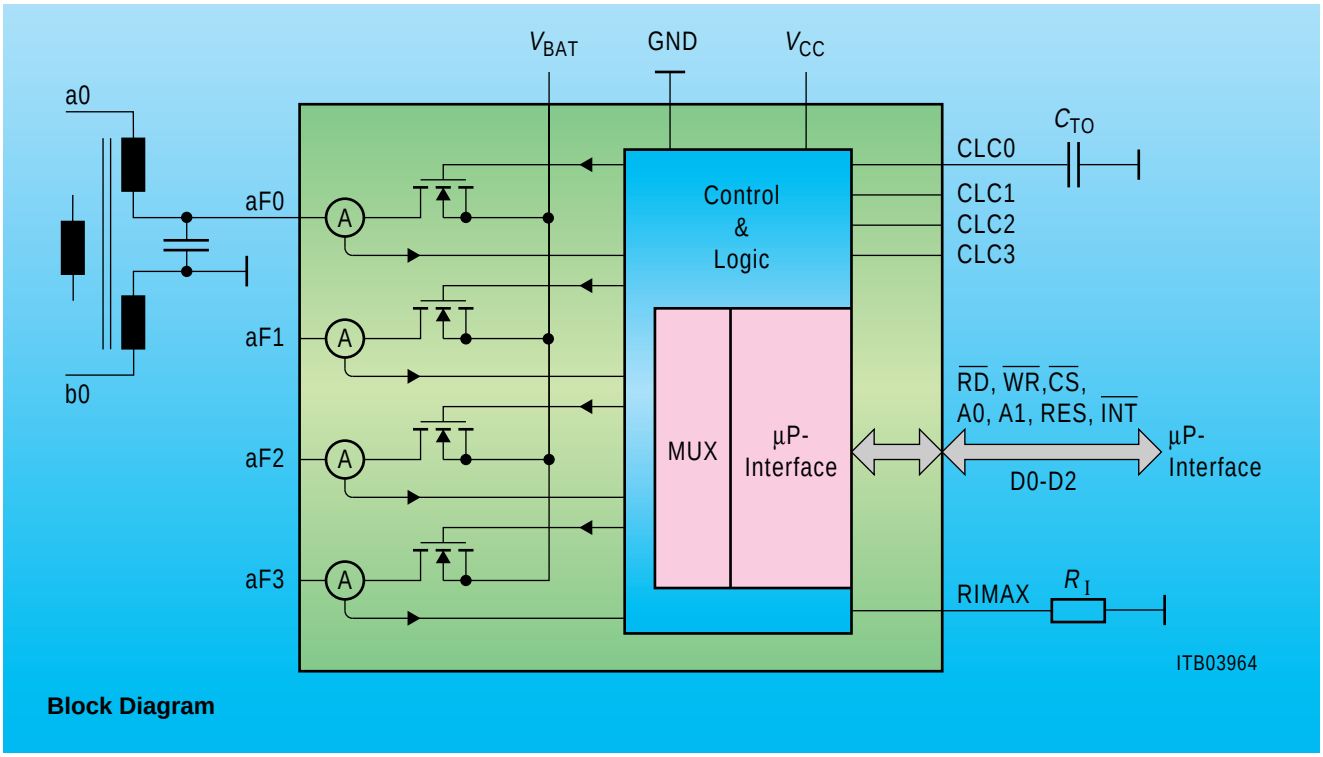
The device is fully compatible with the CCITT recommendations for power feed at the S-interface. Each line is individually powered and controlled via a microprocessor interface. An interrupt output pin signals any malfunction to the microprocessor.

Programmable output current and thermal shutdown guard the PEB 2025 against overloads.

Type	Package
PEB 2025-N	P-LCC-28-1 (SMD)
PEB 2025-P	P-DIP-22-1 (not for new designs)

Features

- Compatible to CCITT recommendations for power feed at the S-interface
- Supplies power for up to four transmission lines. Each line is individually powered and controlled
- High-voltage CMOS technology (up to 60 V, shiftable)
- Maximum output current programmable up to 100 mA
- Programmable switch-off characteristic by overcurrent detection
- Automatic restart after removal of overload conditions
- Status detectors for each line driver
- Microprocessor-compatible interface (up to 8-MHz clock frequency)
- Interrupt output for detection of any malfunction
- Full protection against shorts between transmission lines



Block Diagram

Advanced Information

General Description

In order to maintain its leading position Siemens is defining a new IC – the DOC – comprising all necessary functional blocks like switching, signaling, DTMF/tone handling and conferencing on a single chip. The transceivers (layer-1 ICs) are not integrated.

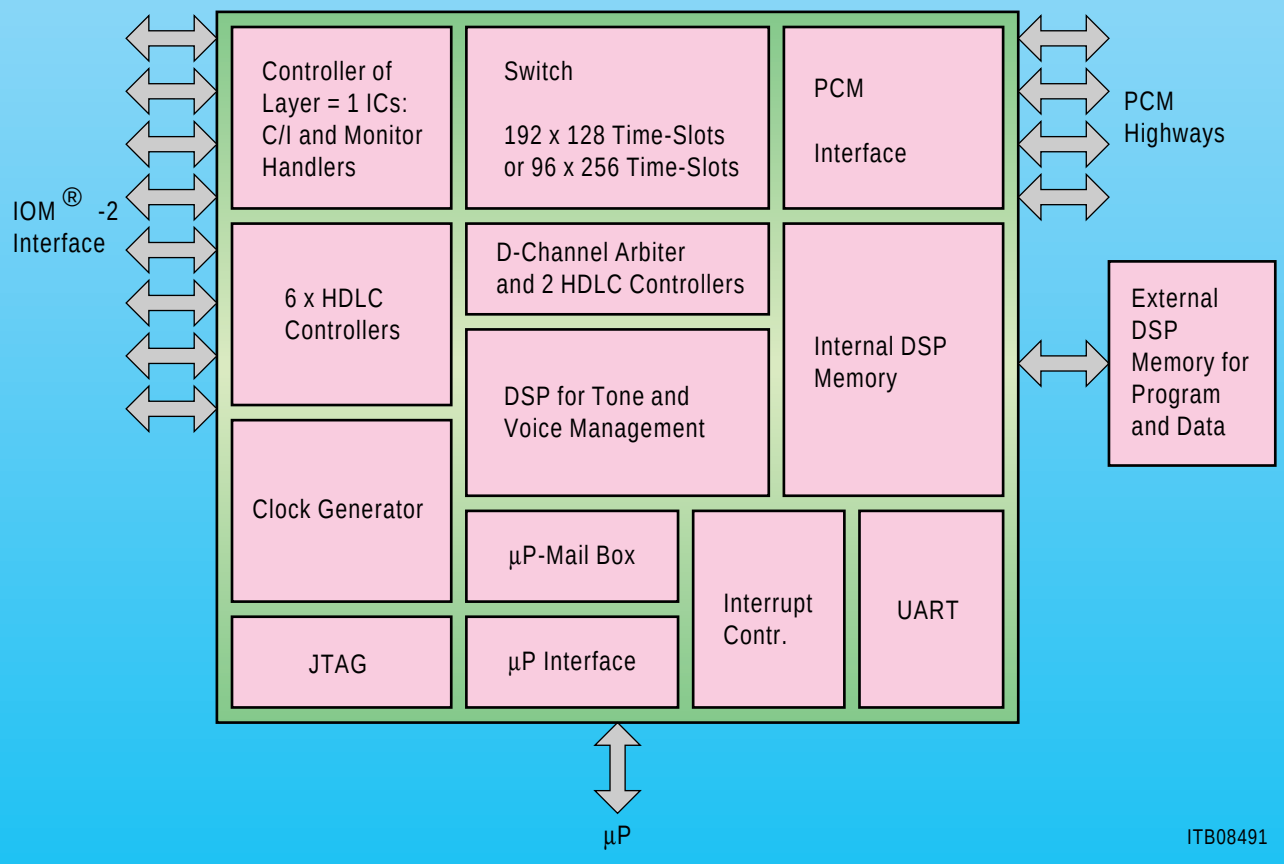
Features

The DOC provides all necessary features for building PBX (Private Branche eXchange) systems and Line Cards.

- In the PBX mode, the DOC provides:
  - 6 fully usable IOM-2 (GCI) interfaces and thus it can control up to 48 ISDN or 96 analog subscribers.
  - 4 PCM highways with 126 time-slots.
- In the Line Card mode, the DOC provides:
  - 2 fully usable IOM-2 interfaces with 16 IOM-2 subframes (2×8) and
  - 2 limited IOM-2 interfaces, as two DSP ports are connected, and thus it can control 16 to 24 ISDN (or 32 to 48 analog) subscribers.
  - 4 PCM highways with 256 time-slots.
- Signaling via 8 assignable HDLC controllers, each with a 64-byte data FIFO for transmit and for receive direction.
  - 2 HDLC controllers (SACCO-A) assignable of two of up to 48 ISDN subscribers at a time via two different D-channel arbiters.
  - 4 HDLC controllers (SIDEC) assignable to any D-/B-channel in data upstream or data downstream direction on four IOM-2 interfaces.
  - 2 HDLC controllers (SACCO-B) assignable to any time-slot in data upstream or data downstream direction on four IOM-2 interfaces or to PCM highway. Optionally, both controllers can be used as stand alone HDLC controllers with up to 8.192-Mbit/s transfer rate. They support DMA interface.

Type	Package
PEB 20560	P-MQFP-160-1 (SMD)

- On-chip user programmable 16-bit Digital Signal Processor, Siemens OAK, (with 20, 30 or up to 40 MIPS) with access to 64 time-slots (via one or two internal IOM-2 interfaces) for DTMF/tone generation and recognition, conferencing, music-on-hold, modem emulation, etc.
  - $1\ K \times 16$-bit on-chip data memory (X)
  - 512×16-bit on-chip data memory (Y)
  - DSP proprietary interface to an external memory:
    Program memory up to $62\ K \times 16$ bit
    Data memory up to $32\ K \times 16$ bit
  - On-chip program memory (Boot)
- a-/µ-Law coding and decoding by hardware (on the fly)
- Firmware for DSP load measurement (within every 125-µs frame)
- µP-DSP communication via a µP-Mail-Box
- On-chip emulation (OCEM) for DSP program debugging
- 8-bit µP interface compatible with Siemens/Intel/Motorola bus schemes
- Programmable clock generator with built-in logic for master and slave configurations
- Watch-dog timer
- Reset logic
- UART for V.24 interface
- Multifunctional input/ouput port configurable as a general I/O port, DMA lines for one SACCO or as additional UART lines for modem connection
- Integrated interrupt controller with vector generation and support for DOC cascading
- JTAG interface for on board tests
- Interface for HW and SW evaluation (debugging)
- Advanced CMOS 0.6-µm technology
- 3.3 and 5-V power supply
- TTL driving capability, TTL and CMOS compatible inputs
- P-MQFP-160 package



Block Diagram

Primary Rate Interface (PRI) ICs

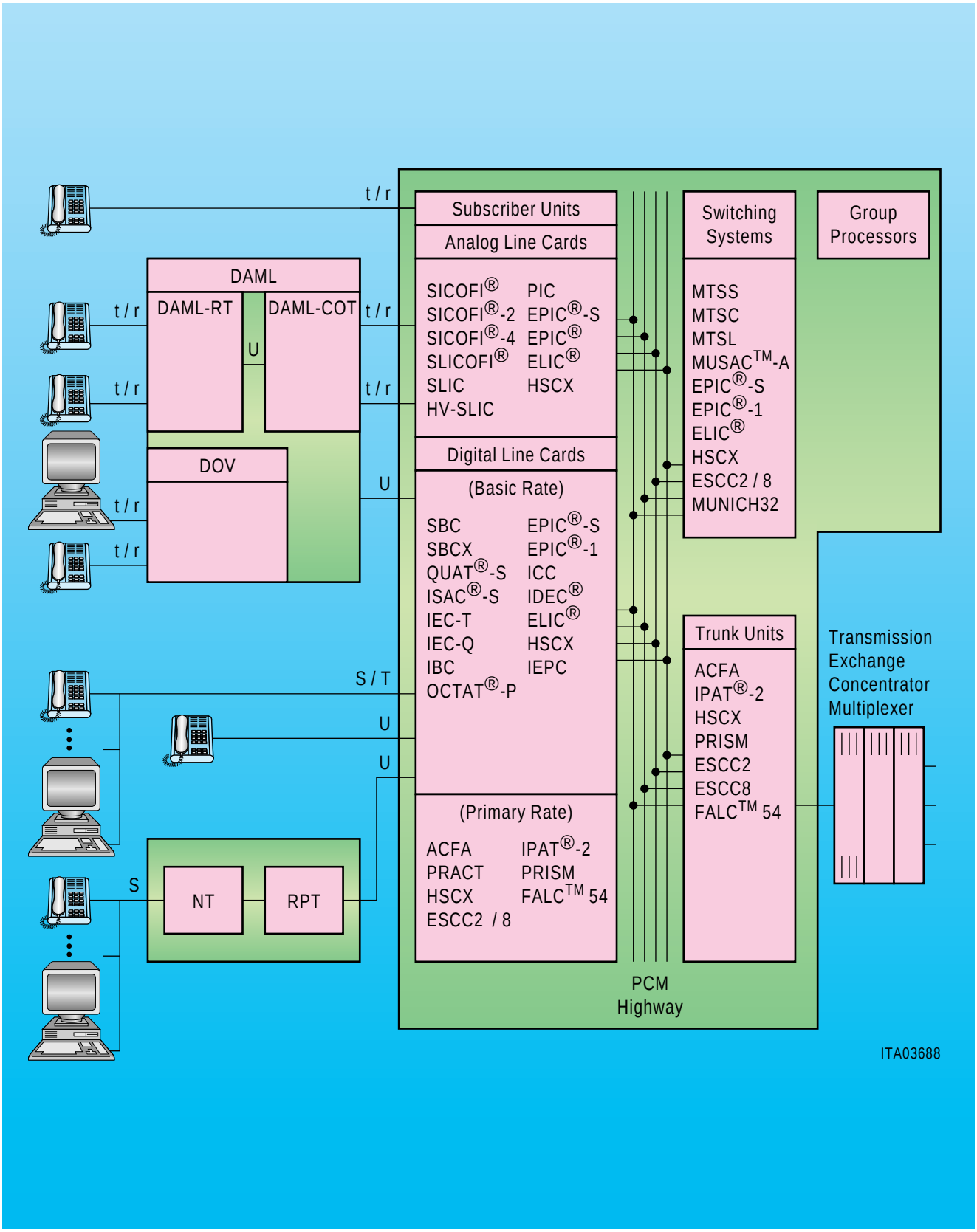
Primary Rate Interface Signaling and Maintenance Controller
PRISM; PEB 3035

Primary Rate Interface (PRI)

Product Overview

Type	Short Title	Description	Page
PEB 2035	ACFA	Advanced CMOS Frame Aligner	132
PEB 2236	IPAT®-2	ISDN Primary Access Controller	134
PEB 3035	PRISM	Primary Rate Interface Signaling and Maintenance Controller	135
PEB 2254	FALC™54	Frame and Line Interface Component	136
PEB 22320	PRACT	Primary Access Clock and Transceiver Component	139
SAB 82525 SAB 82526	HSCX HSCX1	High-Level Serial Communication Controller Extended	162
SAB 82532	ESCC2	Enhanced Serial Communication Controller (2 channels)	163
SAB 82538	ESCC8	Enhanced Serial Communication Controller (8 channels)	165

Primary Rate Interface (PRI)



Applications for the Primary Rate Interface include trunk lines between public central office (CO) exchanges, from a PBX to a CO, interlinking PBXs, the gateway connecting a LAN to the public network on a PBX, interlinking LANs, interfacing a large computer or data intensive terminal (e.g. CAD graphics) with the CO or a PBX etc.

Due to different technical evolutions in Europe and the US there are two basic interface types for 1st order transmission systems, the T1 and the CEPT or E1 standard. The ISDN-PRI is based on these two different standards. The main difference between ISDN-PRI and T1/CEPT transmission systems is the type of signaling used.

The T1 standard is based on the PCM24 technique, where twenty-four 64-kbit/s basic channels and one framing bit are combined into one 1.544-Mbit/s frame format.

The CEPT standard is based on the PCM30 technique. The 2.048-Mbit/s frame consists of thirty 64-kbit/s basic channels, one 64 kbit/s signaling channel and 64-kbit/s framing and maintenance channel.

Siemens Semiconductor Division offers a complete solution of ICs covering different standards and applications.

The PEB 2236 IPAT®-2 (**I**SDN **P**rimary **A**ccess **T**ransceiver) and the PEB 2035 (**A**dvanced **C**MOS **F**rame **A**ligner) fulfill the T1 and CEPT standards. At the system side the ACFA provides a synchronous PCM interface for connecting to other application specific ICs (e.g. MTSx, HSCX).

The IPAT-2, together with the ACFA, implement the layer-1 physical interface.

Both devices are programmed via the µP interface to perform the different standards, applications and maintenance/ service functions.

The IPAT-2 is a monolithic line driver for primary access lines of either the PCM24 (T1, N. America/Japan) or PCM30 (CEPT, W. Europe) standards. In the receive direction, the device recovers the clock and data signals from the line and forwards them to the ACFA.

The IPAT-2 is transparent to the received line code. In the transmit direction, the device takes the signal received from the ACFA and forms it into transmission pulses according to CCITT recommendations for the PCM30 or AT&Ts DMI specifications for PCM24. Correspondingly, input/output jitter requirements comply with both CCITT and AT&T specifications.

Frame alignment for all commonly used framing and multiframing formats is performed by the ACFA. The device synchronizes the transmit and receive signals, interfaces the data rate from the line to the 2.048 Mbit/s or 4.096 Mbit/s internal highway and codes/decodes one of three selectable line codes.

For PCM24, this transmission code can be either B8ZS or AMI-ZCS whereas for PCM30, it is always HDB3. Alarms and error conditions are reported to the microprocessor via a maskable interrupt line. The ACFA can also be used for various signaling schemes. Rather than using the HSCC/ HSCX, signaling information can be handled by a less intelligent communications controller without programmable time-slot access. For such devices, the ACFA provides the required signaling information via special purpose pins. Additionally, the ACFA has a DMA interface for transferring signaling information to/from a microprocessor controlled memory. Finally, signaling data can be accessed directly via the microprocessor interface.

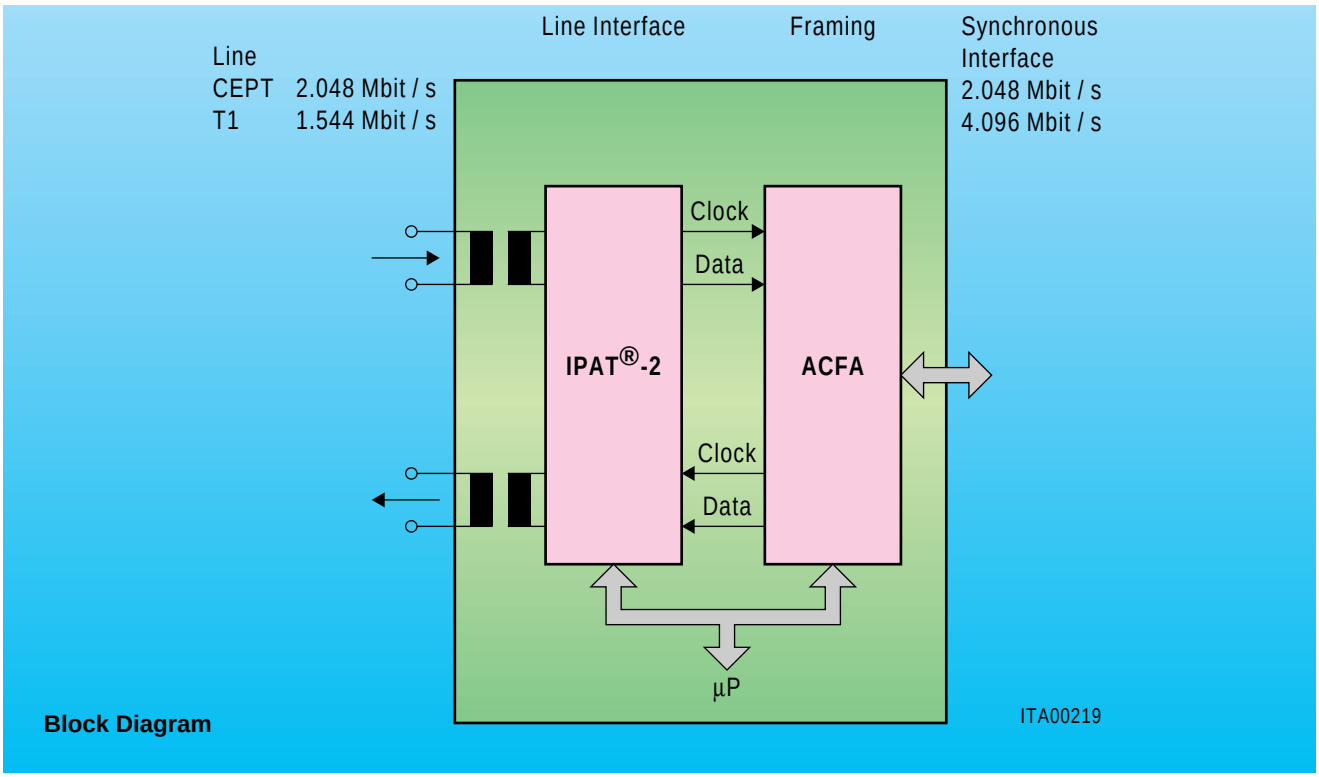
Siemens new generation of Primary Rate Interface component, the PEB 2254 FALC54 (Framing And Line Interface plus signaling Controller), implements the functionality of a line interface, frame aligner and signaling controller for both standards E1 and T1 on a single chip.

Applications

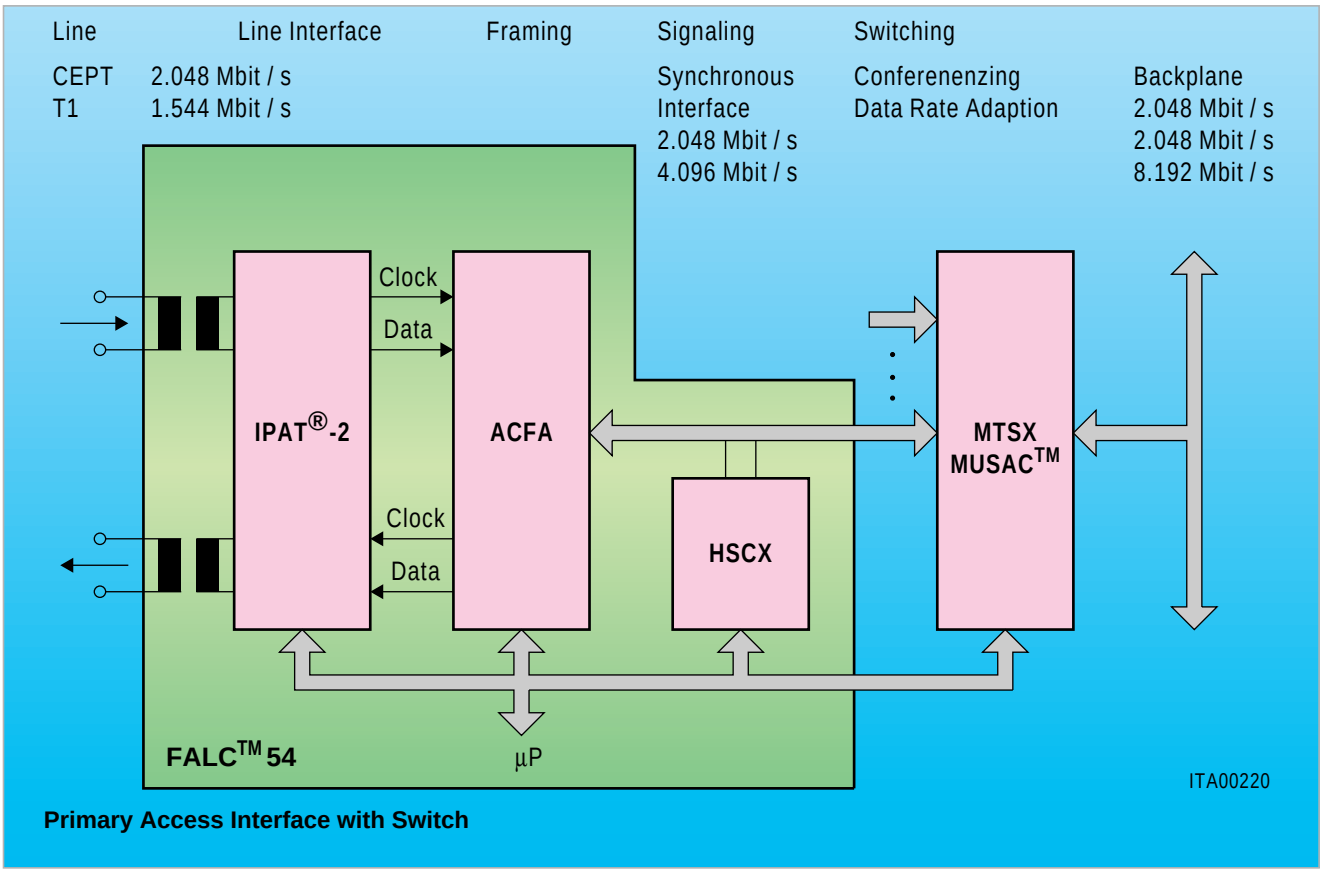
In general the following applications can be covered:
- Synchronous/asynchronous multiplexers
- Digital access cross connects
- Central offices switches
- Remote switches, subscribers loop carriers
- LAN, MAN, WAN, Bridges, Routers
- FITL
- PBX interfaces

The following chapter outlines the application of the Primary Rate devices ACFA, FALC54 and I PAT-2 and shows the flexibility of the architecture.

In the switching application the Primary Rate Interface is connected to a switching network of a PBX, CO or concentrator. The switching devices MTSL (**M**emory **T**ime **S**witch **L**arge), MTSC (**M**emory **T**ime **S**witch **C**MOS) and MTSS (**M**emory **T**ime **S**witch **S**mall) perform the switching and data rate adaption. In addition to the switching function the MUSAC (**M**ultipoint **S**witching **a**nd **C**onferencing) can handle 64-conference channels in any combination.

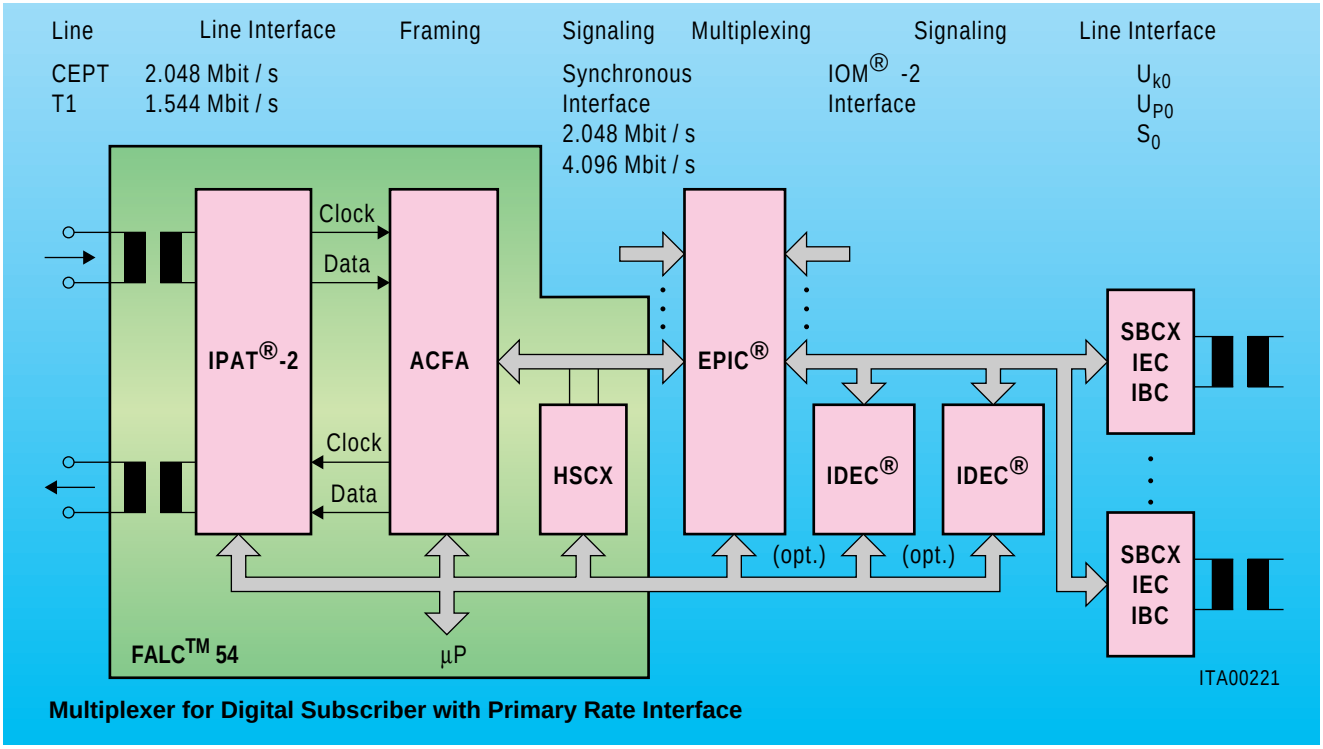


Block Diagram

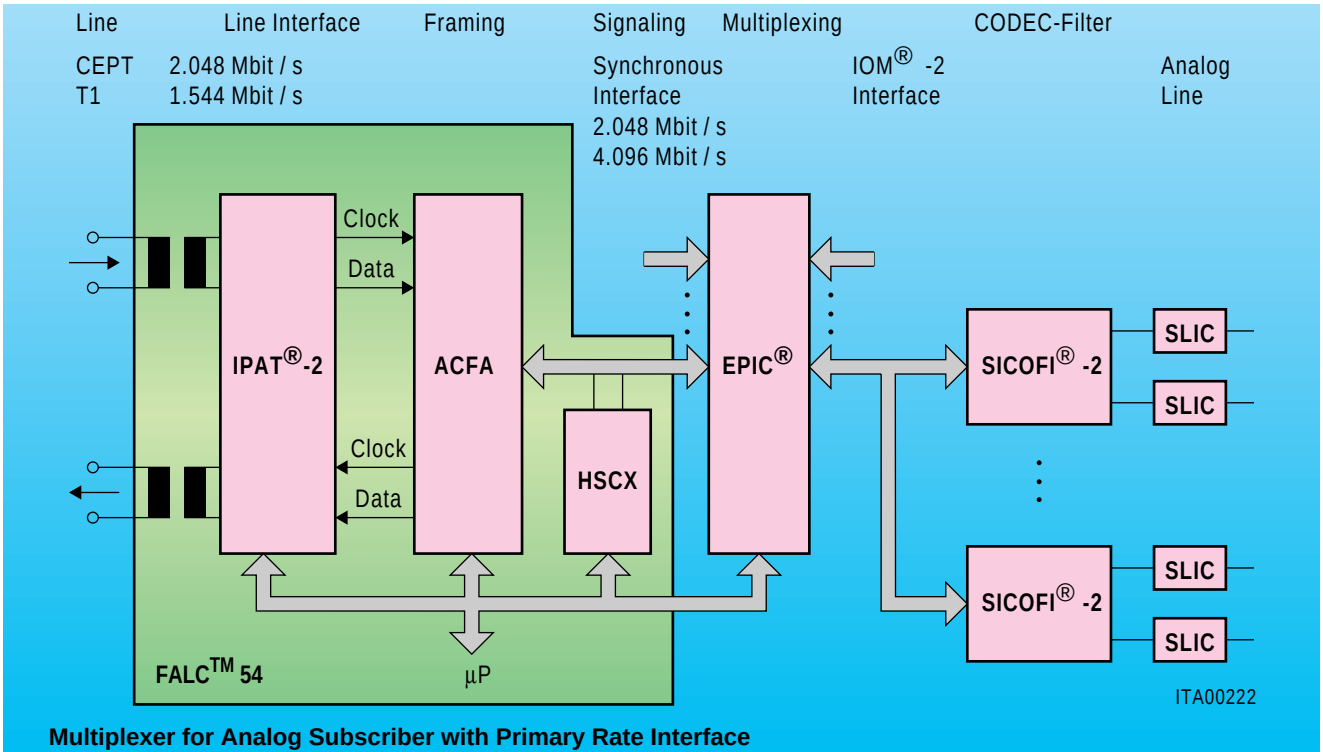


Primary Access Interface with Switch

Using the Primary Rate Interface in a MUX (Multiplexer) application, the EPIC (**E**xtended **P**CM **I**nterface **C**ontroller) multiplexes the analog or digital Subscriber line into the PCM highway. The device handles also the control information for the IOM interface. The HSCX (**H**igh level **S**erial **C**ommunication Controller e**x**tended) and the IDEC (**I**SDN **D**-channel **E**xchange **C**ontroller) performs the signaling function.

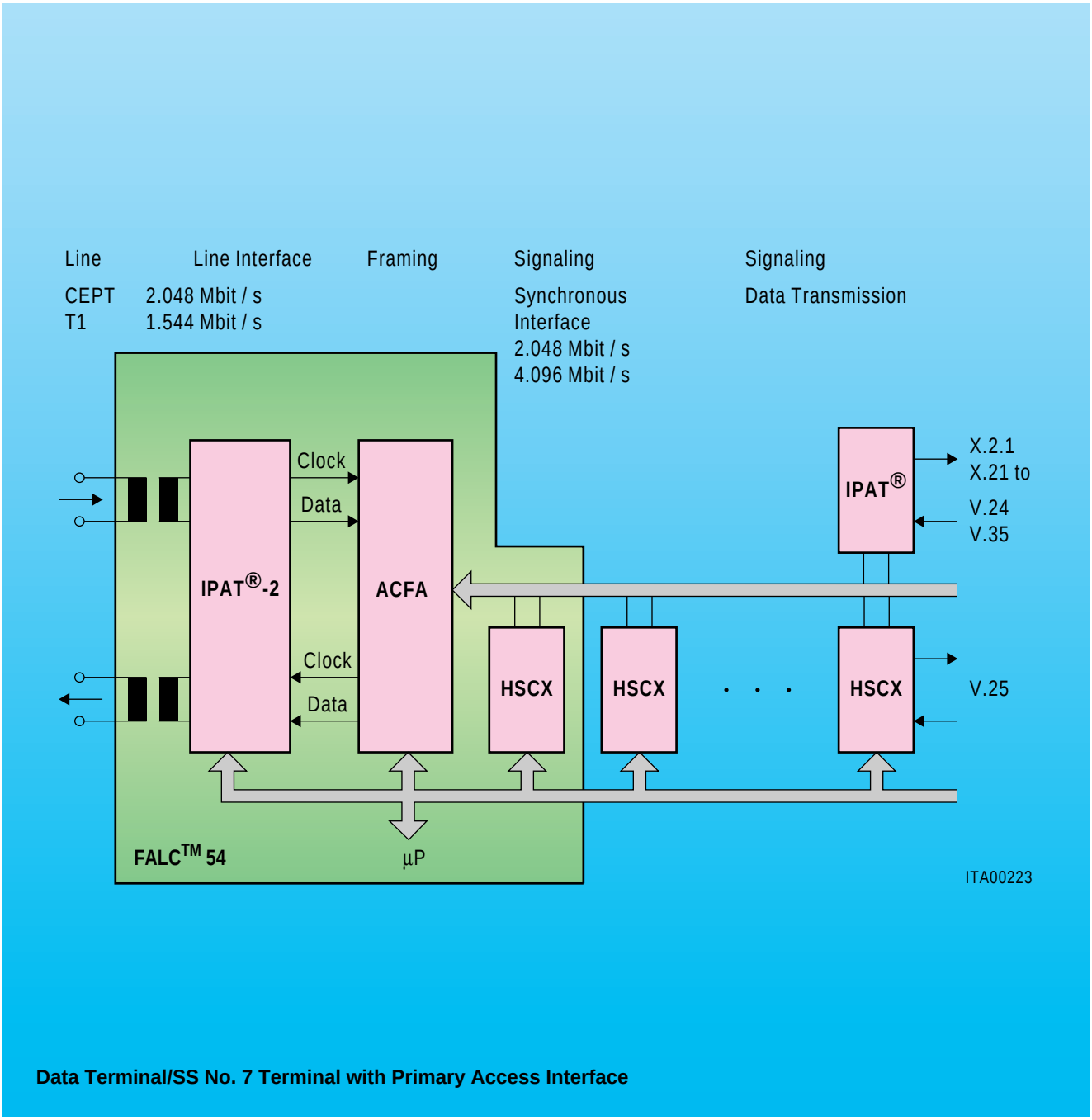


Multiplexer for Digital Subscriber with Primary Rate Interface



Multiplexer for Analog Subscriber with Primary Rate Interface

For fast data transmission via the Primary Rate Interface the HSCX or ITAC (**I**SDN **T**erminal **A**daptor **C**ircuit) is connected to the PCM highway. Using the HSCX, X.25 interfaces can be connected to the PRI or data transmission from the system memory (e.g. file transfer) of a PC to another PC or host computer can be performed. The IPAT handles data from a X.21 into V.24 or V.35 interface and inserts the information into the PRI.



Data Terminal/SS No. 7 Terminal with Primary Access Interface

General Information

The Advanced CMOS Frame Aligner (ACFA) PEB 2035 is a VLSI device used in interface modules with PCM systems.

Designed as an universal frame aligner, the ACFA will implement layer-1 (coding, decoding and synchronizing) functions for all PCM30 (32 channels) and PCM24 (24 channels) oriented applications. It complies with CCITT/ CEPT recommendations as well as with the AT&T DMI specifications (CCITT Rec. G 703, 704, 732, 733, November 1984; DMI specification April 1985).

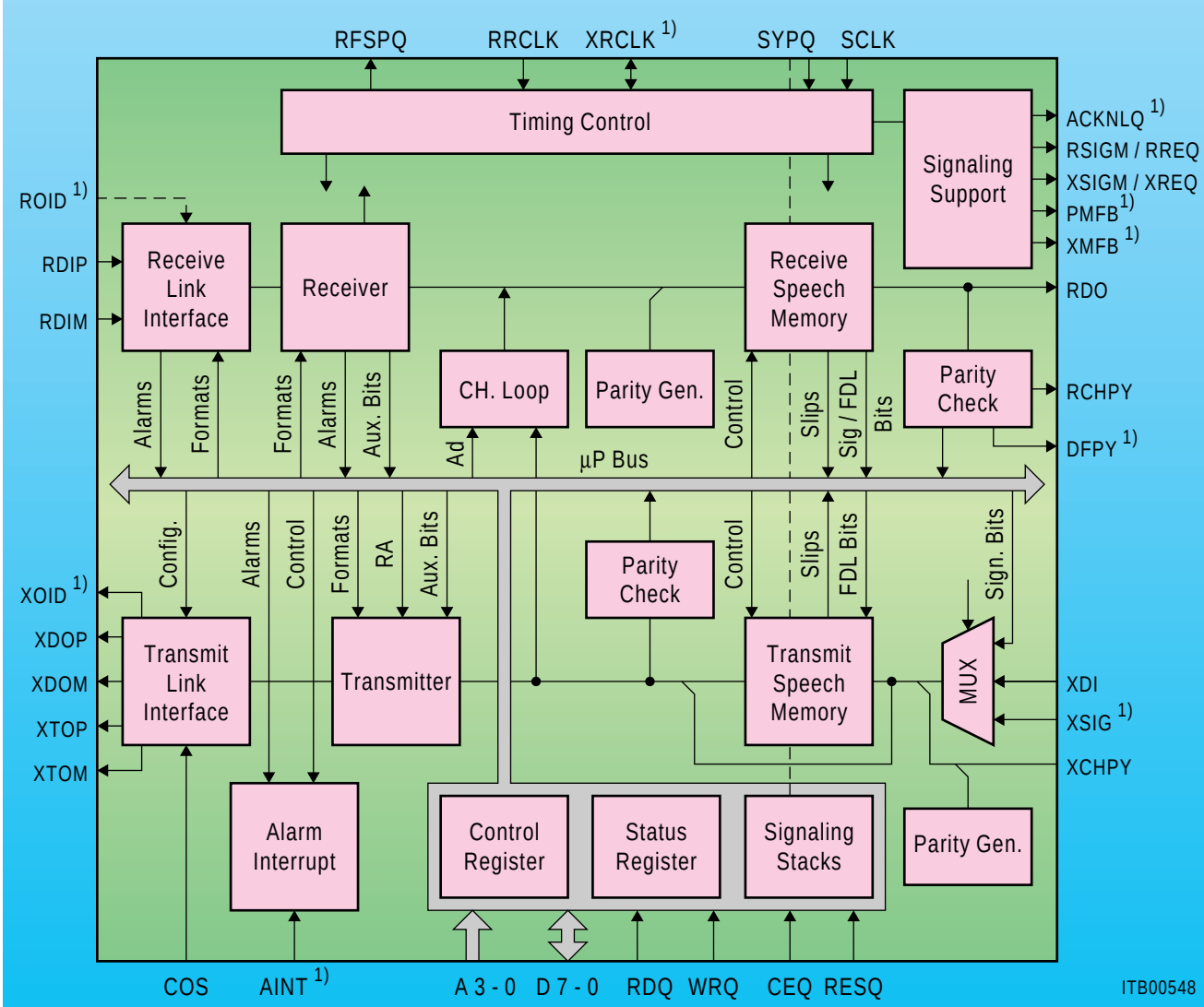
Switching between the PCM24 and the PCM30 modes is performed by programming via the microprocessor interface of the device. The extended features implemented in each of these two modes will meet most present and future requirements. A high degree of flexibility allows its use without addition of specialized hardware.

Besides interfacing to T1/CEPT routes and to an internal system highway, the ACFA supports the following interfaces:
– interface with fiber-optic transmission routes
– parallel microprocessor interface
– interface to support different signaling schemes
– testing and diagnostic interface

Type	Package
PEB 2035-N	P-LCC-44-1 (SMD)
PEB 2035-P	P-DIP-40-1
PEF 2035-N	P-LCC-44-1 (SMD)
PEF 2035-P	P-DIP-40-1

Features

- Frame alignment for 2.048-Mbit/s and 1.544 Mbit/s PCM system
- Meets CCITT Rec's (G 703, 704, 732, 733) and AT&T technical advisories
- Coding/decoding for HDB3, B8ZS and AMI-ZCS (zero code suppression) line codes
- Clear channel capability for AMI ZCS and CAS-BR
- Unipolar NRZ for interfacing fiber-optic transmission routes
- Error checking via CRC4 or CRC6
- Interfacing with a system internal 2.048-Mbit/s or 4.096-Mbit/s highway
- Elastic memory for route clock wander and jitter compensation
- Support for different signaling schemes
- Testing and diagnostics
- Single +5-V power supply
- Advanced CMOS technology
- Low power consumption



Block Diagram

General Information

The ISDN Primary Access Transceiver IPAT-2 (PEB 2236) is a monolithic CMOS device which implements the analog receive and transmit line interface functions to primary rate PCM carriers. It may be programmed or hardwired to operate in PCM30 (2.048 Mbit/s) and PCM24 (1.544 Mbit/s) carrier systems.

The IPAT-2 recovers clock and data using an adaptively controlled receiver threshold. It is transparent to ternary codes and shapes the output pulse according to the AT&T Technical Advisory #34 or CCITT G.703. The jitter tolerance of the device meets the latest CCITT recommendations (I.431) and many other specifications by AT&T/Bellcore. Diagnostic facilities are included.

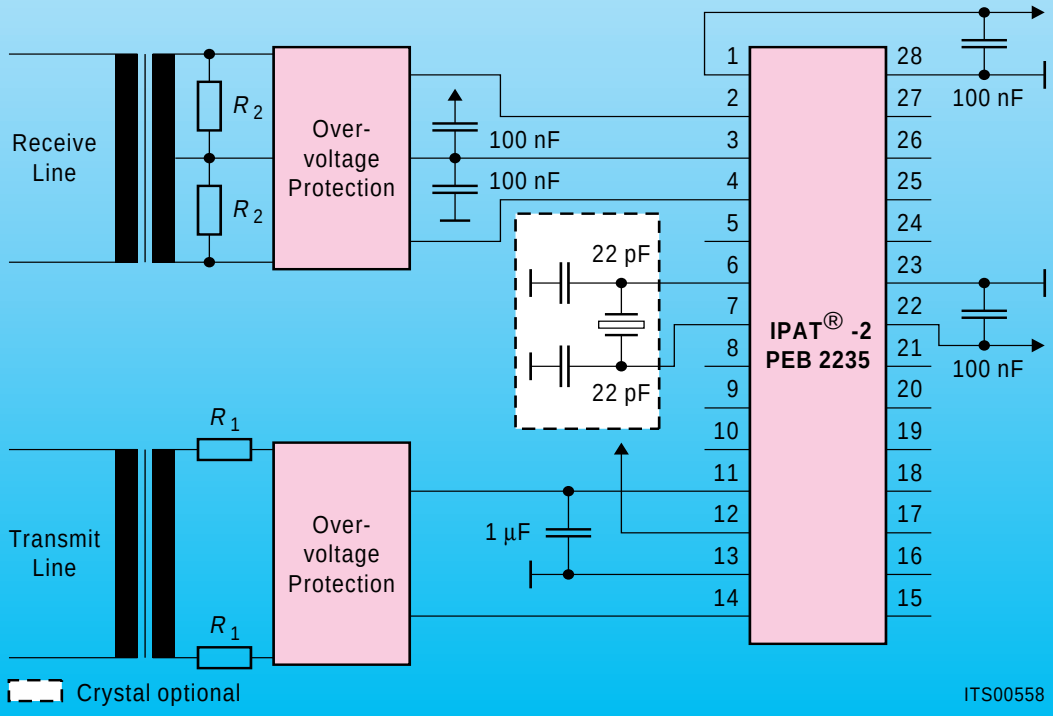
Specially designed line interface circuits simplify the tedious task of protecting the device against overvoltage damage while still meeting the return loss requirements.

The IPAT-2 is suitable for use in a wide range of voice and data applications such as for connections of digital switches and PBXs to host computers, for implementations of primary ISDN subscriber loops as well as for terminal applications. The maximum range is determined by the maximum allowable attenuation.

Type	Package
PEB 2236-N	P-LCC-28-1 (SMD)
PEB 2236-P	P-DIP-28-1
PEF 2236-N	P-LCC-28-1 (SMD)
PEF 2236-P	P-DIP-28-1

Features

- ISDN line interface for 1544 and 2048 kbit/s (T1 and CEPT)
- Data and clock recovery
- Transparent to ternary codes
- Low transmitter output impedance for a high return loss with reasonable protection resistors (CCITT G.703 requirements for the line input return loss fulfilled).
- Adaptively controlled receiver threshold
- Programmable pulse shape for T1 applications
- Jitter specifications of CCITT I.431 and many AT&T/Bellcore publications met
- Implements local and remote loops for diagnostic purposes
- Monolithic line driver for a minimum of external components
- Low power, reliable advanced CMOS technology



External Wiring of the IPAT

General Description

The PEB 3035 (Primary Rate Interface Signaling and Maintenance Controller) is a two channel serial communication controller designed to support signaling and maintenance functions for T1 Primary Rate Interfaces using the Extended Superframe format ESF. The device supports the DL-channel protocol for ESF format according to T1.403-1989 ANSI specification or according to AT&T specification TR 54016, September 1989. The 8-bit parallel µP-interface fits perfectly into every Siemens/Intel 8-bit or 16-bit microcontroller system. Two serial channels can be programmed in three different clock modes to function in time-slot oriented applications, in a strobe mode or as a serial interface.

Type	Package
PEB 3035-N	P-LCC-28-1 (SMD)
PEB 3035-P	P-DIP-28-1
PEF 3035-N	P-LCC-28-1 (SMD)
PEF 3035-P	P-DIP-28-1

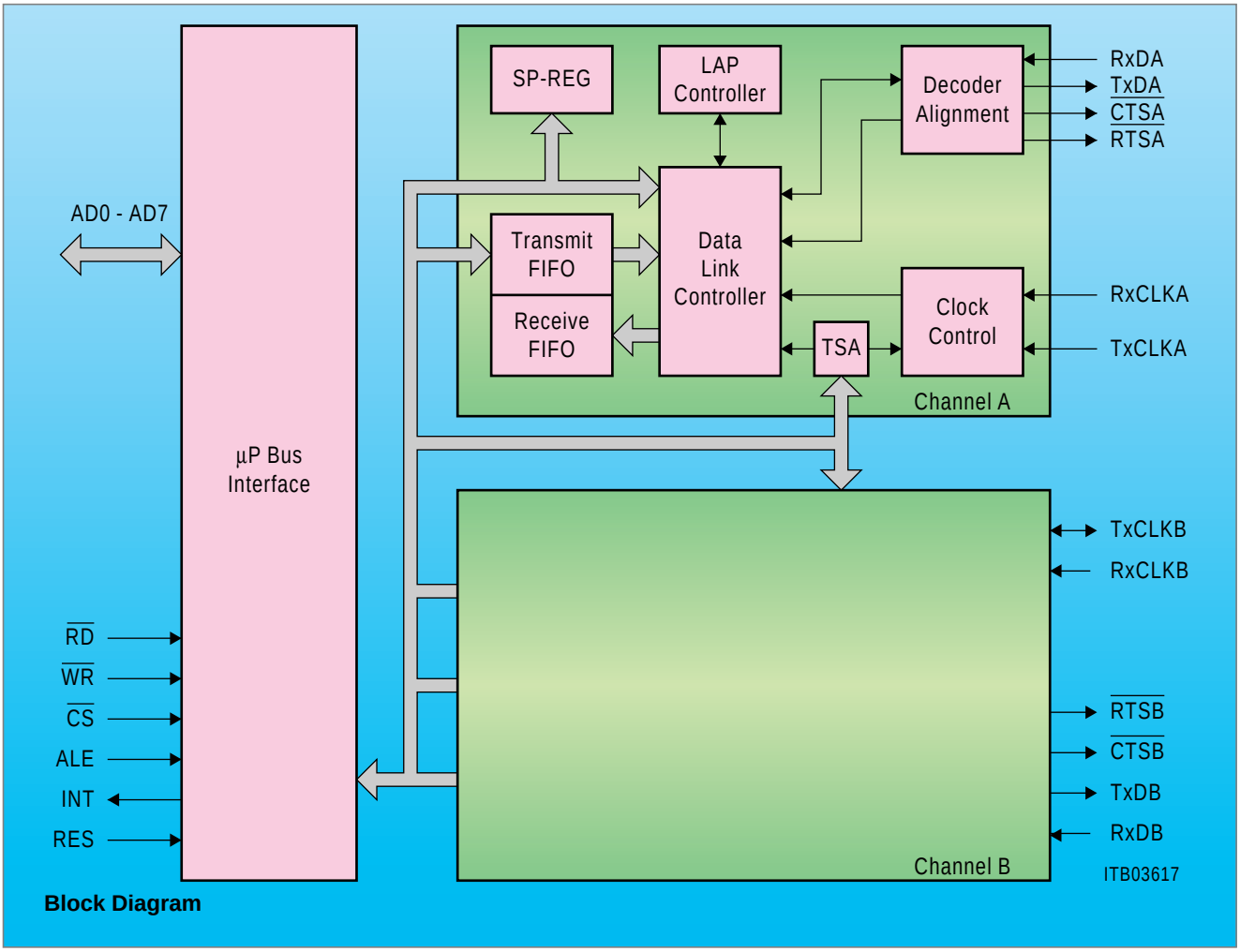
Features

Serial Interface

- Two independent signaling channels
- Programmable idle code (Flags, all ones)
- Continuous transmission of up to 32 bytes of data
- Data rate up to 4 Mbit/s

Protocol Support

- Support of ESF-DL protocol according to T1.403-1989 or according AT&T TR 54016 specifications
- Support of HDLC protocol
- Transparent mode for totally transparent data transmission and reception



Block Diagram

General Information

The Frame and Line Interface Component PEB 2254 (FALC54) is a high sophisticated single chip solution for primary rate PCM carriers. It may be programmed to operate in 1.544-Mbit/s (T1) or 2.048-Mbit/s (CEPT) carrier systems. The FALC54 provides the complete functionality of a line interface-, a framing-, clock generation (2 VCOs) and signaling unit on one chip with greatly increased functionalities.

The FALC54 recovers clock and data using an integrated digital phase-locked loop. It shapes the output pulse following the AT&T Technical Advisory #34 or CCITT G.703 and generates a variety of systems clocks. The jitter tolerance of the device meets the newest CCITT recommendations and many other specifications by AT&T/ BELLCORE.

The FALC54 features include: selectable multiframe (six multiframe formats), error checking (CRC4, CRC6), multiple line codes (HDB3, B8ZS, AMI, CMI, NRZ), alarm reporting, maintenance and performance monitoring. The circuit contains a two-frame elastic memory which ensures wander absorption between the PCM carrier and a synchronous, system internal highway.

All signaling types – CCS, CAS and bit robbed signaling in conjunction with Clear Channel Capability – are controlled by the integrated LAPD/CAS signaling controller. In addition, the FALC54 allows flexible access to facility data link and service channels. All signaling and data link access can be handled via 64-byte FIFOs.

The device includes functions which meet newest CCITT, ETSI and FTZ recommendations for primary rate interfaces and the AT&T Digital Multiplexed Interface specifications (DMI). Controlling and monitoring of the device is performed via a parallel 16-bit data bus interface which is directly compatible with the most popular 8/16-bit microprocessors (Intel or Motorola type).

Below a list of equipment as described by the CCITT which potential FALC54 applications.

2048-kbit/s Applications

- PCM-multiplex equipment according to G.732 G.735, G.738
- Digital multiplex equipment according to G.736, G.742, G.745
- External access equipment according to G.737, G.739
- Digital exchange equipment according to G.705, Q.511 Q.512
- Transmultiplex equipment according to G.793
- Video conferencing according to H.120, H.130
- Transcoder equipment according to G.761
- Digital circuit multiplication equipment according to G.763
- Digital section/line system according to G.921, G.952, G.956

Type	Package
PEB 2254-H	P-MQFP-80-1 (SMD)

1544-kbit/s Applications

- PCM-multiplex equipment according to G.733
- Digital multiplex equipment according to G.734, G.743
- Digital exchange equipment according to G.705, Q.511, Q.512
- Transmultiplex equipment according to G.793
- Video conferencing according to H.120, H.130
- Transcoder equipment according to G.762
- Digital circuit multiplication equipment according to G.763
- Digital section/line system according to G.951, G.955
- ADPCM-multiplex equipment according to G.724

Features

Line Interface

- Data and clock recovery
- Low transmitter output impedance for a high return loss with reasonable protection resistors (CCITT G.703 requirements for the line input return loss fulfilled)
- Adaptively controlled receiver threshold
- Programmable pulse shape for T1 and CEPT
- Transmit line monitor
- Jitter specifications of CCITT I.431 and AT&T publications 62411 met
- Maximum line attenuation more than 16 dB (CCITT I.431)
- Wander and jitter attenuation
- Implements local and remote loops for diagnostic purposes
- Selectable line codes (H DB3, B8ZS, AMI, AMI with ZCS)
- Analog and digital loss of signal indication
- On-chip clock generator for system clocks
- TRISTATE function of transmit line outputs
- Jitter attenuator

Frame Aligner

- Frame alignments/synthesis for 2048 kbit/s (CEPT, PCM30) and 1544 kbit/s (T1, PCM24)
- Meets newest CCITT Rec's, ETSI Rec's, FTZ Rec's, and AT&T Technical References
- Programmable formats for
  PCM30: Doubleframe, CRC Multiframe
  PCM24: 4-Frame Multiframe (F4),12-Frame Multiframe (F12, D3/4), Extended Superframe (ESF), Remote Switch Mode (F72, SLC96)
- Selectable conditions for loss of sync
- Fully implementation of the CRC4 Non-CRC4
- Interworking of CCITT G.706
- Error checking via CRC4 or CRC6 procedures
- Error monitoring via E-bit and SA6-bit in CEPT mode
- Performance monitoring
- Insertion and extraction of alarms (AIS, RRA, AUXP…)
- IDLE-code insertion for selectable channels
- System clock frequency different for receive and transmit
- Selectable 2048/4096-kbit/s system internal highway with programmable receive/transmit shifts
- Programmable TRISTATE function of 4096 kbit/s output via RDO
- Two-frame deep elastic receive memory for receive route clock wander and jitter compensation (can be reduced to one frame length for PCM30 master-slave applications)
- One frame elastic transmit memory (PCM24 mode only) for transmit route clock wander and jitter compensation
- Support for different data link schemes
- Flexible transparent modes
- Channel- and line loop back capabilities

Signaling Controller

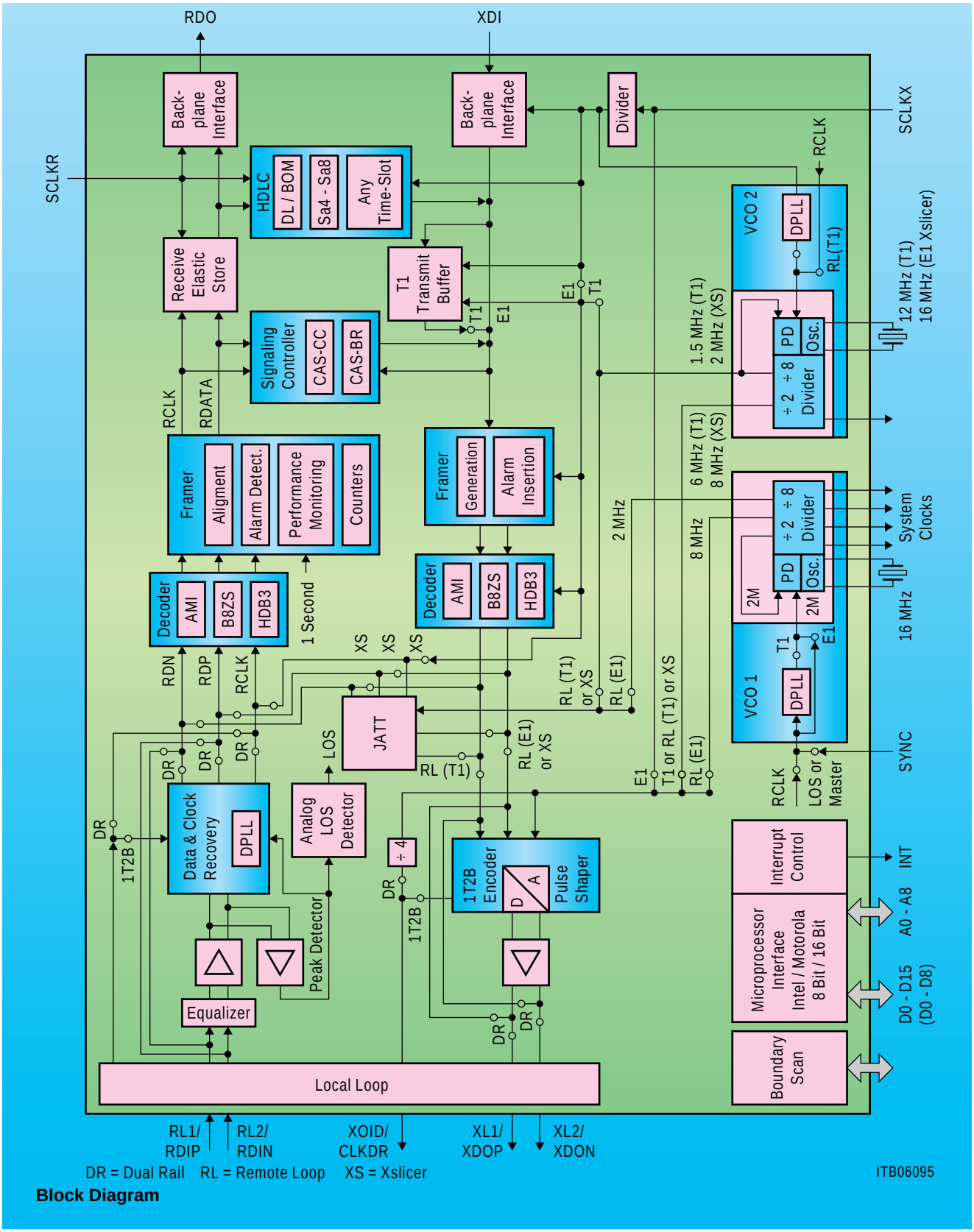
- LAPD controller
- Support DL-channel protocol for ESF format according to T1-403-1989 ANSI specification or according to AT&T specification TR54016 september 1989
- Handling of bit-oriented functions
- Programmable maximum packet size checking
- Programmable preamble
- Extended address masking
- Programmable FIFO size (32,16, …)
- CAS controller
- Multiframe synchronization and synthesis
- Alarm detection and generation
- Bit robbing support
- Clear channel capabilities in PCM24 mode
- Transparent Mode

MP Interface

- 8/16-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Extended interrupt capabilities

General

- Boundary scan standard IEEE 1149.1
- Advanced CMOS technology
- P-MQFP-80 package
- Power consumption less than 400 mW
  Note: The FALC54's power consumption is mainly determined by the line length and type of the cable.



Block Diagram

General Description

The Primary Rate Access Clock Generator and Transceiver PRACT (PEB 22320) is a monolithic CMOS device which implements the analog receive and transmit line interface functions to primary rate PCM carriers. It may be programmed or hard-wired to operate in 1.544-Mbit/s (T1) or 2.048-Mbit/s (CEPT) carrier system.

The PRACT recovers clock and data using an adaptively controlled receiver threshold. It is transparent to ternary codes and shapes the output pulse following the AT&T Technical Advisory #34 or CCITT G.703. The jitter tolerance of the device meets the CCITT (I.431) recommendation and many other specifications by AT&T/Bellcore. An on-chip selectable jitter attenuation is available which meets the I.431 recommendation for CEPT – and the PUB 62411 for T1 application. Diagnostic facilities are included.

Specially designed line interface circuits simplify the tedious task of protecting the device against overvoltage damage while still meeting the return loss requirements.

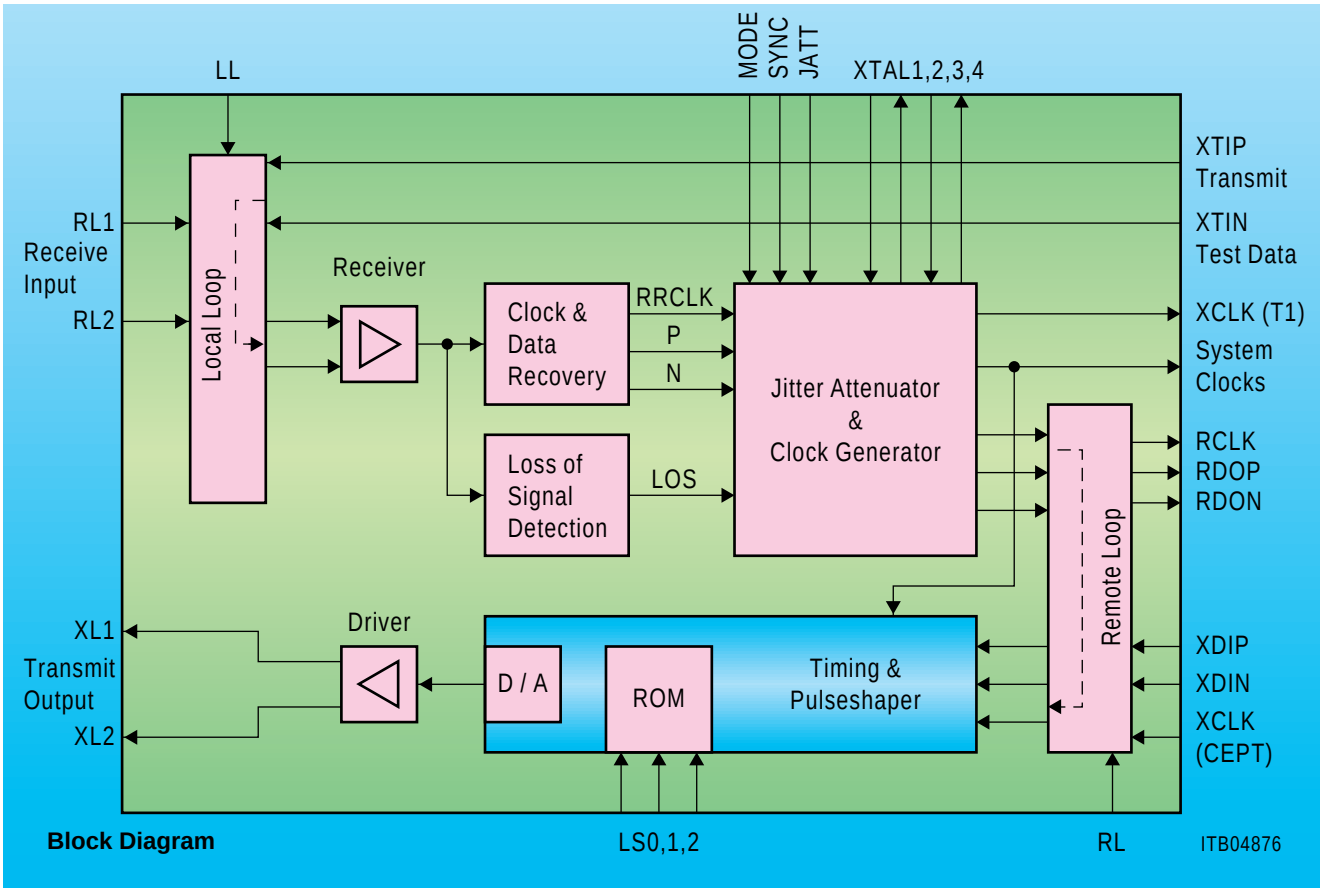
The PRACT is suitable for use in a wide range of voice and data applications such as for connections of digital switches and PBXs to host computers for implementations of primary ISDN subscriber loops as well as for terminal applications. The maximum range is determined by the maximum allowable attenuations.

In the T1 case the PRACT's power consumption is mainly determined by the line length and type of the cable.

Type	Package
PEB 22320-N	P-LCC-44-1 (SMD)

Features

- ISDN-line interface for 1544 and 2048 kbit/s (T1 and CEPT)
- Data and clock recovery
- Transparent to ternary codes
- Low transmitter output impedance for a high return loss with reasonable protection resistors (CCITT G.703 requirements for the line input return loss fulfilled)
- Adaptively controlled receiver threshold
- Programmable pulse shape for T1 applications
- Jitter specifications of CCITT I.431 and many AT&T/Bellcore publications met
- Wander and jitter attenuation
- Jitter tolerance of receiver: 0.5 UI s
- Implements local and remote loops for diagnostic purposes
- Monolithic line driver for a minimum of external components
- Low power, reliable CMOS technology
- Loss of signal indication for receiver
- Clock generator for system clocks



Block Diagram

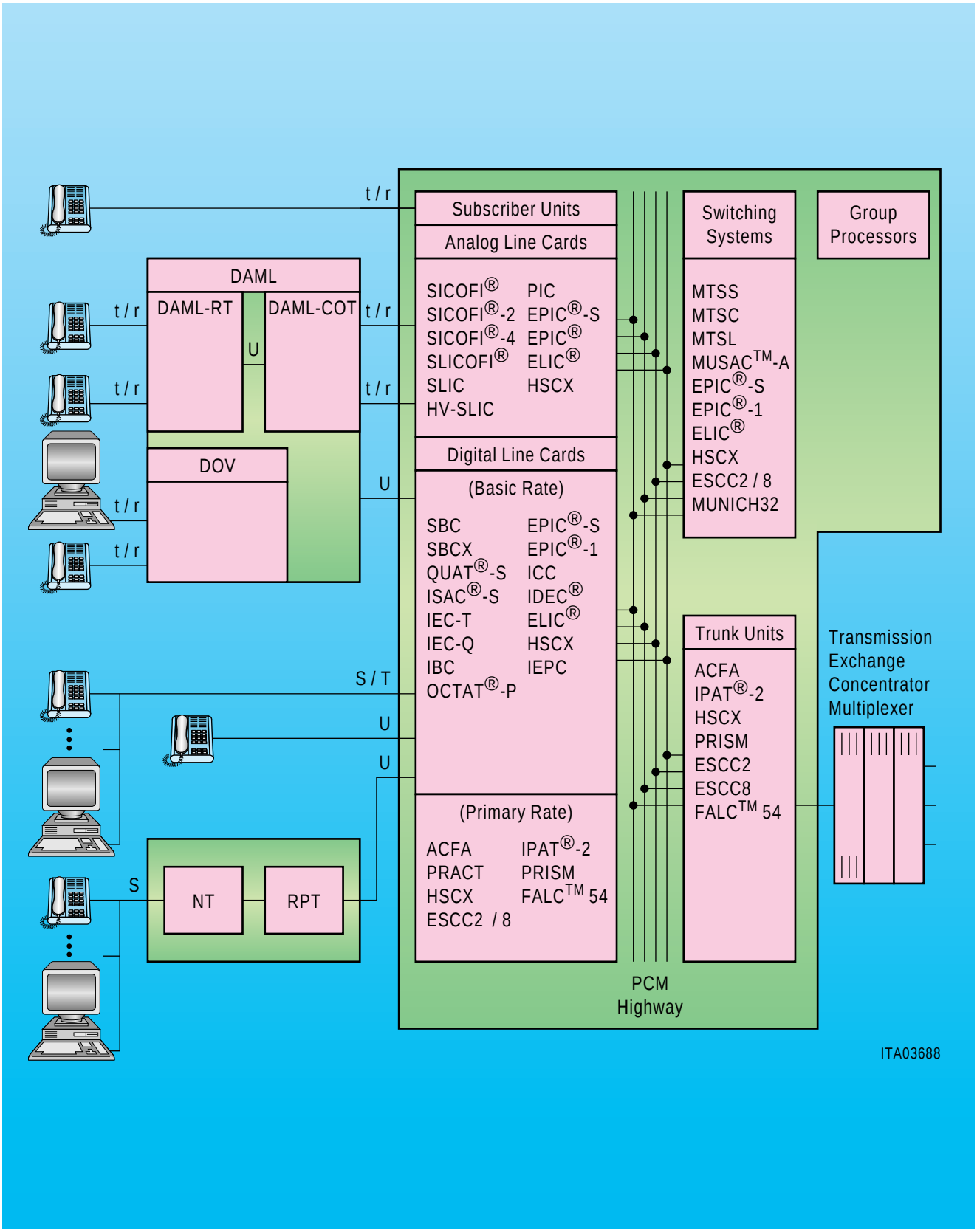
Multipoint Switching and Conferencing Unit Attenuation
MUSAC™-A; PEB 2445

Switching, Attenuation and Conferencing Family ICs

Product Overview

Type	Short Title	Function	Page
PEB 2045	MTSC	Memory Time Switch CMOS	147
PEB 2046	MTSS	Memory Time Switch Small	150
PEB 2047	MTSL	Memory Time Switch Large	151
PEB 2047-16	MTSL-16	Memory Time Switch Large H-16 MHz	153
PEB 2445	MUSAC™-A	Multipoint Switching and Conferencing Unit with Attenuation	154
PEB 2054	EPIC®-S	Extended PCM Interface Controller	90
PEB 2055	EPIC®-1	Extended PCM Interface Controller	91
PEB 20550	ELIC®	Extended Line Card Interface Controller	92
SAB 82C258 SAB 82C257	ADMA ADMA	Internetworking & Protocol Controllers	169
SAB 82525 SAB 82526	HSCX HSCX1	High-Level Serial Communication Controller Extended	162
SAB 82532	ESCC2	Enhanced Serial Communication Controller (2 channels)	163
SAB 82538	ESCC8	Enhanced Serial Communication Controller (8 channels)	165
PEB 20320	MUNICH32	Multichannel Network Interface Controller for HDLC	167

Switching, Attenuation and Conferencing IC-Family



Supervision and control of the entire system, including connection set-up, maintenance and testing, is performed in a powerful central processing unit. Besides this, the through-switching of PCM channels is done in a switching network unit, whereas the tasks of a frame alignment unit are to interface PCM transmission routes with the switching system.

Digital exchanges put calls through by newly arranging the speech signals coded with 8-bit words (PCM time-slots). The code words are transmitted serially on PCM lines. The sampling frequency of 8 kHz produces PCM frames with a duration of 125 µs. The transmission rate on the line determines how many code words (speech channels) can be accommodated within a sampling period. With a data rate of 2048 kbit/s for example, there are 32 time-slots of 8 bits each. Four lines with a data rate of 8192 kbit/s have a transmission capacity of 512 channels.

In a digital switching matrix one distinguishes between two basic switching principles:

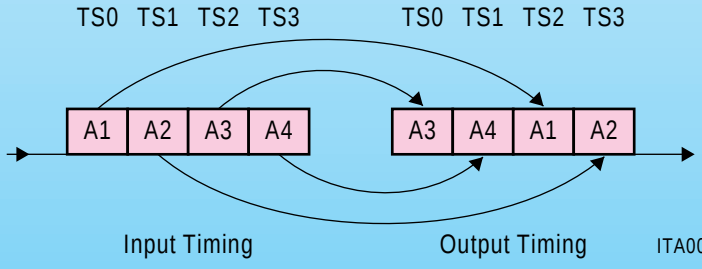
- Time division multiplex
- Space division multiplex

A method that is frequently used involves a combination of the two principles, this being called space/time division multiplex. The figure illustrates the different principles.

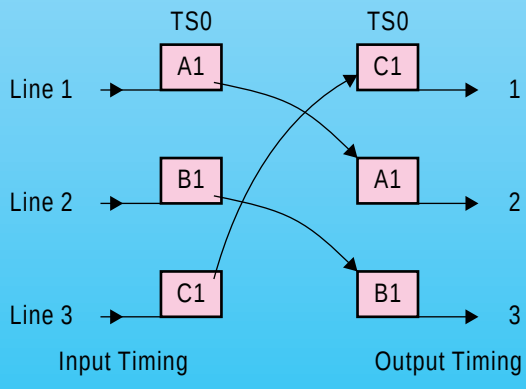
In time division multiplex only the time-slot is altered during switching. All signals from a certain input PCM line are switched to a fixed output line, only the time-slot sequence may change.

In space division multiplex incoming PCM data are only rearranged in space. The input time-slot equals the output time-slot. However, input from one PCM line can be switched to different output lines.

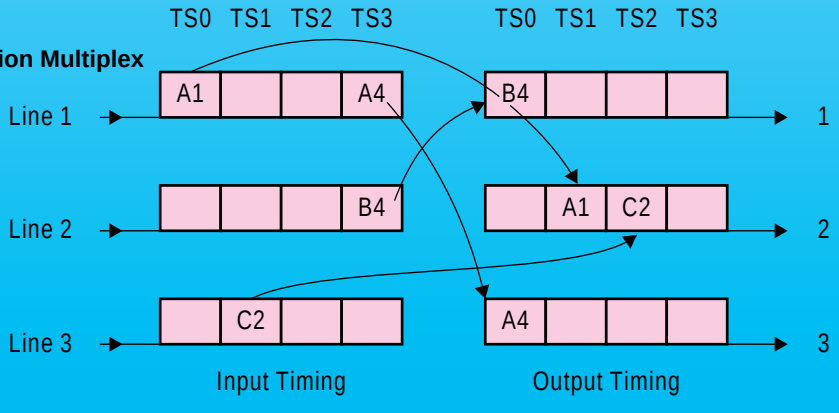
Time-Division Multiplex



Space-Division Multiplex

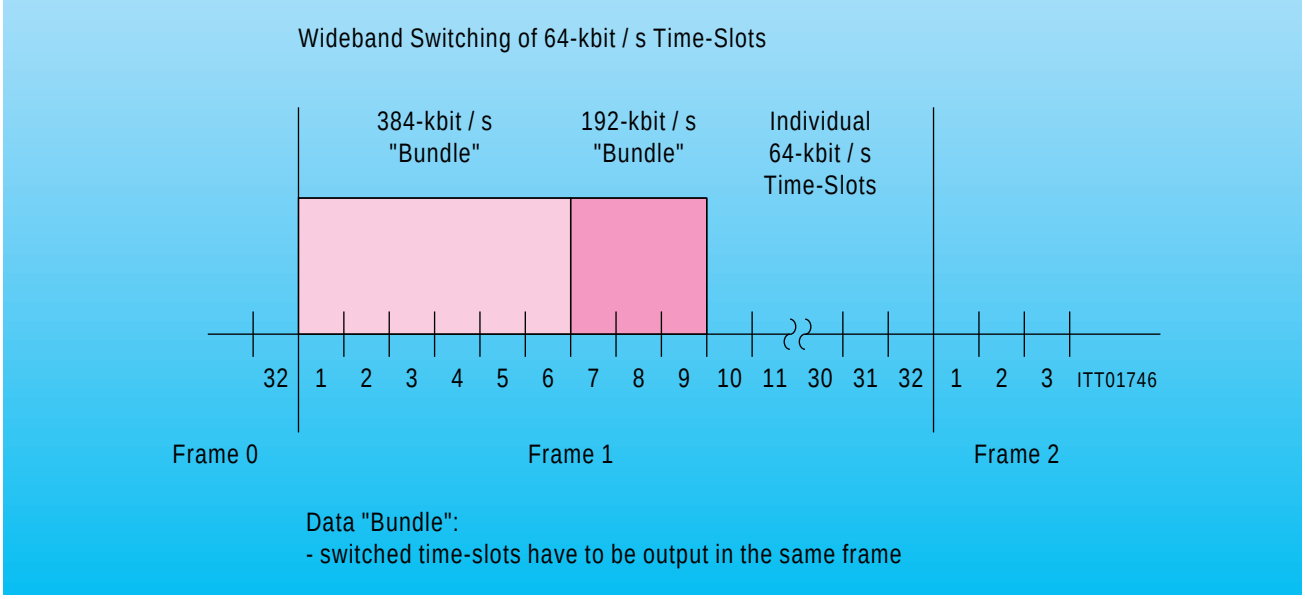


Space/Time-Division Multiplex



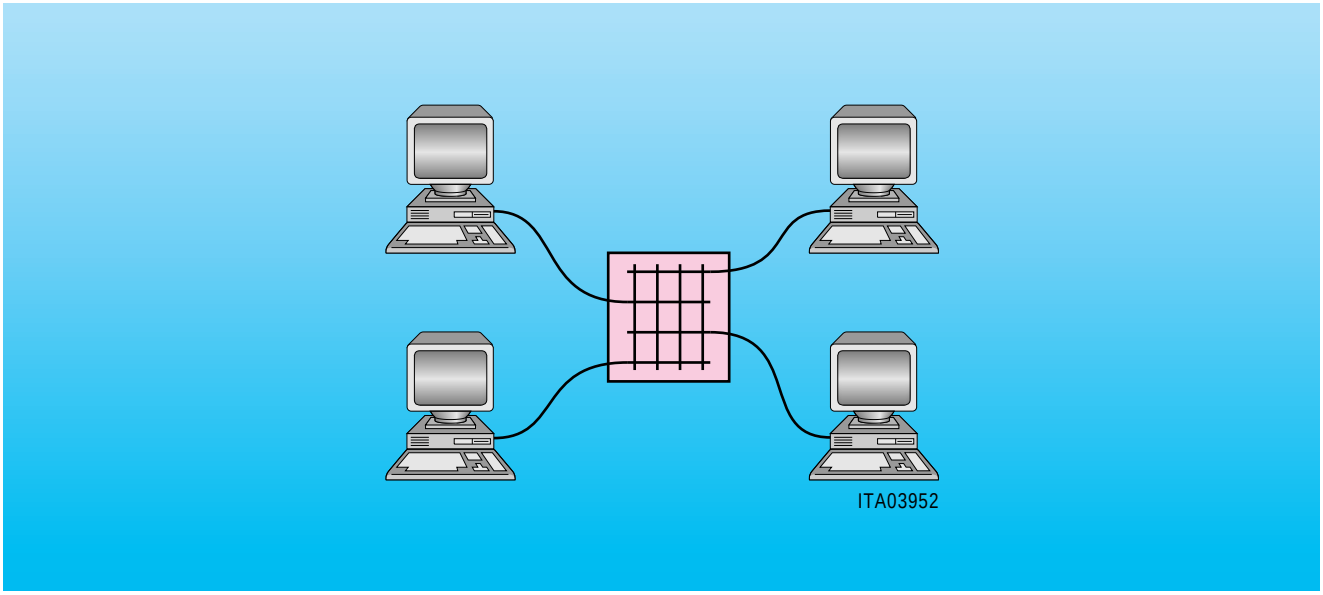
Wideband Switching

An additional future requirement is wideband switching. In contrast to voice switching, wideband switching is optimized for data transmission, e.g. for ISDN H-channels or “Fractional” T1. 64 kbit/s time-slots are combined for higher data rates. As a precondition all switched time-slots have to be output in the same frame. For example 6 time-slots could be combined to a 384-kbit/s bundle.



Multipoint Switching

In a multipoint switching configuration data communication between terminals can be achieved by connecting all stations to one or more time-slots and transmitting the information back. In contrast to audio conferences, data terminals broadcast to the switching matrix which are or-connected. With multipoint switching an independent LAN in a PBX system could be realized.



MTSC

Siemens Semiconductor offers devices which take into consideration the needs for efficient realization of these tasks. One of the switching network circuits offered is the **M**emory **T**ime **S**witch in **C**MOS (MTSC) PEB 2045, which has the ability to connect any of 512 incoming PCM channels to any of 256 outgoing PCM channels on a single chip. A non-blocking switch for 512 time-slots can be built up with two devices only. A further expansion can be realized very easily too. Different kinds of operation modes enable the use of the MTSC PEB 2045 in 2048 Mbit/s, 4096 Mbit/s and 8192 Mbit/s or mixed PCM systems.

As an additional feature the MTSC PEB 2045 together with an **A**dvanced **C**MOS **F**rame **A**ligner (ACFA) PEB 2035 can realize the system interface of up to four primary multiplex access lines.

MTSS

The Memory Time Switch Small (MTSS) PEB 2046 is a smaller version of the MTSC PEB 2045 performing time/ space switch functions for a non-blocking switch of 256 PCM channels.

MTSL/MTSL-16

The largest in our family, the **M**emory **T**ime **S**witch **L**arge (MTSL) PEB 2047 is capable of switching up to 1024 time-slots.

The MTSL allows the switching of fractional T1 and data bundles. The MTSL-16 is a selection for 16-MHz applications.

MUSAC

Siemens Semiconductor also supplies a solution for conferencing, the **M**ultipoint **S**witching **A**nd **C**onferencing Unit (MUSAC) PEB 2245, which performs the complete switching functions of the MTSC, and has a signal processor for handling up to 64 conferencing channels in any combination. The input and output channels can also be attenuated individually to achieve best transmission quality.

MUSAC-A

The MUSAC-A is an upward compatible device to the MTSL and MUSAC. It offers in addition the attenuation and amplification of every time-slot.

An overview on the complete switching and conferencing IC-family is shown in the following table:

Switching, Attenuation and Conferencing IC-Family

	MTSC PEB 2045	**MTSS PEB 2046**	**MTSL PEB 2047**	**MTSL-16 PEB 2047-16**	**MUSAC-A PEB 2445**	**EPIC-1 PEB 2055**	**EPIC-S PEB 2054**
Switching capacity (time-slots)	512 × 256	256 × 256	1024 × 512	1024 × 1024	512 × 256	256 × 256	64 × 256
Input/output lines	‘16/8	‘8/8	‘16/8	‘16/8	‘16/8	‘4/4	‘1/2
PCM-data rate (Mbit/s)	2/4/8 + mixed mode	2	2/4/8 + mixed mode	2/4/8/16 + mixed mode	2/4/8 + mixed mode	up to 8	up to 4
Clock rate (MHz)	4096 8192	4096 8192	4096 8192	4096/8192 16384	4096 8192	up to 8192	2048 8192
Conferencing					64 channels		
Attenuation					all channels – 4 to 12 dB		
PRI/T1 mode	yes				yes		
Fractional T1 data bundling			yes	yes		128 kbit/s channel	
µC access			read	read		yes	yes
Multipoint switching					yes		
Power (mW) max. consumption typ.	50	50	100	170	100	50	50
Package	P-DIP-40-1 P-LCC-44-1	P-DIP-40-1 P-LCC-44-1	P-LCC-44-1	P-LCC-44-1	P DIP-40-1 P-LCC-44-1	P-DIP-40-1 P-LCC-44-1	P-LCC-44-1

General Description

The MTSC PEB 2045 is a monolithic CMOS circuit, which has the ability to connect any of the 512 PCM channels of 16 incoming PCM lines to any of the 256 PCM channels of eight output lines.

The PCM information for a complete frame is stored in the 4-Kbit speech memory SM, i.e. all of the 512 words with 8 bits are written into a fixed position of the SM. This is controlled by the input counter every 125 µs. The words are read using random access with an address that is stored in a connection memory CM for each of the 256 output channels. The access to the CM is controlled by the output counter.

To produce a connection the SM address and the CM address must be written into the PEB 2045 via a µP interface. The SM-address contains the time-slots and line numbers of the incoming PCM words. The CM address consists of the time-slots and line numbers of the output words.

The PEB 2045 can be connected to 2-Mbit/s, 4-Mbit/s and 8-Mbit/s PCM systems, the device clock may be either 4.096 MHz or 8.192 MHz.

In a second operational mode the PEB 2045 together with the PEB 2035 (ACFA, Advanced CMOS Frame Aligner) and the PEB 2235 (IPAT, ISDN Primary Access Transceiver) implements the system interface of up to four primary multiplex access lines. This interface can be configured for 2-Mbit/s, 4-Mbit/s and 8-Mbit/s systems; a clock shift for input and output lines with half clock step resolution is programmable. Selection of operating modes and programming is made by writing to the mode register and, via the Indirect Access Register (IAR), the Clock Shift Register (CSR) and the General Configuration Register (GCR).

The components PEB 2045 and PEF 2045 are functionally identical. The difference between the two types lies in the temperature range. The PEB 2045 operates in the temperature range 0 to 70 °C, the PEF 2045 in the range – 40 to 85 °C.

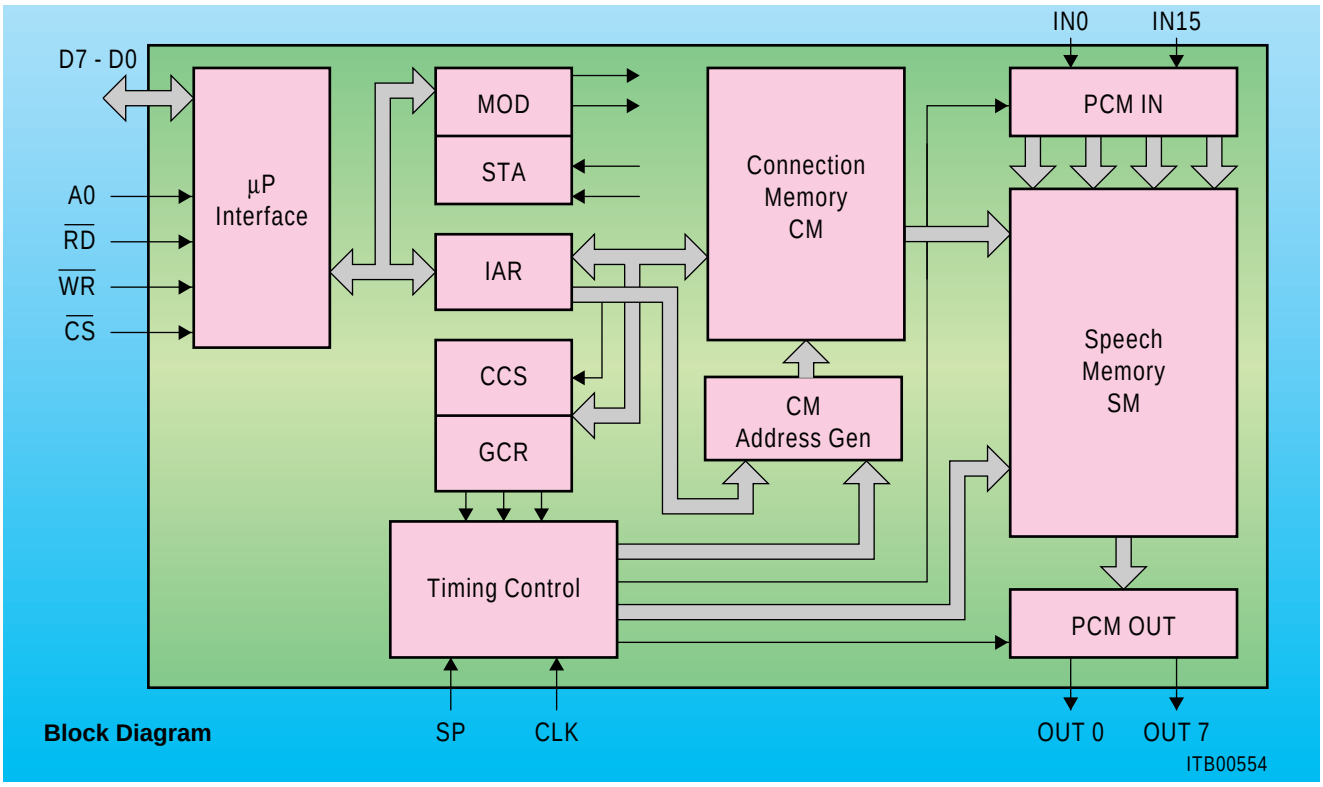
Applications

- All types of switching systems
- Concentrator function
- Frequency transforming interface between 2-Mbit/s, 4-Mbit/s and 8-Mbit/s PCM systems
- 16/16 space switch for 8-Mbit/s PCM systems
- System interface for up to four primary multiplex access lines in combination with the PEB 2035 (ACFA) and *PEB 2235 (IPAT)

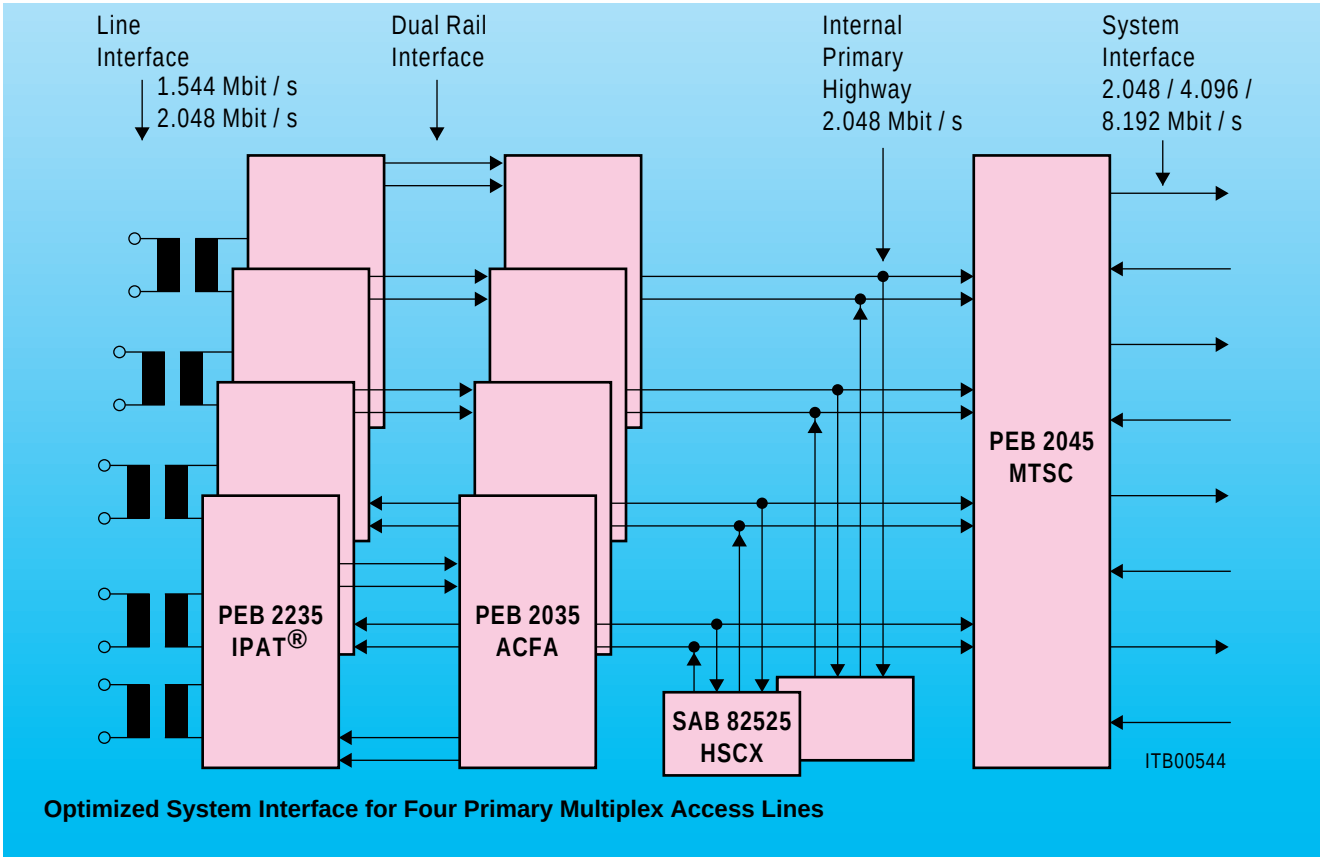
Type	Package
PEB 2045-N	P-LCC-44-1 (SMD)
PEB 2045-P	P-DIP-40-1 (not for new design)
PEF 2045-N	P-LCC-44-1 (SMD)
PEF 2045-P	P-DIP-40-1 (not for new design)

Features

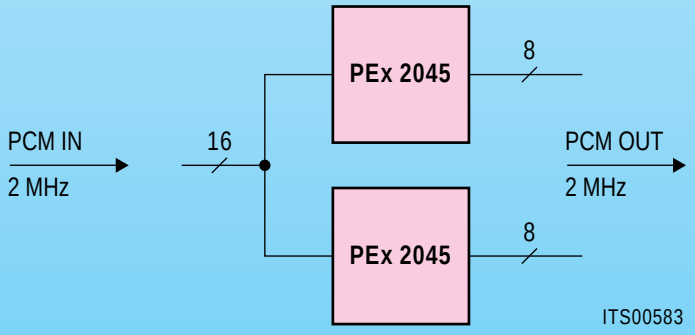
- Time/space switch for 2.048-, 4.096- and 8.192-kbit/s PCM systems
- Different kinds of modes (2048, 4096, 8192 kbit/s or mixed mode)
- Switching of up to 512 incoming PCM channels to up to 256 outgoing PCM channels
- 16 input and eight output PCM lines
- Configurable for primary access and standard applications
- Programmable clock shift with half clock step resolution for input and output in primary access configuration
- Configurable for a 4096- and 8192-kHz device clock
- Tristate function for further expansion and tandem operation
- Tristate control signals for external drivers in primary access configuration
- 2048-kHz clock output in primary access configuration
- Space switch mode
- 8-bit µP interface
- Single + 5-V power supply
- Advanced low power CMOS technology



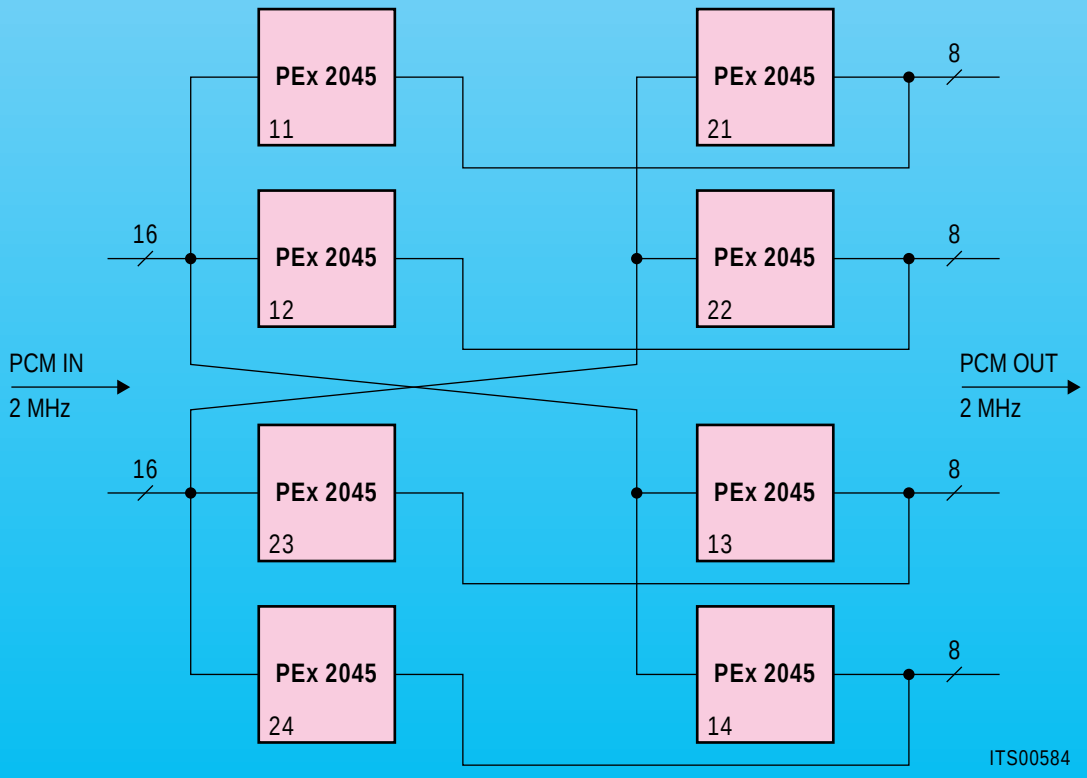
Block Diagram



Optimized System Interface for Four Primary Multiplex Access Lines



Memory time switch 16/16 for a non-blocking 512-channel switch



Memory time switch 32/32 for a non-blocking 1024-channel switch using tristate function

Block Diagram of two PCM Switch Configurations with PEB 2045

General Description

The MTSS PEB 2046 is a monolithic CMOS device which has the ability to connect any of the 256 PCM channels of eight incoming PCM lines to any of the 256 PCM channels of eight output lines.

The input information of a complete frame is stored in the speech memory SM. The incoming 256 channels of 8 bits each are written in sequence into fixed positions in the SM. This is controlled by the input counter in the timing control block with an 8-kHz repetition rate.

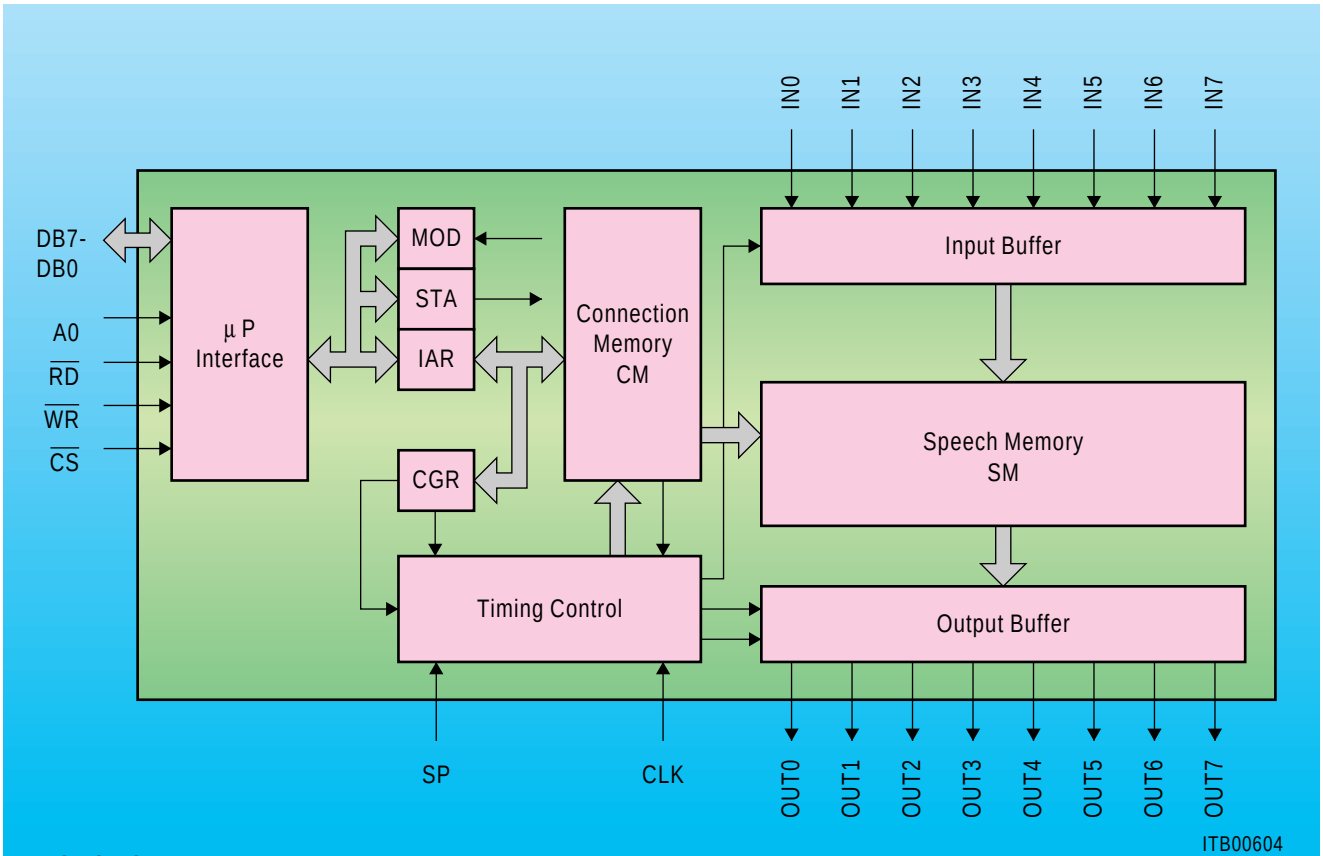
For output, the connection memory (CM) is read in sequence. Each location in CM points to a location in the speech memory. The byte in this speech memory location is read into the current output time-slot. The read access of the CM is controlled by the output counter which also resides in the timing control block.

Thus the CM needs to be programmed beforehand for the desired connection. The CM address corresponds to one particular output time-slot and line number. The contents of this CM-address point to a particular input time-slot and line number (now resident in the SM).

Type	Package
PEB 2046-N	P-LCC-44-1 (SMD)
PEB 2046-P	P-DIP-40-1

Features

- Time/space switch for 2.048-kbit/s PCM systems
- Switching of up to 256 incoming PCM channels to up to 256 outgoing PCM channels
- Eight input and eight output PCM lines
- Configurable for a 4096- and 8192-kHz device clock
- Tristate function for further expansion and tandem operation
- 8-bit µP-interface
- Single +5-V power supply
- Advanced low power CMOS technology

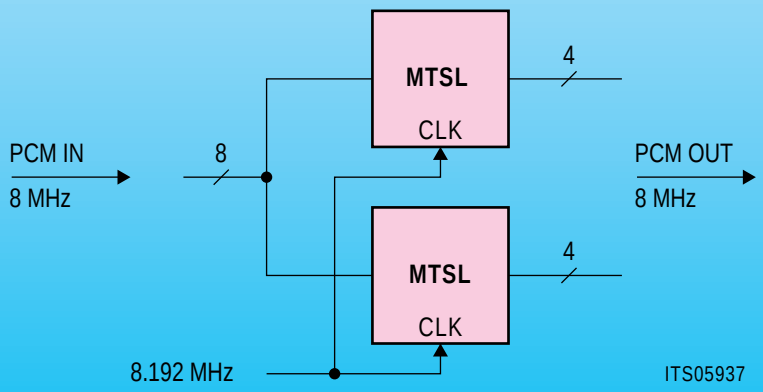


Block Diagram

Features

- Time/space switch for 2048-, 4096- or 8192-kbit/s PCM systems
- Different modes programmable for input and output separately 2048 kbit/s (4096 kbit/s, 8192 kbit/s or mixed mode)
- Switching of up to 1024 incoming PCM channels to up to 5124 outgoing PCM channels
- Configurable for a 4096-kHz or 8192-kHz device clock 16 input and 8 output PCM lines
- Constant frame delay for switching of wideband data, e.g. ISDN H-channels or minimized delay for voice applications
- Tristate function for further expansion and tandem operation
- µP read access to PCM data
- Programmable clock shift with half clock step resolution for input and output
- Individual line delay measurement and clock shift mechanism for 8 PCM inputs
- Built-in selftest
- 8-bit Motorola or Intel type µP interface
- Advanced low power 1 µ-CMOS technology
- Single 5-V-power supply

Type	Package
PEB 2047-N	P-LCC-44-1 (SMD)



Memory Time Switch for a Non-blocking 1024 Channel Switch with 8-MHz Device Clock

General Description

The MTSL PEB 2047 is a memory time switch device. Operating with a device clock of 4096 kHz or 8192 kHz it can connect any of 1024 PCM-input channels to any of 512 output channels.

The input information of a complete frame is stored in the on-chip 8-kbit data memory DM. The incoming 1024 channels of 8 bits each are written in sequence into fixed positions in the DM. This is controlled by the input counter in the timing control block with an 8-kHz repetition rate.

For outputting, the connection memory (CM) is read in sequence. Each location in CM points to a location in the data memory. The byte in this data memory location is transferred into the current output time-slot. The read access of the CM is controlled by an output counter.

The synchronization of this procedure will be achieved by a rising edge of the synchronizing pulse SP, which is always sampled with the falling edge of the device clock.

Different modes of operation are configurable at the PCM-input interface. Also, 8 PCM-input lines can be synchronized with individual clock shift values to compensate different line delays. If more than 8 inputs are used one clock shift value controls up to two ports at the same time.

The input lines IN8 to IN15 can be used as additional frame-synchronization inputs FS. After synchronizing the device by the SP pulse, the FS inputs can be evaluated on a per port basis. This evaluation procedure is started by a microprocessor command. As a result the input countervalue on the rising edge of the FS signal can be read from an internal register. Thus delay compensation is easily managed by programming appropriate clock shift values and/or a possible software offset.

During operation of the chip, a frame length check, which controls correct synchronization by the SP pulse and generates an interrupt in case of lost or achieved synchronization is also supplied.

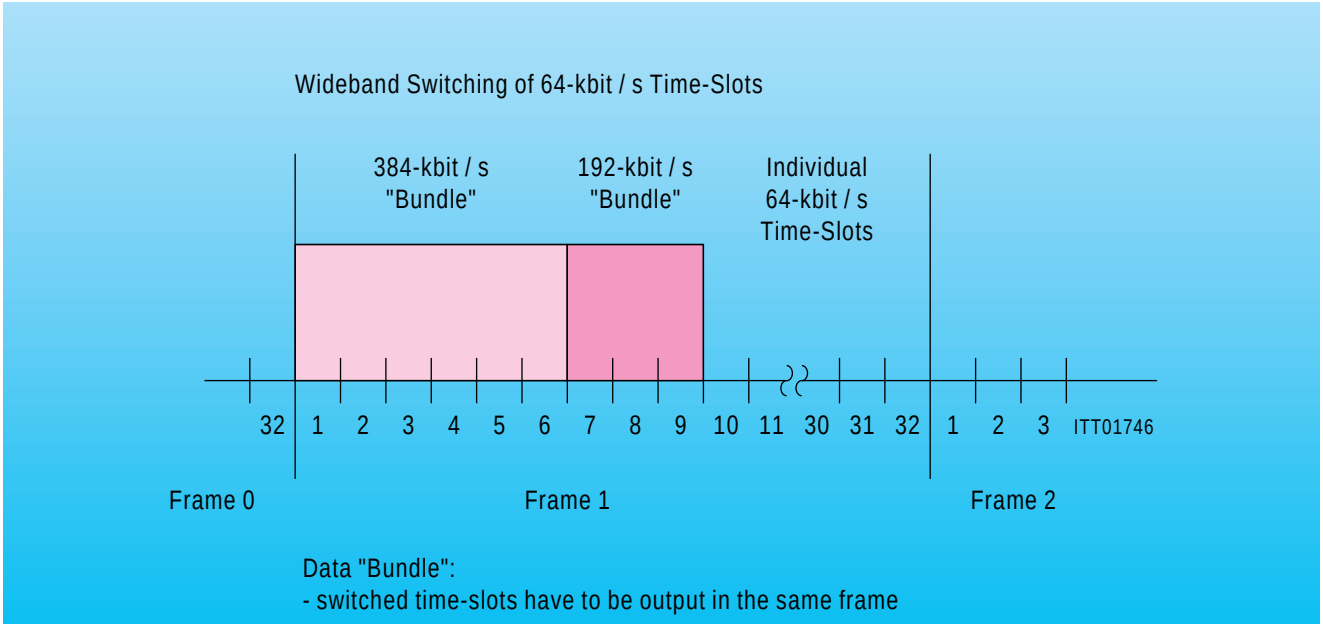
The standard 8-bit µP interface can communicate with Intel multiplexed/demultiplexed microprocessors as well as with Motorola demultiplexed processors. It gives access to the internal registers and to the control – and data memory. Five directly addressable registers are provided. All other registers and the memories are accessed by a simple three byte indirect access method (similar to the MTSC PEB 2045).

The switching path of the MTSL including input buffer, data memory, control memory, output buffer and timing control can be tested in the system by a built-in selftest. After activating this mechanism it takes 1.25 ms (8192 kHz) until the result “selftest ok/selftest not ok” can be read from the internal status register.

After test completion the control-memory is also reset.

In applications where 64-kbit/s channels are combined for higher data rates (e.g. ISDN H-channels) the MTSL ensures that all switched time-slots are output in the same frame.

In voice applications where a low delay is important, the MTSL can be programmed for minimized switching delays.



MTSL Submultiplexing of 64-kbit/s Time-Slot

General Description

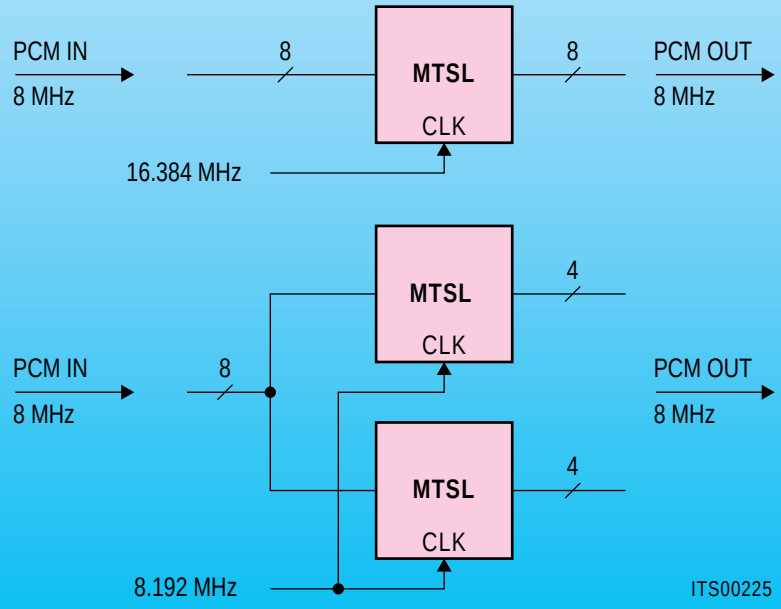
The MTSL-16 is an upward compatible device to the MTSL. The MTSL-16 supports 16-MHz clocking and switching capability of 1024 × 1024 time-slots.

Features

- Upward compatible to MTSL
- Time/space switch for 2048-, 4096-, 8192- or 16384-kbit/s PCM systems
- Different modes programmable for input and output separately (2048-, 4096-, 8192- or 16384-kbit/s or mixed mode)
- Switching of up to 1024 incoming PCM channels to up to 1024 outgoing PCM channels
- Configurable for a 8192-kHz or 16384-kHz device clock
- 16 input and 8 output PCM lines
- Constant frame delay for switching of wideband data, e.g. ISDN H-channels or minimized delay for voice applications

Type	Package
PEB 2047-16-N	P-LCC-44-1 (SMD)

- Tristate function for further expansion and tandem operation
- µP access to PCM data
- Programmable clock shift with half clock step resolution for input and output
- Individual line delay measurement and clock shift mechanism for 8 PCM inputs
- Built-in selftest
- 8-bit Motorola or Intel type µP interface
- Advanced low power 1-µ CMOS technology
- Single 5-V-power supply



Memory Time Switch for a Non-blocking 1024 Channel Switch with 16-MHz Device Clock

General Description

The MUSAC-A is an upward compatible device to the components MTSC and MUSAC. Additionally to the standard MUSAC features switching and conferencing, the MUSAC-A supports additional attenuation functions.

Every time-slot is freely programmable in 1-dB step resolutions to an attenuation range from 0 to 12 dB and amplified from 0 to 4 dB.

With enlarged attenuation functions to every time-slot the MUSAC-A fulfills the ability for new requirements. I.e. different PBX terminals could be adapted to a certain reference point from the private network to the public network.

Features

Switching

- Time/space switch for 2048-, 4096- or 8192-kbit/s PCM systems
- Switching of up to 512 incoming PCM channels to up to 256 outgoing PCM channels
- 16 input and 8 output PCM lines
- Different kinds of modes (2048, 4096, 8192 kbit/s or mixed mode)
- Configurable for a 4096- and 8192-kHz device clock
- Tristate function for further expansion and tandem operation

Attenuation and Amplification

- Attenuation and amplification of every time-slot
- Attenuation range from 0 to 12 dB
- Amplification range from 0 to 4 dB

Type	Package
PEB 2445-N	P-LCC-44-1 (SMD)

Conference Mode

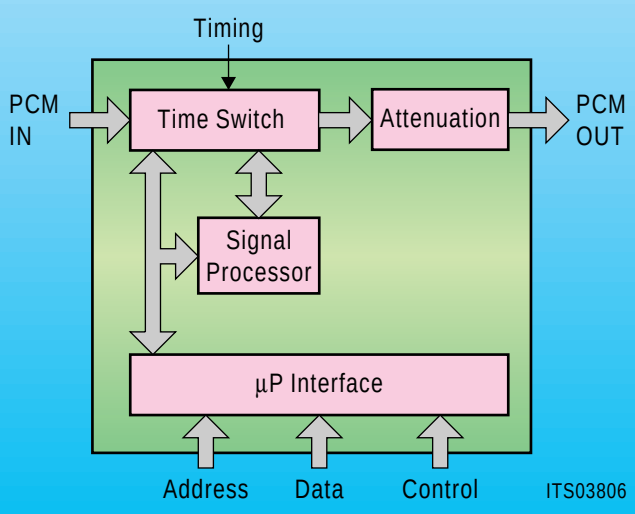
- Up to 64 conference channels in any combination
- Up to 21 independent conferences simultaneously (3 subscribers)
- Programmable attenuation (0/3/6/9 dB) on each input channel
- Programmable attenuation (0/3 dB) on each output channel
- Programmable PCM-level adaption (attenuation or amplification) of up to 64 channels
- Programmable noise suppression (four thresholds)
- Conference overflow handling
- Tone insertion capability
- A-Law/µ-Law compatible
- Compatible with all kinds of PCM-byte formats

Multipoint Switching

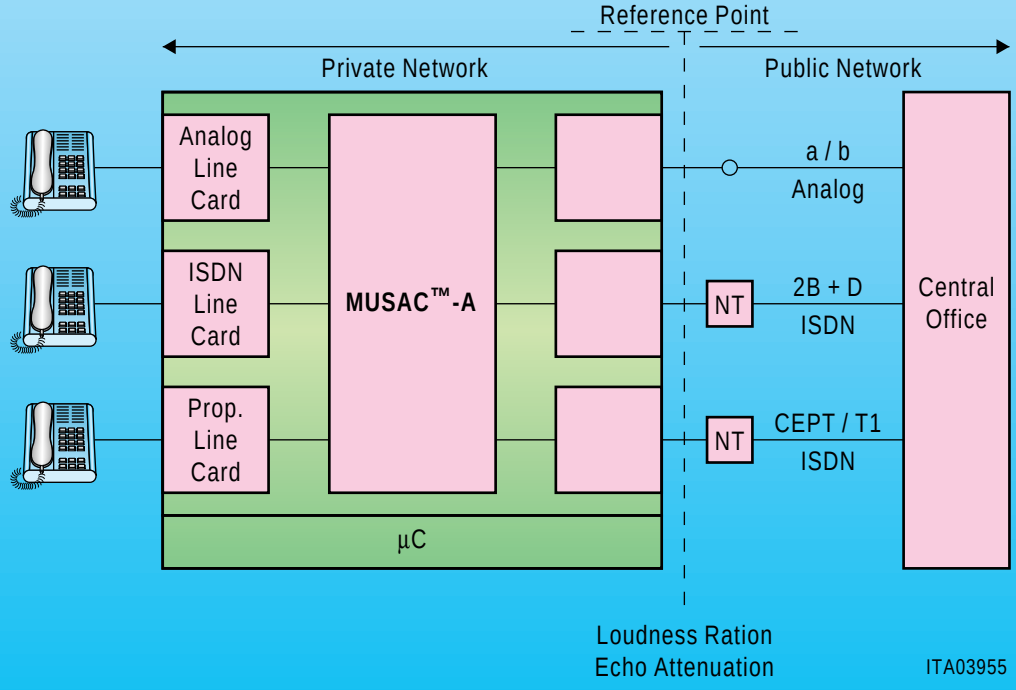
- Multiple independent LAN s within one PBX
- Multiplexing of up to 64 channels
- 64-kbit/s channels

General

- 8-bit µP interface
- Single + 5-V-power supply
- Advanced low power CMOS technology
- TTL compatible inputs/outputs
- Upward compatible to MTSL



Block Diagram



PBX-Example Attenuation for Every Time-Slot

Multichannel Network Interface Controller for HDLC
MUNICH32; PEB 20320

Communication Network ICs

Product Overview

Type	Short Title	Function	Page
SAB 82525 SAB 82526	HSCX HSCX1	High-Level Serial Communication Controller Extended	162
SAB 82532	ESCC2	Enhanced Serial Communication Controller (2 channels)	163
SAB 82538	ESCC8	Enhanced Serial Communication Controller (8 channels)	165
SAB 82518	ASCC8	Universal Asynchronous Reciever/Transmitter (UART)	161
PEB 20320	MUNICH32	Multichannel Network Interface Controller for HDLC	167
SAB 82C257 SAB 82C528A	ADMA	Advanced DMA Controller for 16-bit Microcomputer Systems	169

A World of Applications

Data communication has gained a key role in modern computer systems. We are on the threshold of an era of total communication: every (micro)computer unit has to be able to communicate with other devices – either in synchronous or asynchronous data transmission mode.

Let us have a look at this rapidly growing world of many different applications. There are among others the following applications: telecom, office automation, traffic control, medical equipment, and factory automation.

Telecom

Todays telephone and telecommunication equipment is getting more and more digitalized while the older analog units are being replaced. This means that analog signals are converted to digital data as soon as possible before being transferred and processed. Back-conversion is made as late as possible. Consequently the amount of transferred data in telecom applications is increasing tremendously. Depending on the desired data throughput and transmission mode, the designer always gets the right choice with serial communication ICs from Siemens. There are a lot of goals to be met: transfer control by high level transportation protocols, transmitting and receiving data pockets, time-division multiplexing in time-slot systems, handling of different data encoding/decoding schemes, etc.

All these kinds of data transfer can be managed by SAB 82525 or SAB 82526. These ICs are called High-Level Serial Communication Controllers Extended (HSCX, SAB 82525) and Single-Channel High-Level Serial Communication Controllers Extended (HSCX1, SAB 82526). They were especially designed for serial communication interfaces in telecom networks requiring HDLC based protocols.

Typical HSCX applications are network communication boards, central D-channel signaling, DMI boards, data-link controllers in digital mobile radio networks as well as cordless telephone sets.

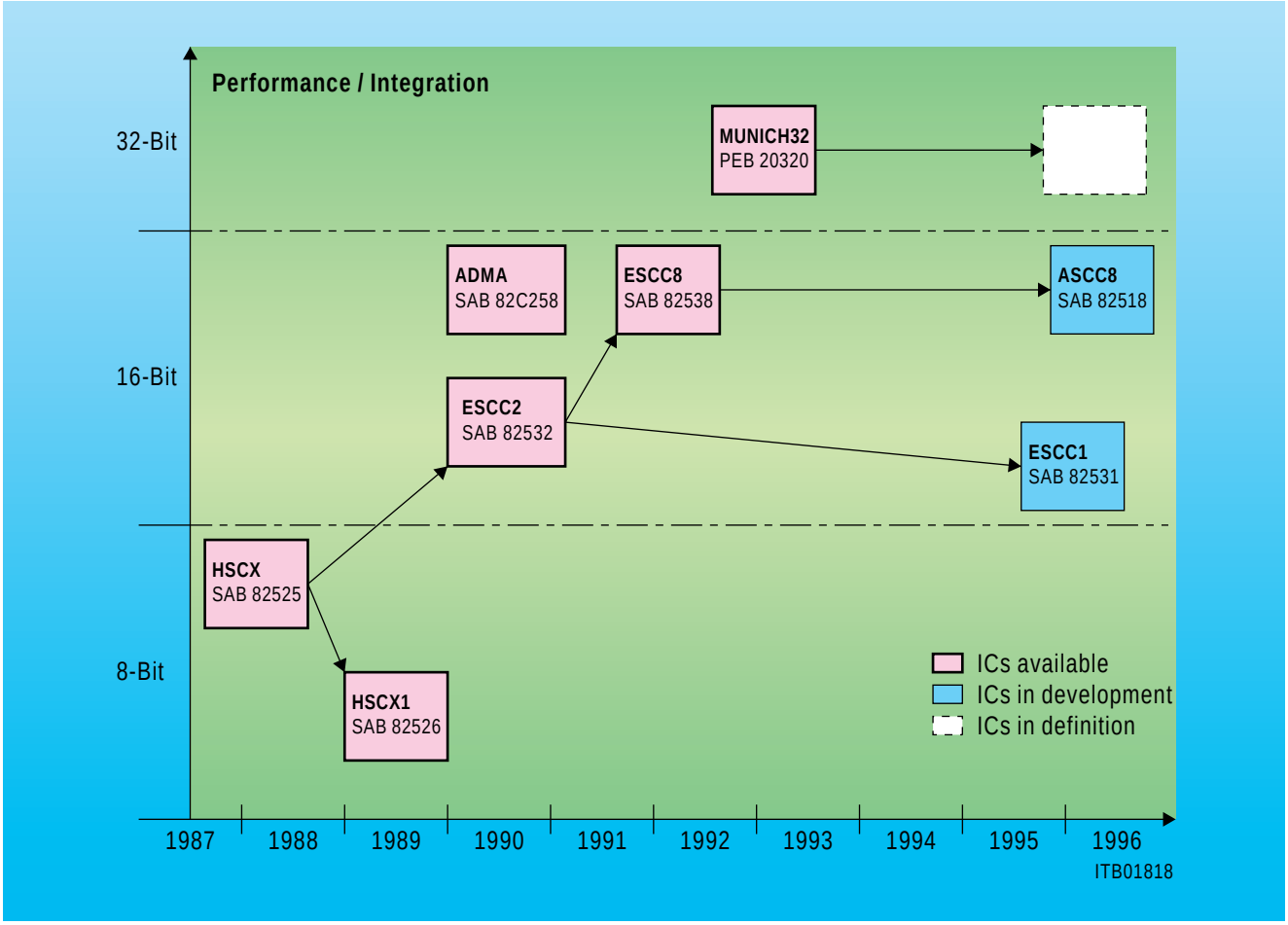
Office Automation and Wide Area Networks (WAN)

Typical ESCC2 (Enhanced Serial Communication Controller with 2 channels, SAB 82532) applications are communication boards for workstations and minicomputers as well as I/O multiplexers, bridges and gateways (X.24, PRI). ESCC2 can be used for nearly all applications from terminal adaptors and fast HDLC links to Primary Rate Interfaces (T1/S2) or ISDN interfaces (SO); using unique software.

If the designer requires multichannel access, he can save a tremendous amount of board space by using the highly integrated eight-channel multiprotocol controller SAB 82538 (ESCC8): four ESCC2s (eight serial channels) in one package.

Fast LANs

If clock recovery up to 4 Mbit/s is needed (e.g. in fiberoptic transmission systems), the designer can use ESCC2 (Enhanced Serial Communications Controller, SAB 82532). Basically, the ESCC2 is a faster 16-bit HSCX with a big bundle of extra functions. HDLC-data transfer can be implemented up to 10 Mbit/s. ESCC2 is a multiprotocol controller which enables designers to use synchronous, bisynchronous as well as asynchronous, fast data transfer with one chip on one software basis.



Siemens' family of serial communication controllers comprises a full range of different ICs. While each of them is designed to enhanced particular features, together they compose a wide profile of performance. Thus, most likely our family of complementary devices offers an ideal solution to many applications in serial data communications.

HSCX

The High-Level Serial Communications Controller Extended (HSCX) supports a number of synchronous standardized protocols and a greater number of proprietary protocols at a transfer rate of up to 4 Mbit/s. Each of its two channels works independent of the other. Its specific fields of application are proprietary HDLC local area networks (LAN).

HSCX 1

The Single-Channel High-Level Serial Communications Controller Extended (HSCX1) is the single channel version of HSCX.

ESCC2

The Enhanced Serial Communications Controller (ESCC2) is a multiprotocol controller offering an extraordinary profile of protocol options at a high-speed transfer rate of up to 10 Mbit/s for each of its two independent channels.

ESCC2 was developed for the different communication requirements of wide area network, local area network, small area network and proprietary network applications.

The result is a communications controller as a standard for implementing Open System Interconnection (OSI) layers-1 and -2 in all these applications. This fact noticeably reduces development and system costs.

The board space, for example, is reduced by on-chip collision detection and resolution, programmable preamble, clock recovery, the logic for multiple protocols and multiple encodings, 16- and 32-bit CRC, time-slot, assignment, queued interrupt status for all important events like receiver FIFO full, receiver FIFO overrun and end of frame transmission.

Features Type	HSCX1 SAB 82526	HSCX SAB 82525	ESCC2 SAB 82532	ESCC8 SAB 82538	ASCC8 SAB 82518	MUNICH32 PEB 20320
Number of serial channels	1	2	2	8	8	32
Parallel ports	no	no	8-bit	28-bit	28-bit	no
Serial communication	SYNC	SYNC	SYNC/ASYNC	SYNC/ASYNC	ASYNC	SYNC
Supported protocols	HDLC/SDLC	HDLC/SDLC	HDLC/SDLC ASYNC/ BISYNC	HDLC/SDLC ASYNC/ BISYNC	ASYNC	HDLC/SDLC
Encoding schemes	NRZ, NRZI	NRZ, NRZI	NRZ, NRZI FM0, FM1 Manchester	NRZ/NRZI FM0, FM1 Manchester	NRZ	NRZ
Programmable preamble	no	no	yes	yes	no	no
CRC	16-bit	16-bit	16-/32-bit	16-/32-bit	–	16-/32-bit
Max baud rate/channel (SYNC)	4 Mbit/s	4 Mbit/s	10 Mbit/s	10 Mbit/s	–	4 Mbit/s/128 Kbit/s
Max baud rate/channel (ASYNC)	–	–	2 Mbit/s	2 Mbit/s	2 Mbit/s	–
Integrated clock recovery (DPLL) up to	1.2 Mbit/s	1.2 Mbit/s	2 Mbit/s	2 Mbit/s	no	no
FIFO size per channel (R × D/T × D)	64/64 bytes	64/64 bytes	64/64 bytes	64/64 bytes	64/64 bytes	256/256 bytes
Data-bus width	8-bit	8-bit	8-/16-bit	8-/16-bit	8-/16-bit	16-/32-bit
Data bus types	Intel/Motorola	Intel/Motorola	Intel/Motorola	Intel/Motorola	Intel/Motorola	Intel/Motorola
DMA controller on-chip	no	no	no	no	no	yes
DMA support	yes	yes	yes	yes	yes	–
Time-slot assignment	yes	yes	yes	yes	no	yes
Package	P-LCC-44	P-LCC-44 P-MQFP-44	P-LCC-68	P-MQFP-160	P-MQFP-160	P-MQFP-160

The reduction of the software size, due to the 16-bit Intel or Motorola processor interface, the direct register accessibility, large FIFOs, vectorized interrupts and four channel DMA support lead to higher performance and decrease CPU time to an absolute minimum.

Less system cost, less development cost, less board space, less power consumption and high performance in a proven 1-µm CMOS technology are what you gain by using this communication genius as a standard for all your applications.

The following ICs are in development or under definition and will be available in due time to offer new attractive solutions for serial communication control.

ESCC8

The eight-channel Enhanced Serial Communications Controller (ESCC8) offers eight independent serial channels. Basically it consists of four ESCC2 cores. It is a very suitable solution for multiprotocol and multichannel applications.

MUNICH32

The Multichannel Network Interface Controller for HDLC (MUNIC32) is a protocol controller for handling up to 32 data channels of a full-duplex PCM highway. It has been designed for use in fractional T1 interfaces as well as for applications in switching systems.

ADMA

The Advanced DMA Controller (ADMA) is a four channel I/O coprocessor that is optimized to handle data transfers in either 8-, 16- or 32-bit microprocessor systems. It can transfer up to 40 Mbytes of data per second in a 20-MHz system. The ADMA transfers data using single cycle, two cycle and 32-bit fly by operations and can gather or scatter data with efficient linked list data chaining, making it one of the most versatile DMA controllers available today. A smaller, reduced cost version of the ADMA (SAB 82C257) is also available.

ASCC8

The ASCC8 is an eight-channel Universal Asynchronous Receiver/Transmitter (UART). It is optimized to handle eight high-speed asynchronous channels at rates of up to 2 Mbit/s in 16-×-oversampling mode. The ASCC8 is ideally suited for applications that include card-to-card signaling MODEM pools, asynchronous routers, and simple high speed point-to-point communications between processing elements within a large system.

General Description

The HSCX (SAB 82525) has been designed to implement high speed communication links using HDLC protocols and to reduce the hard and software overhead needed for serial synchronous communications.

Due to its 8-bit demultiplexed adaptive bus interface it fits perfectly into every INTEL or Motorola 8- and 16-bit microcomputer system.

The HSCX directly supports the X.25 LAPB, the ISDN LAPD- and SDLC protocols and is capable of handling a large set of layer-2 protocol functions independently from the host processor.

The time division capability of the SAB 82525 and other programmable telecom features make it suitable for time-slot oriented PCM systems designed for packet switching. Due to its high speed data transfer and high level protocol support it fits very well in industrial applications e.g. laser printers.

The HSCX1 (SAB 82526), the single channel version of the HSCX, opens another wide application area.

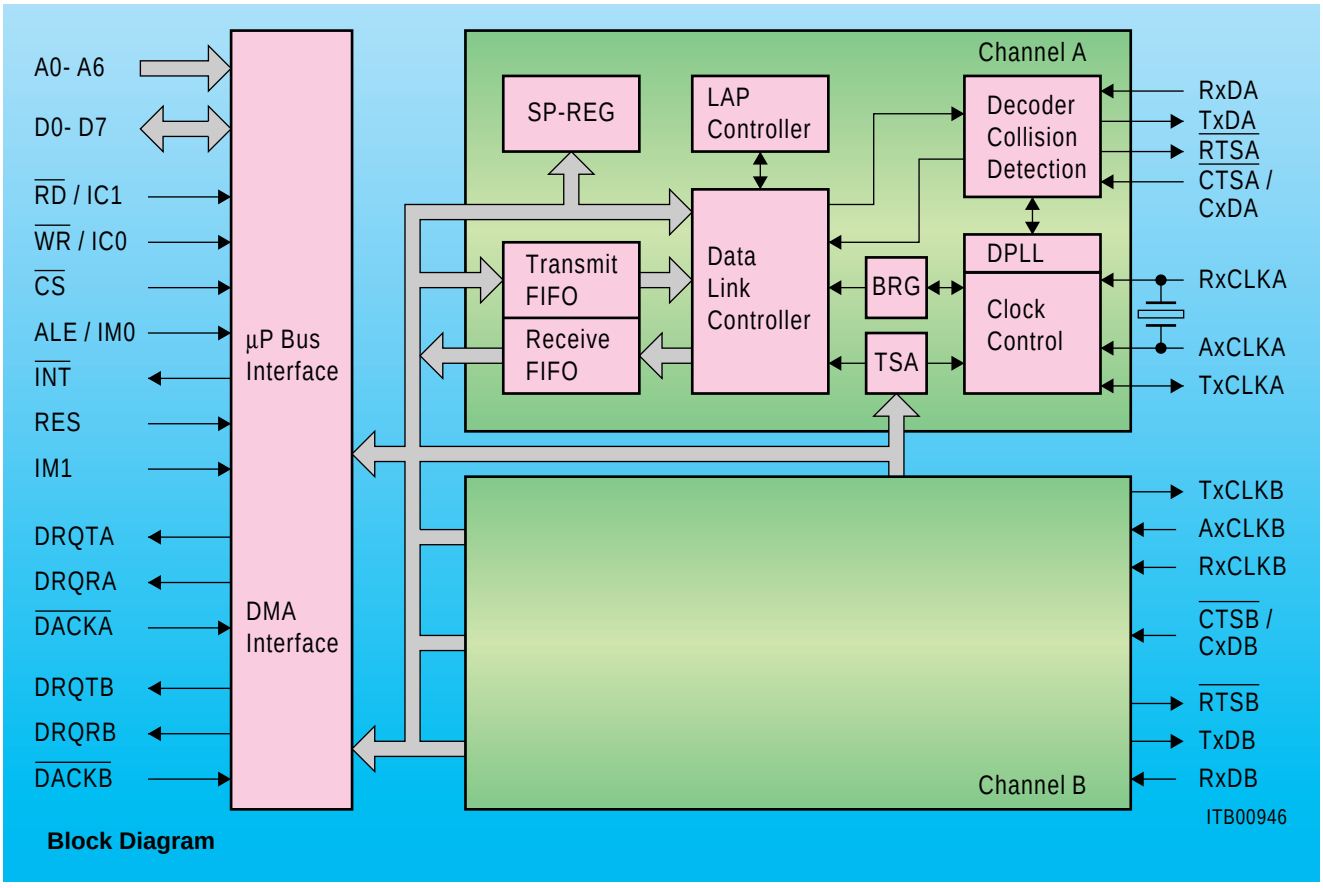
For an easy access to the wide variety and complexity of synchronous data transfer Siemens provides a PC based HSCX evaluation Kit.

The SAB 82525/82526 operates in the temperature range 0 to 70 °C, the SAF 82525/82526 in the range -40 to 85 °C.

Type	Package
SAB 82525-N	P-LCC-44-1 (SMD)
SAF 82525-N	P-LCC-44-1 (SMD)
SAB 82526-N	P-LCC-44-1 (SMD)
SAF 82526-N	P-LCC-44-1 (SMD)
SAB 82525-H	P-MQFP-44-1 (SMD)

Features SAB 82525 (82526)

- Two (one) independent HDLC/SDLC channels
- High level support of LAPB/LAPD protocols
- Oscillator DPLL and baud rate generator for each channel
- Collision detect and resolution logic
- Data rate up to 4 Mbit/s
- Clock recovery up to 1.2 Mbit/s
- 8 bit parallel multiplexed and demultiplexed system bus adaption
- 64-byte FIFO per channel and direction
- 4 (2) channel DMA interface
- CMOS technology



Block Diagram

General Description

The Enhanced Serial Communication Controller ESCC2 (SAB 82532) is a multiprotocol data communication controller with two symmetrical serial channels. It has been designed to implement high speed communication links and to reduce hardware and software overhead needed for serial synchronous/asynchronous communications.

The version 82532N-10 of the ESCC2 opens a wide area for application which use time division multiplex methods (e.g. time-slot oriented PCM systems, systems designed for packet switching, ISDN applications).

General Features

Serial Interface

- Two independent full-duplex serial channels
  - On-chip clock generation or external clock source
  - On-chip DPLL for clock recovery of each channel
  - Two independent baud rate generators
  - Independent time-slot assignment for each channel with programmable time-slot length (1 - 256 bits)
- Async, sync character oriented (MONOSYNC/BISYNC) or HDLC/SDLC modes (including SDLC LOOP)
- Transparent receive/transmit of data bytes without framing
- NZR, NRZI, FM and Manchester encoding
- Modem control lines ($\overline{RTS}$, $\overline{CTS}$, CD)
- CRC support:
  - HDLC/SDLC: CRC-CCITT or CRC-32
  - (automatic handling for transmit/receive direction)
  - BISYNC: CRC-16 or CRC-CCITT
  - (support for transmit direction)
- Support of bus configuration by collision detection and resolution
- Statistical multiplexing
- Continuous transmission of 1 to 32 bytes possible
- Programmable preamble (8 bit) with selectable repetition rate (HDLC/SDLC and BISYNC)
- Data rate up to 10 Mbit/s
- Master clock mode with data rate up to 4 Mbit/s

Applications

- Universal, multiprotocol communication board for Workstation- and PC-boards
- Terminal controllers
- Computer peripherals
- Time-slotted packet networks
- Multimaster communication networks
- LANs

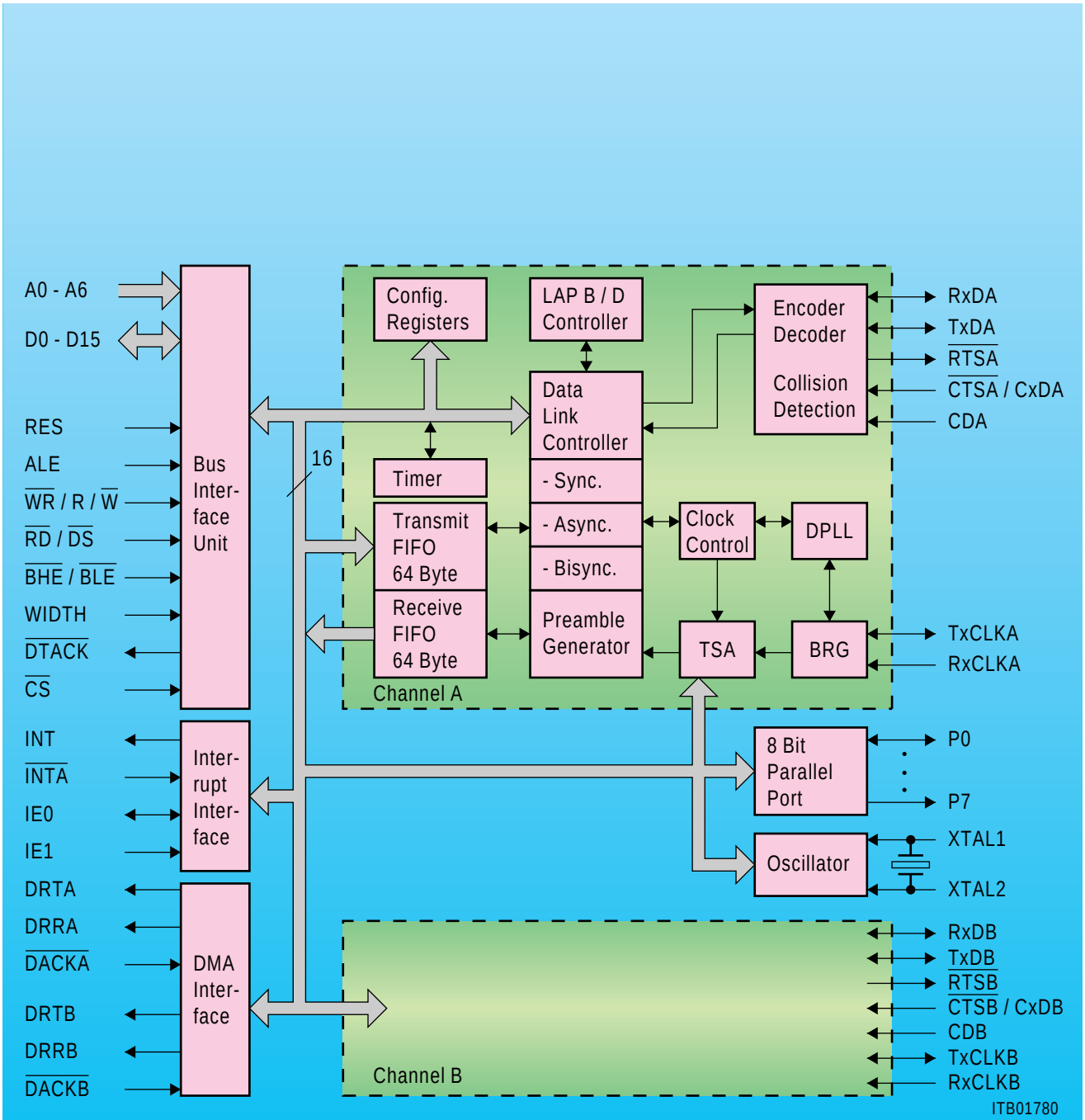
Type	Package	Max. Data Rate Clocked		Time-Slot Mode
		ext.	int. (DPLL)	
SAB 82532-N	P-LCC-68-1	2 Mbit/s	2 Mbit/s	no
SAB 82532-N-10	P-LCC-68-1	10 Mbit/s	2 Mbit/s	yes

Protocol Support (HDLC / SDLC)

- Various types of protocol support depending on operating mode
  - Auto-mode (automatic handling of S- and I-frames)
  - Non-auto mode
  - Transparent mode
- Handling of bit oriented functions
- Support of LAPB / LAPD / SDLC / HDLC protocol in auto-mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable time-out and retry conditions
- Programmable maximum packet size checking

MP Interface and Ports

- 64-byte FIFOs per channel and direction (byte or word access)
- 8/16-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte and work access)
- Efficient transfer of data blocks from/to system memory via DMA or interrupt request
- Support of Daisy Chaining and Slave Operation with Interrupt Vector generation
- 8-bit programmable bidirectional universal port



Block Diagram

General Description

The Enhanced Serial Communication Controller ESCC8 (SAB 82538) is a data communication device with eight serial channels. It has been designed to implement high speed communication links and to reduce hardware and software overhead needed for serial synchronous/asynchronous communications.

The version 82538 H-10 of the ESCC8 opens a wide area for application which use time division multiplex methods (e.g. time-slot oriented PCM systems, systems designed for packet switching, ISDN applications).

General Features

Serial Interface

- Eight independent full-duplex serial channels
- On-chip clock generation or external clock source
- On-chip DPLL for clock recovery of each channel
- Eight independent baud rate generators
- Independent time-slot assignment for each channel with programmable time-slot length (1 - 256 bits)
- Async., sync. character oriented (MONOSYNC BISYNC) or HDLC/SDLC modes (including SDLC LOOP)
- Transparent receive/transmit of data bytes without framing
- NZR, NRZI, FM and Manchester encoding
- Modem control lines ($\overline{RTS}$, $\overline{CTS}$, CD)
- CRC support:
  – HDLC/SDLC: CRC-CCITT or CRC-32 (automatic handling for transmit/receive direction)
  – BISYNC: CRC-16 or CRC-CCITT (support for transmit direction)
- Support of bus configuration by collision detection and resolution
- Statistical multiplexing
- Continuous transmission of 1 to 32 bytes possible
- Programmable preamble (8 bit) with selectable repetition rate (HDLC/SDLC and BISYNC)
- Data rate up to 10 Mbit/s
- Master clock mode with data rate up to 4 Mbit/s

Applications

- Universal, multiprotocol communication board
- Asynchronous and synchronous terminal cluster controllers
- LAN gateways and bridges
- Multiplexers, cross-connect points, DMI boards
- Time-slotted packet networks
- Packet switches, packet assemblers/disassemblers

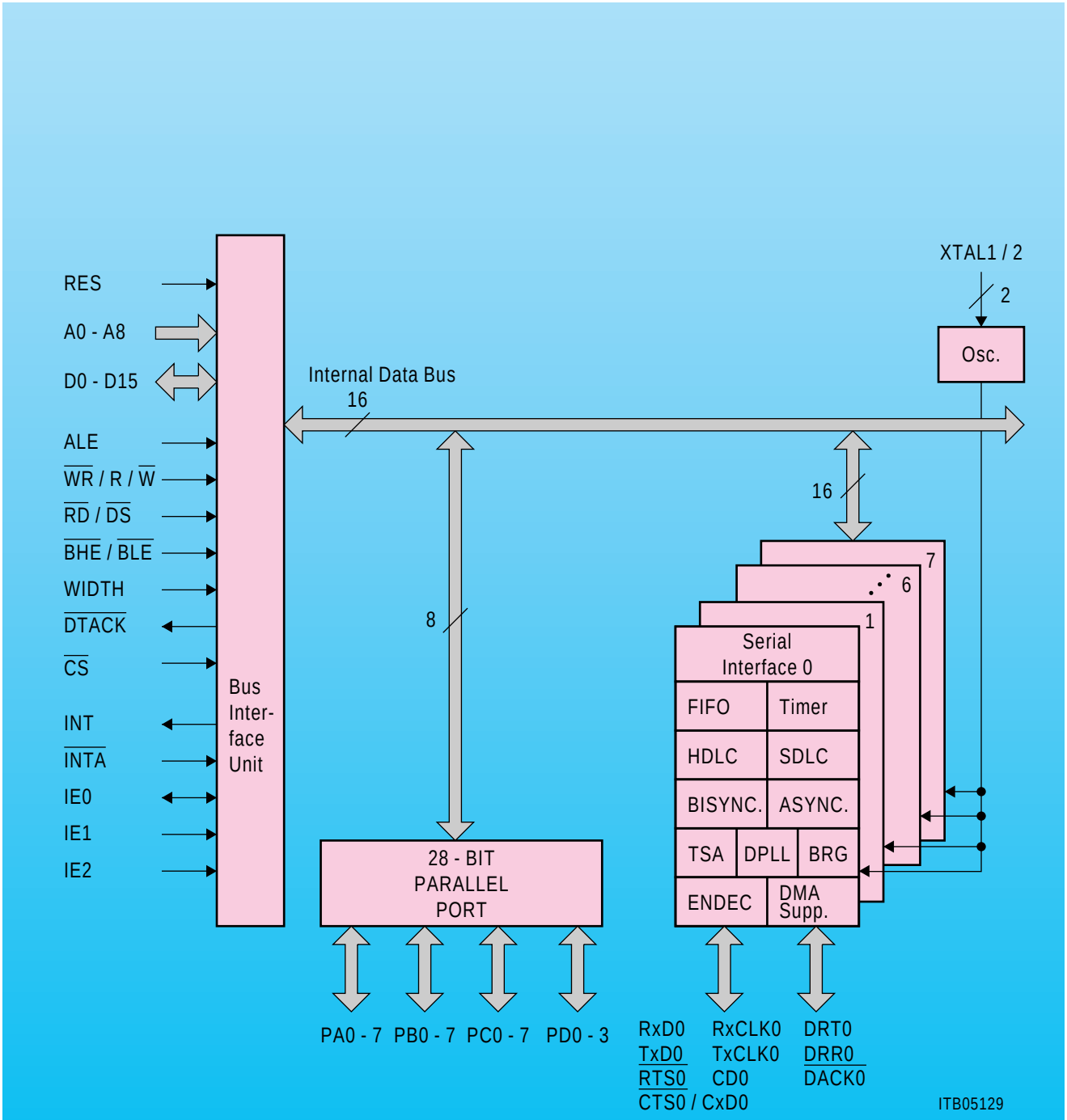
Type	Package	Max. Data Rate Clocked		Time-Slot Mode
		ext.	int. (DPLL)	
SAB 82538-H	P-MQFP-160-1	2 Mbit/s	2 Mbit/s	no
SAB 82538-H-10	P-MQFP-160-1	10 Mbit/s	2 Mbit/s	yes

Protocol Support (HDLC / SDLC)

- Various types of protocol support depending on operating mode
  – Auto-mode (automatic handling of S- and I-frames)
  – Non-auto mode
  – Transparent mode
- Handling of bit-oriented functions
- Support of LAPB / LAPD / SDLC / HDLC protocol in auto-mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable time-out and retry conditions
- Programmable maximum packet size checking

MP Interface and Ports

- 64-byte FIFOs per channel and direction (byte or word access)
- 8/16-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte and word access)
- Efficient transfer of data blocks from/to system memory via DMA or interrupt request
- Support of Daisy Chaining and Slave Operation with Interrupt Vector generation
- 28-bit programmable universal I/Os



Block Diagram

General Description

The Multichannel Network Interface Controller for HDLC (MUNICH32, PEB 20320) is a multichannel protocol controller which handles up to 32 data channels of a full-duplex PCM highway. It performs layer-2 HDLC formatting/deformatting or transparent modes of the DMI protocol, passing on data to an external memory shared with one or more processors.

The MUNICH32 is compatible with the LAPD ISDN (Integrated Services Digital Network) protocol specified by CCITT as well as with HDLC, SDLC, LAPB DMI protocols. It provides any rate adaptation for time-slot transmission data rates from 64 kbit/s, 56 kbit/s down to 8 kbit/s as well as the concatenation of any time-slots to data channels supporting ISDN superchannels.

The MUNICH32 can be used in a wide area of communication applications, e.g. in gateways with fractional T1 interface, I/O multiplexers, central office switches or for the connection of a digital PBX to a host computer or as a central D-channel handler for 32 ISDN basic-access D-channels. Up to four MUNICH32s can be connected to one PCM highway to implement a controller for 128 D-channels.

The PEB 20320 operates in the temperature range 0 to 70 °C, the PEF 20320 in the range -40 to 85 °C.

Features

Serial Interface

- Up to 32 independent communication channels
- Serial multiplexed (full-duplex) input/output for 2048-, 4096-,1544- or 1536-kbit/s PCM highways

Dynamic Programmable Channel Allocation

- Compatible with T1/DS1 24-channel and CEPT 32-channel PCM byte format
- Concatenation of any, not necessarily consecutive, time-slot to superchannels independently for receive and transmit direction
- Support of H0, H11, H12 ISDN channels
- Subchannelling on each time-slot possible

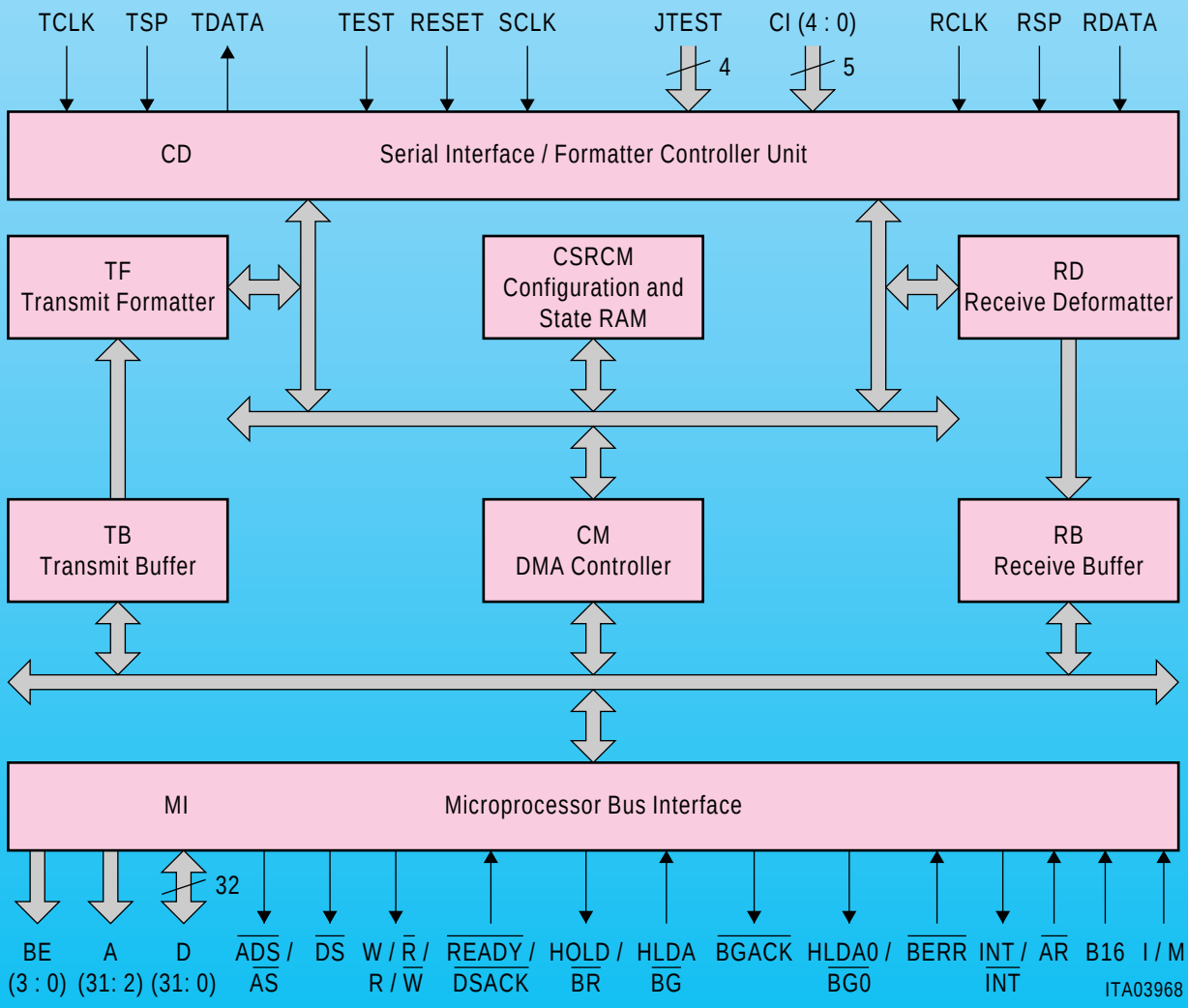
Type	Package
PEB 20320-H	P-MQFP-160-1 (SMD)
PEF 20320-H	P-MQFP-160-1 (SMD)

Bit Processor Functions (adjustable for each channel)

- Transparent mode or HDLC protocol selectable
- Automatic flag detection and transmission
- Shared opening and closing flags
- Zero-bit insertion and deletion
- Flag stuffing and flag adjustment for rate adaption
- Detection of interframe-time-fill change
- Channel inversion
- CRC generation and checking (16 or 32 bits)
- Transparent CRC option
- Error detection (abort, long frame, short frame, data under and overflow) as well as ABORT/IDLE generation and transmission
- V.110, X.30 80-bit framing, network data rate up to 38.4 kbit/s

Processor Interface

- On-chip 64 channel DMA controller with buffer chaining capability
- Compatible with Motorola 68020 processor family and Intel 32-bit processor (80386)
- 32-bit data and 32-bit address buses (4-GByte RAM addressable)
- Interrupt-circular buffer with variable size
- Maskable interrupts for each channel
- Burst cycles of up to 16 long words in the generic case are possible
- General on-chip receive and transmit data buffer; the buffer size is 256 bytes each
- Loop mode, complete loop as well as single channel loop
- JTAG-boundary scan test



Block Diagram

General Description

The SAB 82258A is an advanced general-purpose four-channel DMA controller tailored for efficient high speed data transfer between peripheral devices and memories. It is either coupled tightly with a companion CPU (local mode) or working in stand alone applications using the remote mode. The SAB 82258A is unique among DMA controllers providing complete direct interfacing to the SAB 80286 as well as to SAB 80186/188/86/88 bus.

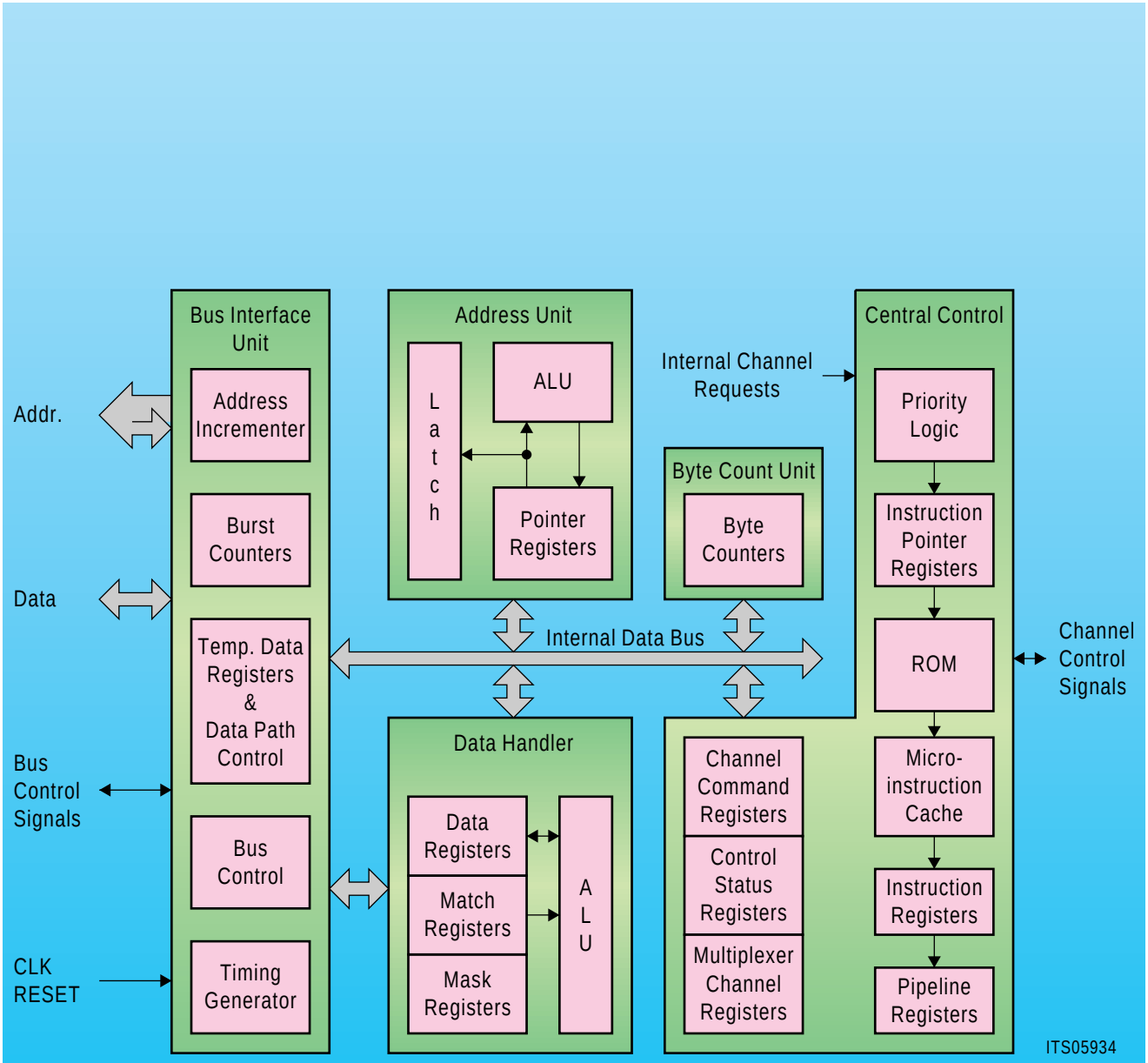
Its four superfast DMA channels transfer rate up to 10 Mbytes per second are possible. If the maximum transfer rate reaches as much as 20 Mbyte/second. In addition one of the DMA channels may be configured as multiplexer channel so that a large number of low speed peripherals can share the use of the same channel. The interrupt structure belongs to the fastest and most versatile ones available. Multiple SAB 82258A DMAs can be integrated very easily by using a simple local bus arbiter logic.

The SAB 82258A is the only DMA controller that provides source or destination-oriented data chaining (two chaining modes) as well as conditional command chaining (jumps within channel program based on several conditions).

Type	Package	Speed	Muxed Channel
SAB 82C257-1-N	P-LCC-68-1 (SMD)	10 MHz	no
SAB 82C258A-12-N	P-LCC-68-1 (SMD)	12 MHz	yes
SAB 82C258A-20-N	P-LCC-68-1 (SMD)	20 MHz	yes

Features

- 16-bit DMA controller for
  16-bit family processors
  – SAB 80286
  – SAB 80186 188
  – SAB 8086/88
- 4 independent high-speed DMA channels
- 16 Mbyte addressing range
- 16 Mbyte maximum block length
- Memory based communication with CPU
- “On-the fly” compare, translate and verify operations
- Transfer rates up to 10 Mbyte/s
- 32-bit-fly-by transfers with
  up to 20 Mbyte/s (10-MHz system)
- Single cycle and two cycle transfer
- Automatic chaining of command blocks
- Variable chaining of data blocks
- Multiplexer mode operation with up to 32 subchannels
- Local and remote (standalone) mode
- Support of 16-bit and 8-bit data buses
- Multiple programmable control of channel priorities
- Direct and fast CPU/channel communication



Block Diagram SAB 82C258A

Asynchronous Transfer Mode (ATM) ICs

Asynchronous Transfer Mode (ATM) ICs

Product Overview

Type	Short Title	Function	Page
PEB 2254	FALC™54	Frame and Line Interface Component	178
PXB 4220	IWE™	Interworking Element	179
PXB 4110	SARE™	Segmentation and Reassembly Element	180
PXB 4230	UTPT™	Unshielded Twisted Pair Transceiver	181
PXB 4240	SDHT	SDH/SONET Transceiver	182
PXB 4310	ASM™	ATM-Switching Matrix	183
PXB 43201	ASP™-up	ATM-Switching Preprocessor Chip Set (up)	184
PXB 43202	ASP™-down	ATM-Switching Preprocessor Chip Set (down)	184

Asynchronous Transfer Mode (ATM) ICs

Introduction

In the last few years, Asynchronous Transfer Mode (ATM) has made big leaps towards standardization and practicability.

Acceptance in the market is high, due to the future need of highspeed networking and seamless internetworking. This new technology perfectly suits these market demands. ATM networks offer bandwidth on demand, thus being capable of matching the user's data needs from sporadic high-bandwidth bursts to isochronous constant-bandwidth. ATM technology offers high-speed networks with various bandwidths and works with any type of transmission infrastructure. The very flexible basic structure allows to build and interconnect high-speed WANs, corporate WANs/MANs, backbone LANs, or powerful links to desktop terminals.

Traditional telecommunication structures are based on Time Division Multiplexing (TDM), offering fixed-bandwidth time-slots. ATM however sends data only when required, i.e. frames are sent asynchronously. By packing the information in 53-byte cells, including a 5-byte header containing the destination address, data is guided through the network along virtual paths and channels. ATM offers bandwidth on demand with highspeed transmission ranging from kilobytes up to gigabytes per second.

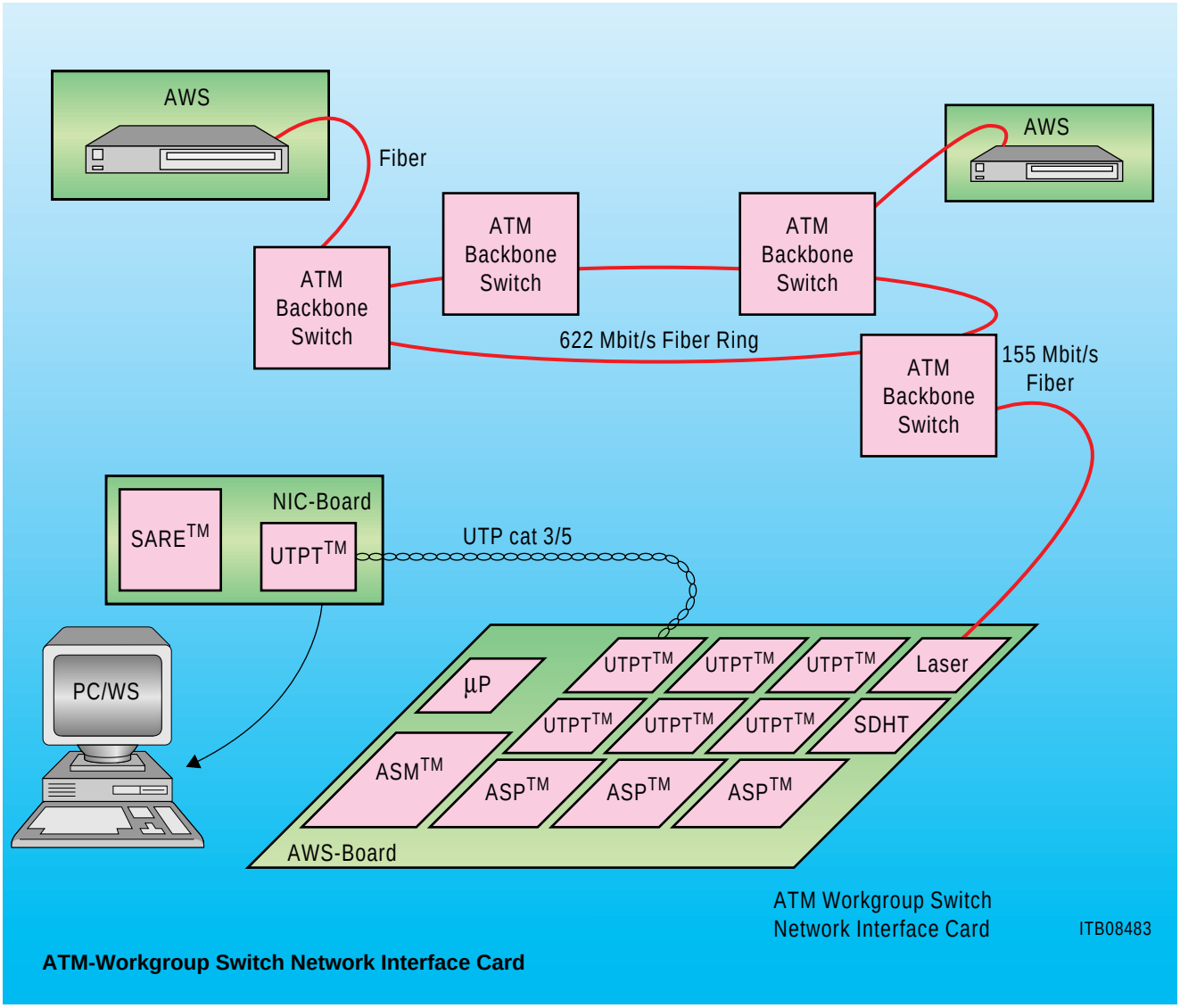
Siemens Semiconductor Group addresses the market's demand for this kind of network technology by being a driving force in the standardization activities and providing a complete ATM chipset to the market. ATM-system designers are supported by a family of Siemens ATM devices to build all kind of ATM applications. This ranges from dedicated ICs for Network or Line Interface Cards to powerful ATM switches and transmission devices.

Asynchronous Transfer Mode (ATM) ICs

Building Seamless ATM Networks

ATM technology is capable of providing powerful networks for various needs. Such an application could be a large campus network, just as shown in the figure below. In this example, several backbone switches, located at different places, are linked together. However, ATM allows this network to be managed centrally, since all backbone switches are configured to logically constitute one single switch. Workgroups are connected to the backbone via ATM workgroup switches.

The functionality of the Siemens ATM chipset, such as the cross connect feature of the ATM-Switching Matrix PXB 4310, allows members of the same workgroups to communicate effectively with each other without occupying the backbone. Only two devices of the Siemens ATM chipset are required to develop ATM-Network Interface Cards for PCs and WS, providing seamless access to the network.



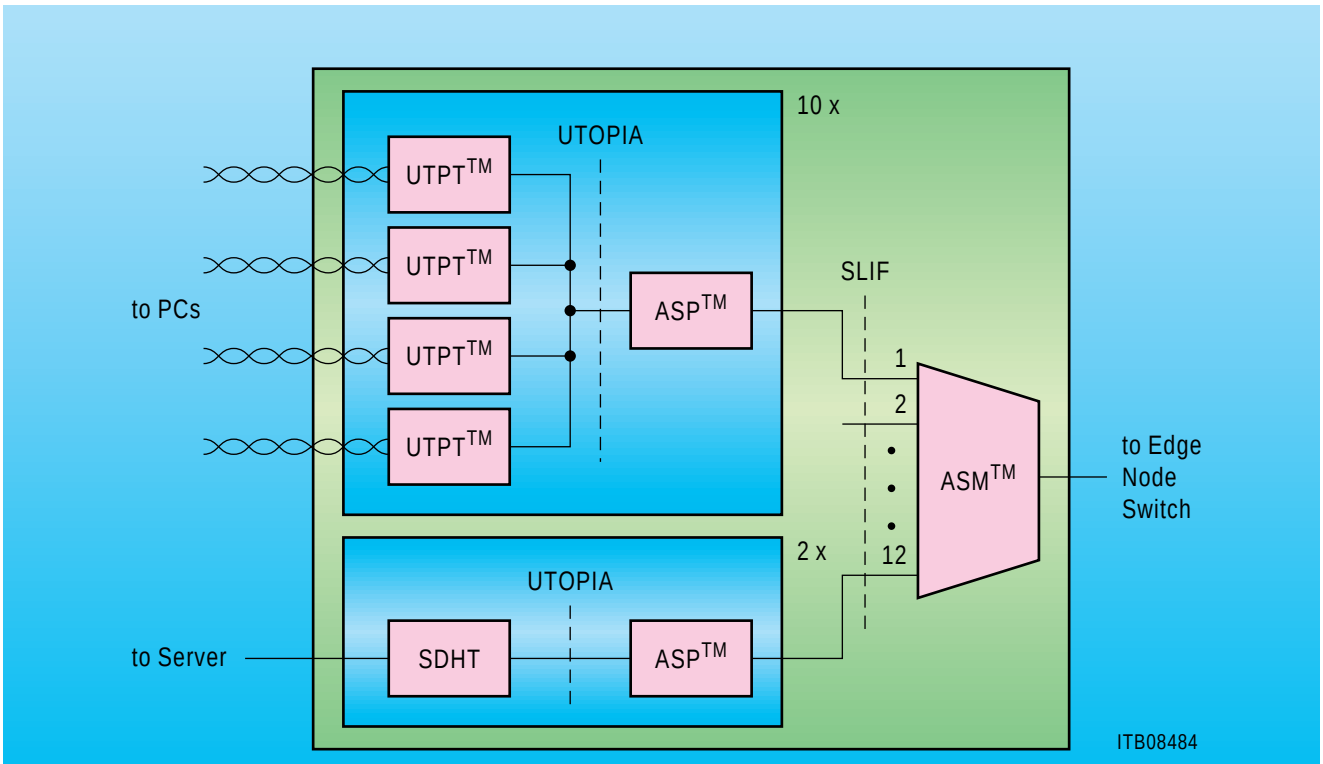
ATM-Workgroup Switch Network Interface Card

ATM-Application Examples

ATM-Workgroup Switch

Instead of using a hub to connect a small number of computers (workgroup), an ATM-work group switch can be applied. Data transmission to the computers is handled by transceiver devices, such as the PXB 4230 for unshielded twisted pair lines, or PXB 4240 for SDH/SONET lines. The actual switching function is performed by the ATM-Switching Matrix (ASM) PXB 4310.

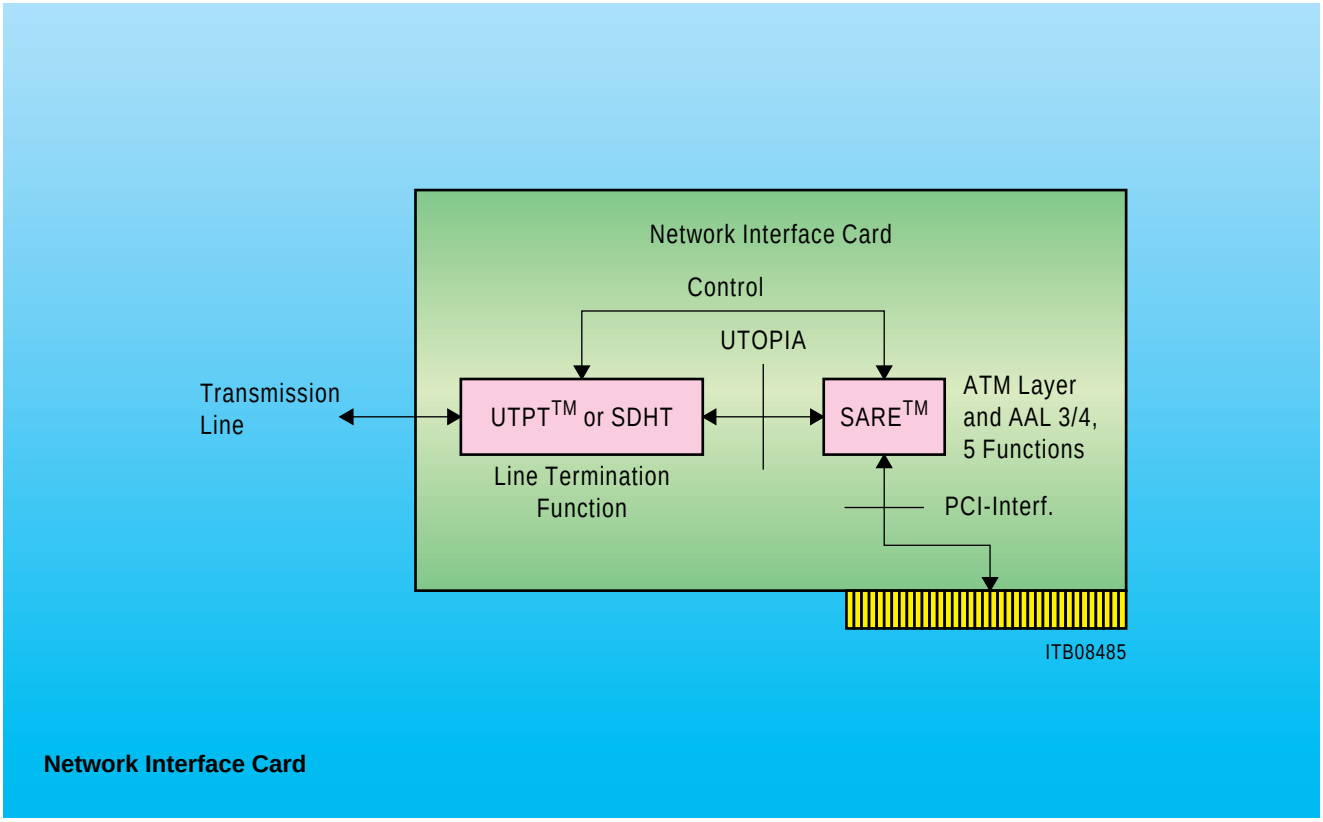
This cell switch features 32 inputs and 16 outputs with cross connect functionality. The ASM chip is designed to a special cell format, in order to reduce the pin count and power dissipation. Up-stream and down-stream conversion from the standard 53-byte ATM-cell format to this Siemens proprietary format SLIF (Switch Link Interface) is performed by the ASP chipset PXB 43201 and PXB 43202.



ATM Workgroup Switch

Network Interface Card (NIC)

A Network Interface Card can be designed with a Siemens ATM two-chip solution. It consists of the PXB 4110, which converts data (or video) frames to ATM cells, and a transceiver device. For twisted pair lines, the PXB 4230 (Unshielded Twisted Pair Transceiver) is used, whereas for optical transmission the PXB 4240 (SDH/SONET Transceiver) is required.

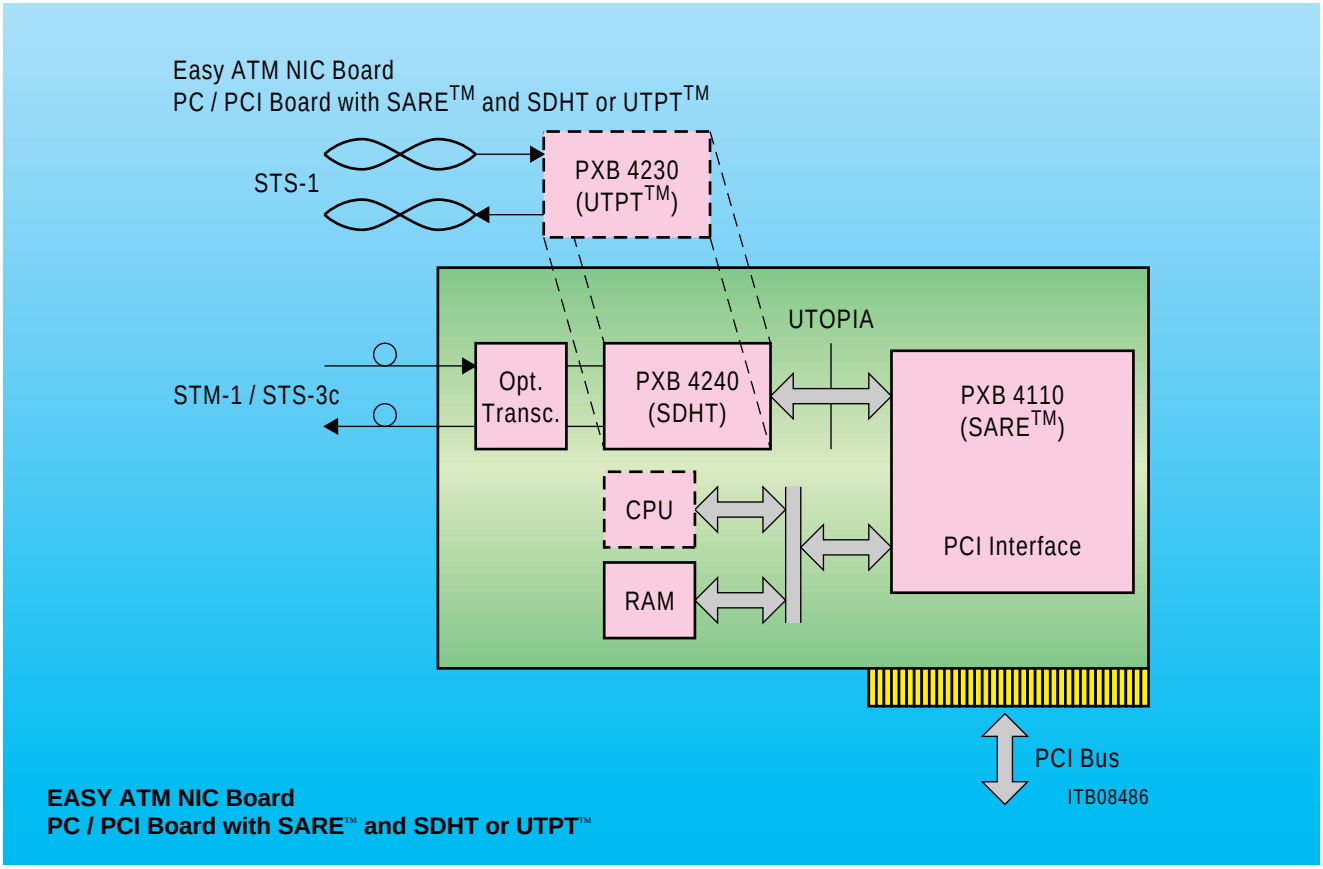


Network Interface Card

Evaluation/Demonstration Tools

The EASY ATM Demonstration, Evaluation & Development System provides designers of ATM systems with a H/W-and S/W tool kit. The Network Interface Card Evaluation System allows the designer to evaluate and test the following members of the Siemens ATM IC family: The Segmentation and Reassembly Element PXB 4110, the Unshielded Twisted Pair Transceiver PXB 4230 and the SDH Transceiver PXB 4240.

The demonstration system shows the functionality and performance of the Siemens ATM chipset by demonstrating high speed and/or time critical data transfer in multimedia or videoconferencing applications.



EASY ATM NIC Board
PC / PCI Board with SARE™ and SDHT or UTPT™

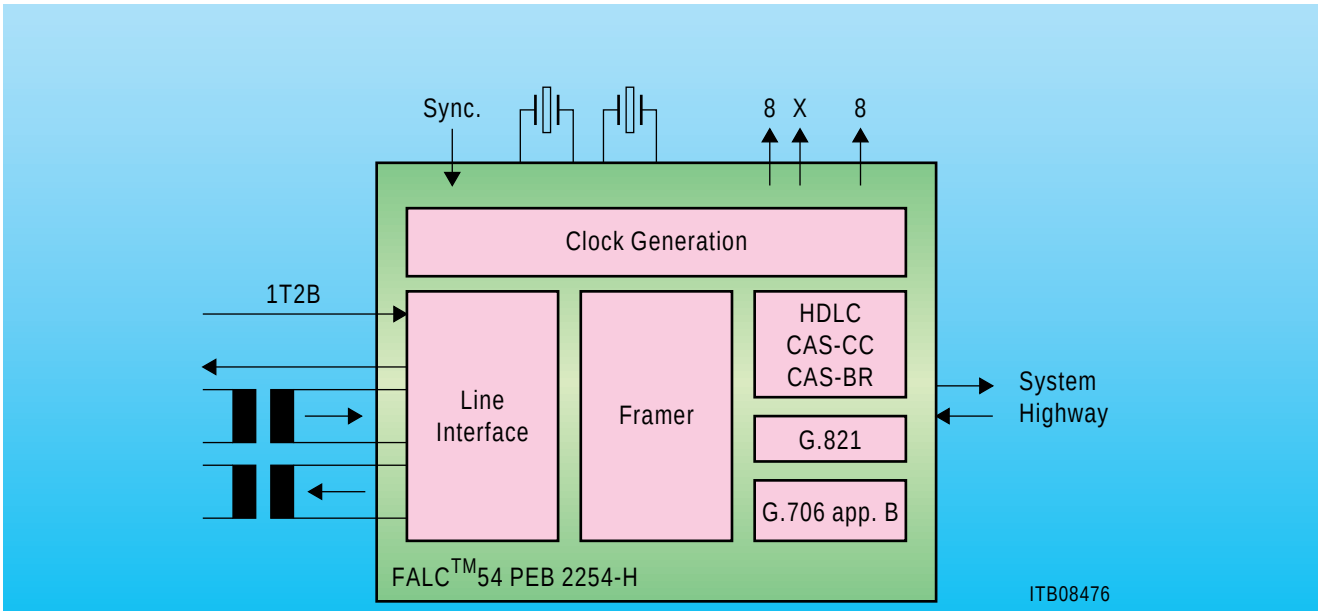
General Description

The Frame and Line Interface Component PEB 2254 (FALC54) is a high sophisticated single-chip solution for primary rate PCM carriers., It may be programmed to operate in either 1.544 Mbit/s (T1) or 2.048 Mbit/s (CEPT) carrier systems. The FALC54 provides the complete functionality of a line interface, a framer, clock generation (2 VCOs) and signaling unit on one chip with greatly increased functionalities. The FALC functions include selectable multiframe, error checking, multiple line codes, alarm reporting, maintenance and performance monitoring. All signaling types are controlled by either the integrated CAS-signaling controller or the integrated HDLC controller. Furthermore, the FALC54 allows flexible access to facility data link and service channels. Controlling and monitoring of the devices is performed via a Siemens/Intel/Motorola compatible 8/16-bit data bus.

Type	Package
PEB 2254-H	P-MQFP-80-1 (SMD)

Features

- Covers both standards E1 and T1
- On-Chip Line Interface including Data & Clock Recovery
- On-Chip CAS-CC/CAS-BR Signaling Controller
- On-Chip HDLC Controller (LAPD, F/DL, Sa-bit data)
- On-Chip System Clock Generation Unit
- Meets CCITT, ETSI and AT&T Requirements for use in systems that are compliant with:
  AT&T CB119, TR-NWT-499, ANSI T1.406, CCITT G.703, G.704, G.706, G.732, G.735-9, G.775, G.823-4, I.431, ETS 300233, V5.1 Interface, V5.2 Interface
- 8-/16-bit microprocessor interface, Siemens/Intel/Motorola compatible
- Performance Monitoring support (16-bit error counters, 1 second timer)
- JTAG-boundary scan interface
- P-MQFP-80 package



Block Diagram

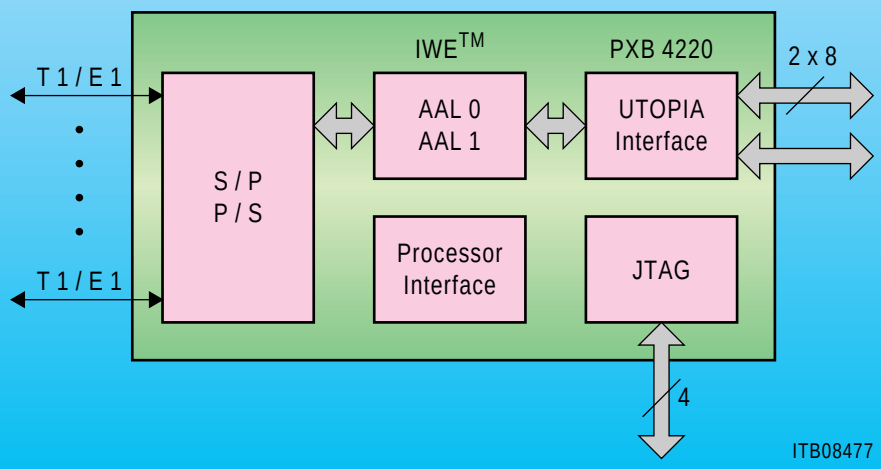
General Description

The Interworking Element functions as a gateway between Asynchronous Transfer Mode networks and time-slot based networks. The device supports both the mapping and demapping of ATM cells into/from PDH frame (T1/E1) according to G.804 and the packetizing and depacketizing of n x 64-bit time-slots into/from ATM cells according to AAL1 or AAL0. Target end products are Network and Line Interface Cards supporting the low bit rate UNI according I.432. The IWE can be directly connected to the Siemens ASP chipset via its UTOPIA level 1 interface at the ATM layer. At the physical layer several devices of the Siemens Frame and Line Interface Component PEB 2254 (E1/T1 framer) can be connected to the IWE's serial interface.

Type	Package
PXB 4220	P-MQFP-256-1 (SMD)

Features

- Single chip full duplex ATM packetizer / depacketizer for several T1/E1 highways
- All T1/E1 channels are independently configurable
- Structured and unstructured mode
- ATM-cell mapping according to G.804
- AAL1 and optional AAL0 functionality
- VPI / VCI assignment
- Support for partially filled cells
- UTOPIA level 1 interface
- 16-bit microprocessor interface
- Built-in data path loops fortest
- JTAG-boundary scan test support
- 0.5 µm 3.3-V CMOS technology
- P-MQFP-256 package



Block Diagram

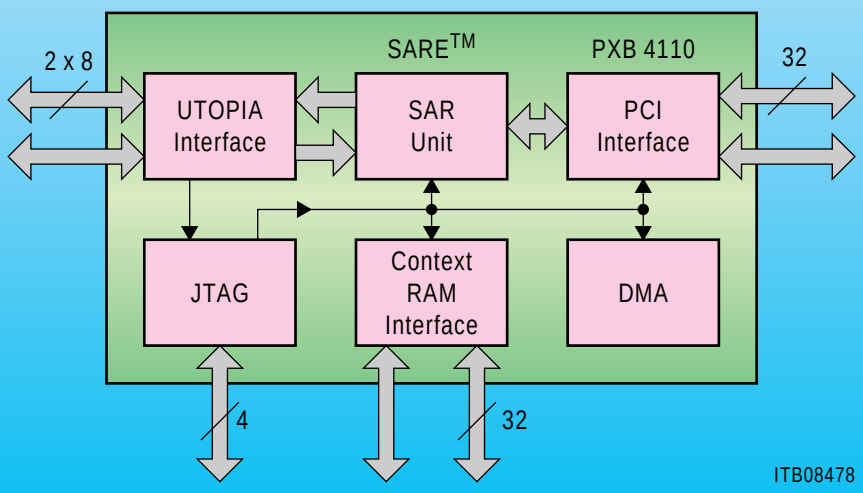
General Description

The SARE is specifically developed to build up ATM applications such as Network Interface Cards and ATM switches/hubs. This Segmentation And Reasssembly Element converts data (or video) frames to ATM cells. The flexible architecture enables it not only to handle the ATM-adaption layers AAL3/4 or AAL5, but also cell FIFO mode to support CBR. The interface for the ATM-physical layer is implemented as industry standard UTOPIA level 1. The device operates this UTOPIA interface in either slave mode, as required by switch/hub applications, or in master mode to be used in NIC (Network Interface Card) products. On the AAL side SARE features a PCI-bus interface. A 0.5-µ technology with 3.3-V supply ensures a highly integrated and cost effective system design. The SARE enables the implementation of glueless, truly cost optimized solutions for AAL-terminating equipment in ATM networks.

Type	Package
PXB 4110	P-MQFP-208-1 (SMD)

Features

- AAL 3/4 and 5 segmentation/reassembly
- Transparent mode to support constant bit rate
- On-chip support of 32 virtual connections
- Built-in FIFO (2+10 cell receive and 4 cell transmit)
- Full duplex transfer rate 155.52 Mbit/s
- VC level OAM-cell detection and CRC-10 calculation
- Cell rate shaping in transmit direction with up to 8 (dual) leaky buckets
- Bus master DMA with linked list structure and programmable buffer length
- Integrated MMU with packet scatter/gather capability
- Built-in data path loops for self-test purpose
- JTAG-(IEEE 1149.1) boundary scan
- 0.5 µ 3.3-V CMOS technology
- Optional ext. RAM supports up to 64 K virtual connections
- 32-bit PCI-bus interface
- UTOPIA level 1 interface
- P-MQFP-208 package



Block Diagram

General Description

The UTPT is a full duplex ATM transceiver for two pairs of twisted pair lines, one for each direction.

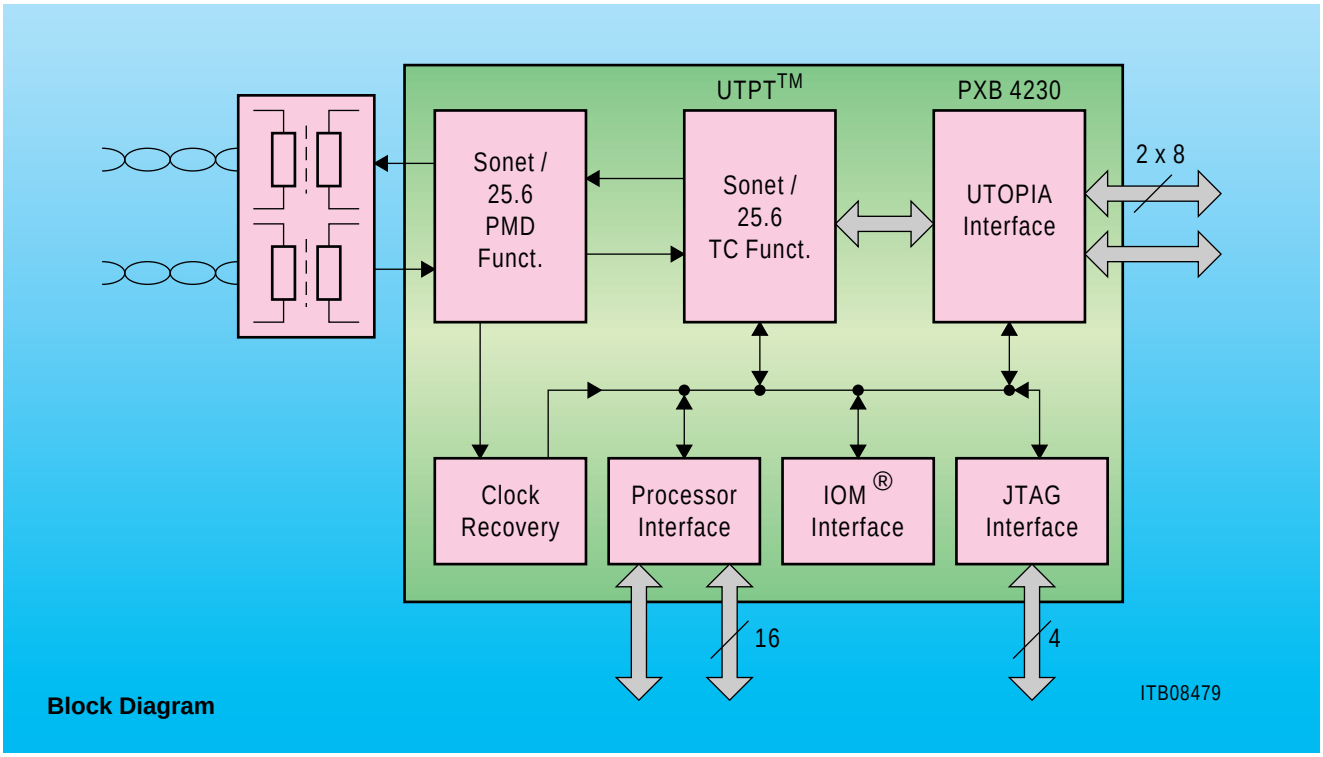
It supports both the ATT and IBM mode. In AT&T mode provides automatic bit rate adaption depending on the quality of the transmission line. The UTPT communicates with other devices on the ATM side via the industry standard universal multiport UTOPIA interface being compatible with UTOPIA level 1 and level 2.

As additional feature, the device is able to transmit 2B+1D ISDN channels when operating in AT&T mode. It also provides an ISDN IOM-2 inter-device interface and as such can be directly connected to Siemens ISDN chips. The UTPT is perfectly suited to be integrated into Network and Line Interface Cards.

Type	Package
PXB 4230	P-MQFP-160-1 (SMD)

Features

- Single chip full duplex ATM transceiver for unshielded twisted pair cat 3/5 cables
- Programmable to AT&T and IBM mode
- AT&T mode: STS-1 framing, CAP-n coding 51.84-Mbit/s, 25.92-Mbit/s and 12.96-Mbit/s automatic rate adaption according to cable and B.E.R.
- IBM mode: 4b/5b coding, NRZI, 25.6 Mbit/s
- Serial, differential in/outputs with direct connection to line transformers
- Built-in clock recovery
- ATM-layer functions: HEC evaluation, payload descrambling, cell delineation and cell rate decoupling according to ITU-T I.423
- Universal multiport UTOPIA interface compatible to level 1 and level 2
- Complete overhead handling including bit error measurement
- 16-bit microprocessor interface
- Built-in data path loops for test
- Support of JTAG-boundary scan test
- 0.5 µm 3.3-V CMOS technology
- P-MQFP-160 package



Block Diagram

General Description

The SDHT is a complete Synchronous Optical Network Synchronous Digital Hierarchy framer for 155-Mbit/s ATM implementations. It includes Transmission Convergence (TC) Sublayer processing for ATM payloads and performs the framing of data for transmission and receipt from an SHD or SONET-based Physical Layer medium.

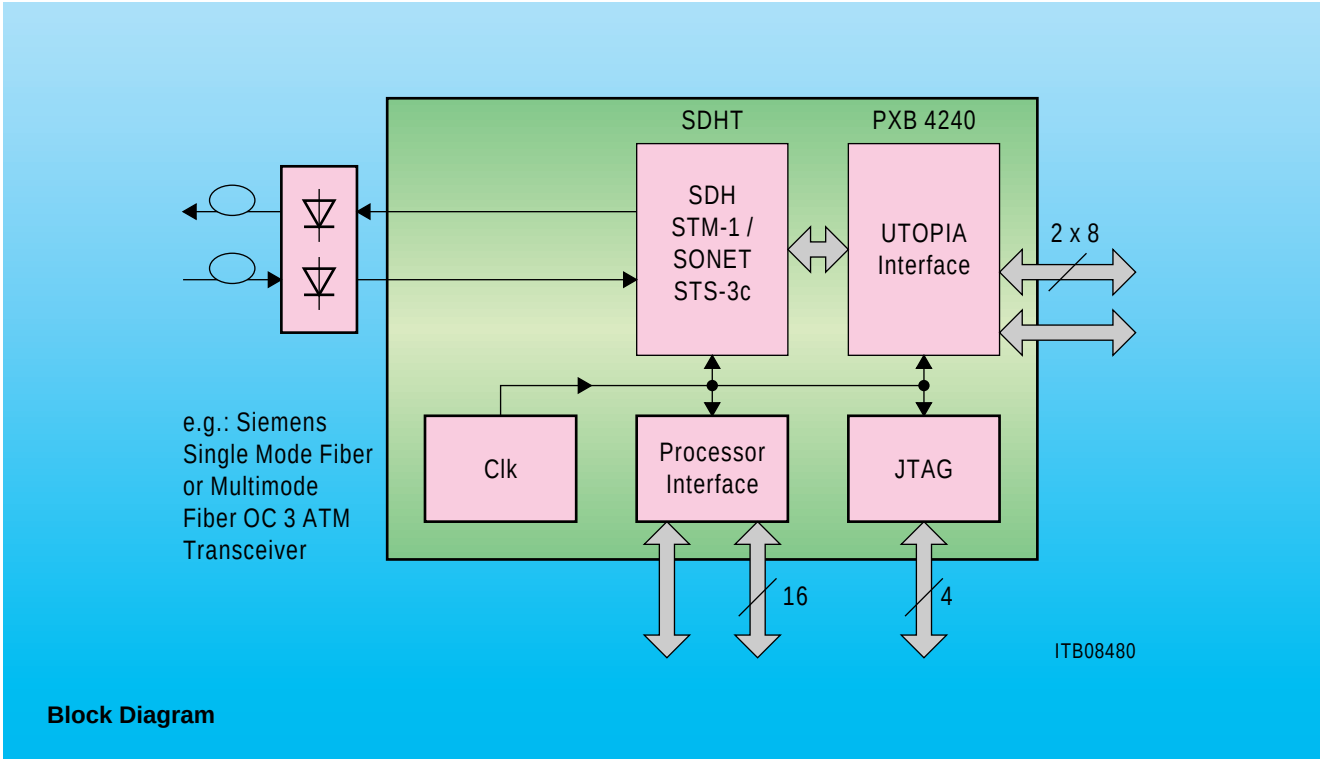
The flexible architecture allows the chip to operate in two different modes. In ATM mode for use in transmission path equipment, and in VC-4 mode to be used in multiplexer section transmission equipment.

The SDHT-chip interfaces with the ATM layer via a standard UTOPIA interface. Communication with the Physical Medium Sublayer is handled via its LVDS-level interface. To control the SDHT, a µP can be directly connected to the 16-bit microprocessor I/F.

Type	Package
PXB 4240	P-MQFP-160-2 (SMD)

Features

- Single chip full duplex ATM transceiver for STS-3c/STM-1 optical transmission lines
- Transfer rate 155.52 Mbit/s
- Serial, differential in/outputs with LVDS levels according to IEEE 1596.3
- Output of serial, differential data stream with 155.52 Mbit/s
- ATM-layer functions: HEC evaluation, payload descrambling, cell delineation and cell rate decoupling according to ITU-T I.423
- UTOPIA interface level 1
- Complete overhead handling (incl. alarms, error measurement, DCC, orderwire)
- Error counting with built-in 1 second timer
- 16-bit microprocessor interface
- Automatic laser shutdown
- Built-in data path loops for test
- Support of JTAG-boundary scan test
- 0.5 µm 3.3-V CMOS technology
- P-MQFP-160 package, pin compatible with UTPT



Block Diagram

Advanced Information

General Description

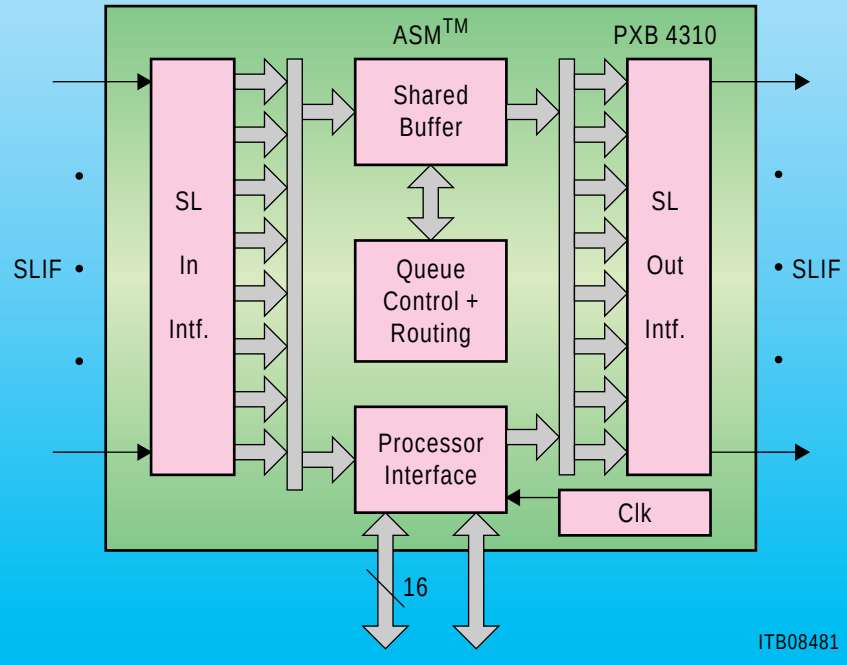
The ATM-Switching Matrix is a cell switch with a maximum total throughput of 2.5 Gbit/s. The switch has a maximum transport capacity of one STM-1 per output. Furthermore the ASM has the capability of bundling lines to form ports up to 2.5 Gbit/s.

The ASM supports both self-routing and multicast. The device can be used as either standalone or in a networked configuration to build switching networks of arbitrary size. In order to achieve a lower pin count and lower power dissipation, the inputs and outputs are realized as serial, differential transmission lines. This Siemens proprietary interface is defined as SLIF (Switch Link Interface) and its electrical characteristics are according to the LVDS standard. Internally the ASM works with 64-byte ATM cells, each cell containing the 53-byte ATM cell extended by routing and housekeeping information. Conversion from 53-byte cell format to SLIF format is done by the Siemens ASP (ATM - Switching Preprocessor) chipset PXB 43201/2.

Type	Package
PXB 4310	P-BGA-352

Features

- Self-routing switching matrix with multicast capability
- High performance: 10E-11 cell loss probability (at 95 % Bernoulli type traffic)
- Central buffer architecture provides minimum cell delay variation at high data throughput with up to 2.5 Gbit/s
- Routing header provides 48-bit routing address
- Scalable architecture from 16 x 16 to 256 x 256
- Configuration as multiplexer/concentrator
- I/O aggregation of lines to form 622-Mbit/s and 2.5-Gbit/s ports
- Switch Link Interface interconnects (208 Mbit/s serial, differential data link lines)
- Switch Link Interface uses LVDS levels for low crosstalk, less interference and low power consumption
- Individual phase adaption per input; no separate clock required
- 0.5 µm 3.3-V CMOS technology
- P-BGA-352 package



Block Diagram ITB08481

Advanced Information

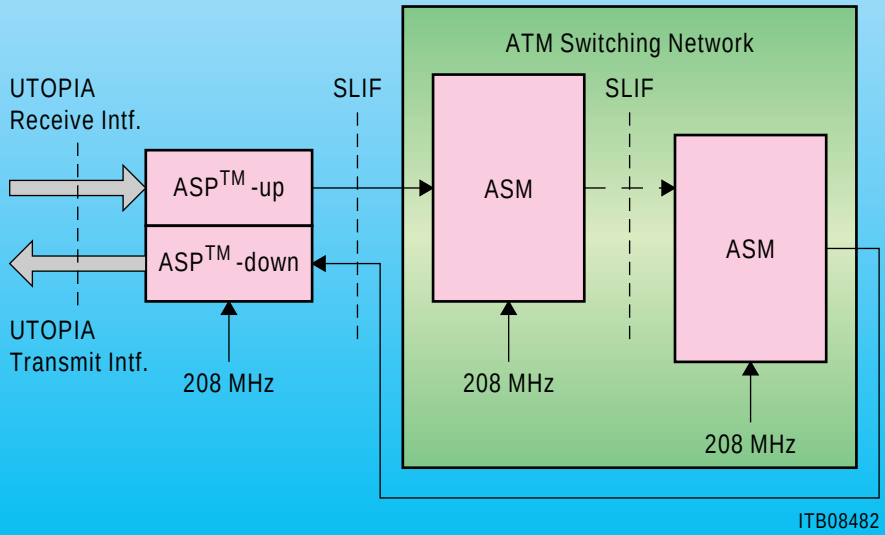
General Description

The ATM-Switching Preprocessor (ASP) chipset PXB 43201 and PXB 43202 is used to adapt the 53-byte standard ATM cell format to the 64-byte Siemens proprietary format. This cell format, also known as Switch Link Interface (SLIF), is used by the Siemens ATM-Switching Matrix to achieve a lower pin count and reduced power dissipation. At the physical layer side the ASP supports via its UTOPIA interface up to 4 physical layer devices with a total throughput of up to 150 Mbit/s. For example the following number of Siemens devices can be connected with the ASP: Up to 4 Interworking Elements (IWE) or Unshielded Twisted Pair Transceivers (UTPT) or 1 SDH Transceiver (SDHT). The ASP devices are designed to perform header translation and OAM functions according to ITU-T I.610 and Bellcore 1248.

Type	Package
PXB 43201	P-BGA-342
PXB 43202	P-BGA-342

Features

- Interfaces directly to ATM-switching networks built with ASM chips
- Header translation
- Throughput 150 Mbit/s
- OAM functions according to ITU-T I.610 and bellcore 1248:
  - Alarms: generation of AIS/RDI cells for all connections (F4 and F5)
  - Continuity check: automatic for all connections
  - Loopback: automatic loop of LB cells
  - Performance Monitoring: complete HW support for up to 64 connections
- Double switch plane support for redundant fail safe switching systems
- System Control Information Flow via SLIF Datalink supported
- Use external SDRAMs for storage of connection related data
- 16-bit general purpose microprocessor interface
- JTAG-boundary scan
- P-BGA-342 ball grid array package



Block Diagram

Development Systems for Information Technology

Product Overview

Introduction

Todays highly complex system development projects make it necessary to have a powerful development environment available additionally to the components themselves.

Some of the necessary tools are supplied by the chip manufacturer himself.

The tools consist of either component evaluation boards or sometimes even almost ready to copy system designs. Also software chip drivers are often supplied to ease the integration of components into a customer's software design. In some cases software skeleton solutions or even ready to use software is supplied to speed up the whole system design.

Besides the tools supplied by the silicon vendor a lot of third party tools are available on the market which can efficiently be used. The support tools supplied by Siemens are typically designed to be used in conjunction with a PC and third party software tools giving a very powerful environment.

The application oriented guide describes the different support tools supplied by Siemens in an application oriented way and it gives hints to set up a development environment by adding third party equipment whenever meaningful.

This is an application oriented guide meant to provide a fast way into the typical development environments customers need. Such a general approach does of course not necessarily describe the customers specific environment exactly. However it describes the most common ones.

1 Tools for Analog Line Card Design

1.1 PCM Codec Filter for Analog Line Cards in Digital Communication Systems

The Siemens PCM Codec Filter are fully integrated PCM CODEC and Filter in advanced low power CMOS technology for applications in digital communication systems.

Based on a digital signal processing technique programmable digital filters adapt the transmission behaviour especially for AC impedance matching transhybrid balancing frequency response and gain.

For analog line card designs in digital communication systems a family of Siemens Codec-Filter ICs can be offered:

Codec	Channel per Chip	Part Number	Best Application
SICOFI®	1	PEB 2060	PBX and CO
SICOFI®-2	2	PEB 2260	PBX and CO
SICOFI®-4	4	PEB 2465	PBX
SICOFI®-4 µC	4	PEB 2466	PBX
SLICOFI®	1	PEB 3065	CO
HV-SLIC	1	PEB 4065	CO

As shown in the table above the best application for our codec filter ICs may be in a Private Branch Exchange (PBX) and/or in a Central Office (CO). The SICOFI, SICOFI-2 and SICOFI-4 Codec-Filter ICs may also be used in TRUNK applications.

The four channel codec filters PEB 2465 and PEB 2466 are the logic continuation of a well established family of Siemens Codec-Filter ICs.

The SLICOFI PEB 3065 is a single codec and filter with an optimized high voltage. SLIC interface including all low voltage SLIC functions. The DC-characteristic is fully digitally programmable. Together with the HV-SLIC circuitry PEB 4065, Siemens offers a complete system solution for central office applications.

Based on an advanced digital filter concept the PEB 2465 as well as the PEB 3065 provide excellent transmission performance and high flexibility. They fulfill all specifications to relevant CCITT, EIA and LSSGR recommendations. The new filter concept (second generation) leads to a maximum of independence between the different filter blocks.

1.2 Software to Calculate Digital Filter Coefficients

Different software tools are available to get optimized sets of filter coefficients for the Siemens Codec-Filter lCs easily and quickly.

Software	Codec	Part Number
SICOFI®	SICOFI® Coefficients Program for PEB 2060 and PEB 2260	STS 2060
QSICOS	Quad SICOFI® Coefficients Software for PEB 2465/PEB 2466	STS 2465
SLICOS	SLICOFI® Coefficients Software for PEB 3065	STS 3065

1.3 Hardware Support for Analog Line Cards

For development different hardware environments are offered for the analog line card design. For additional detailed information please refer also to the description of the **Tools for PCM Control and Switching System Designs**.

To build a typical development environment for an analog subscriber line card one of the following set-ups may be used:

Codec	Codec Board	Additional Hardware
SICOFI®	SICOFI® Test Board STUT 2060	none
SICOFI®-2	SICOFI® Test Board STUT 2060 SICOFI®-2 Board SIPB 5135	none 1) or 2)
SICOFI®-4	SICOFI®-4 Board STUT 2465	1) or 2)
SICOFI®-4 µC Kit	STSI 2466 (SICOFI®-4 µC Board STUT 2466 EVC50X µC Board)	none
SLICOFI®	SLICOFI® Board STUT 3065	1) or 2)

Additional Hardware

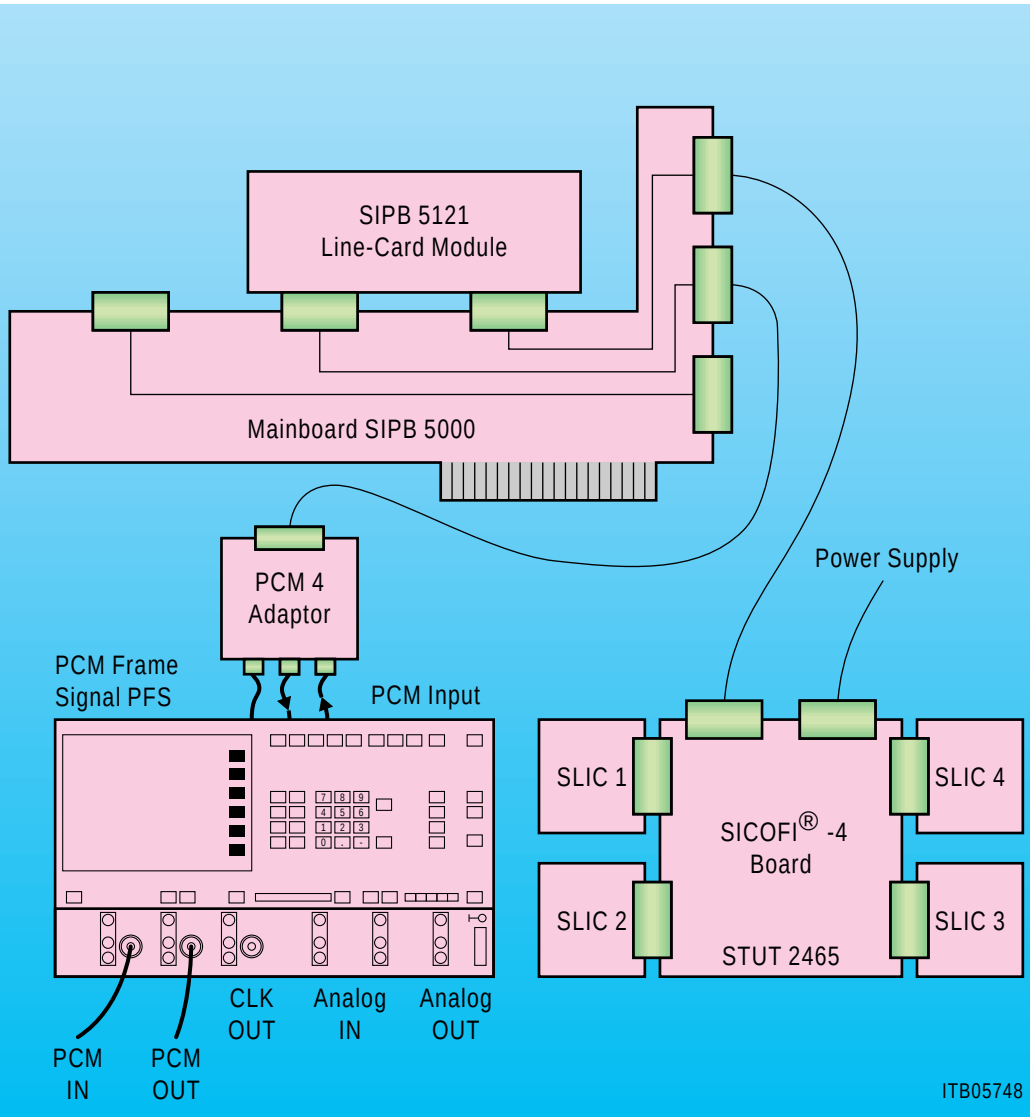
1. Board configuration:
   SIPB 5000 + SIPB 5121 + SIPB 5311
2. PERCOFI Board STUT 2000

1.3.1 Using the SIPB 5000 PC-Userboard System in Conjunction with a Line Card Module

The next figure shows a set-up that is used to measure the SICOFI and SLIC transfer characteristic using a PCM4 by Wandel & Goltermann. In this configuration the PC mainboard SIPB 5000, the Line Card module SIPB 5121, the PCM4 adaptor SIPB 5311 and the SICOFI-4 Board STUT 2465 are used.

Instead of using the SICOFI-4 Board STUT 2465 also the SICOFI-2 Board SIPB 5135 or the SLICOFI Board STUT 3065 may be connected via IOM interface to the Line Card Module SIPB 5121.

If the STUT 2466 and the SICOFI-4 µC are used together, the SIPB 5000 and SIPB 5121 are not required. Instead the microcontroller board EVC50X (Part of STSI 2466 kit) is used to program the SICOFI-4 µC.



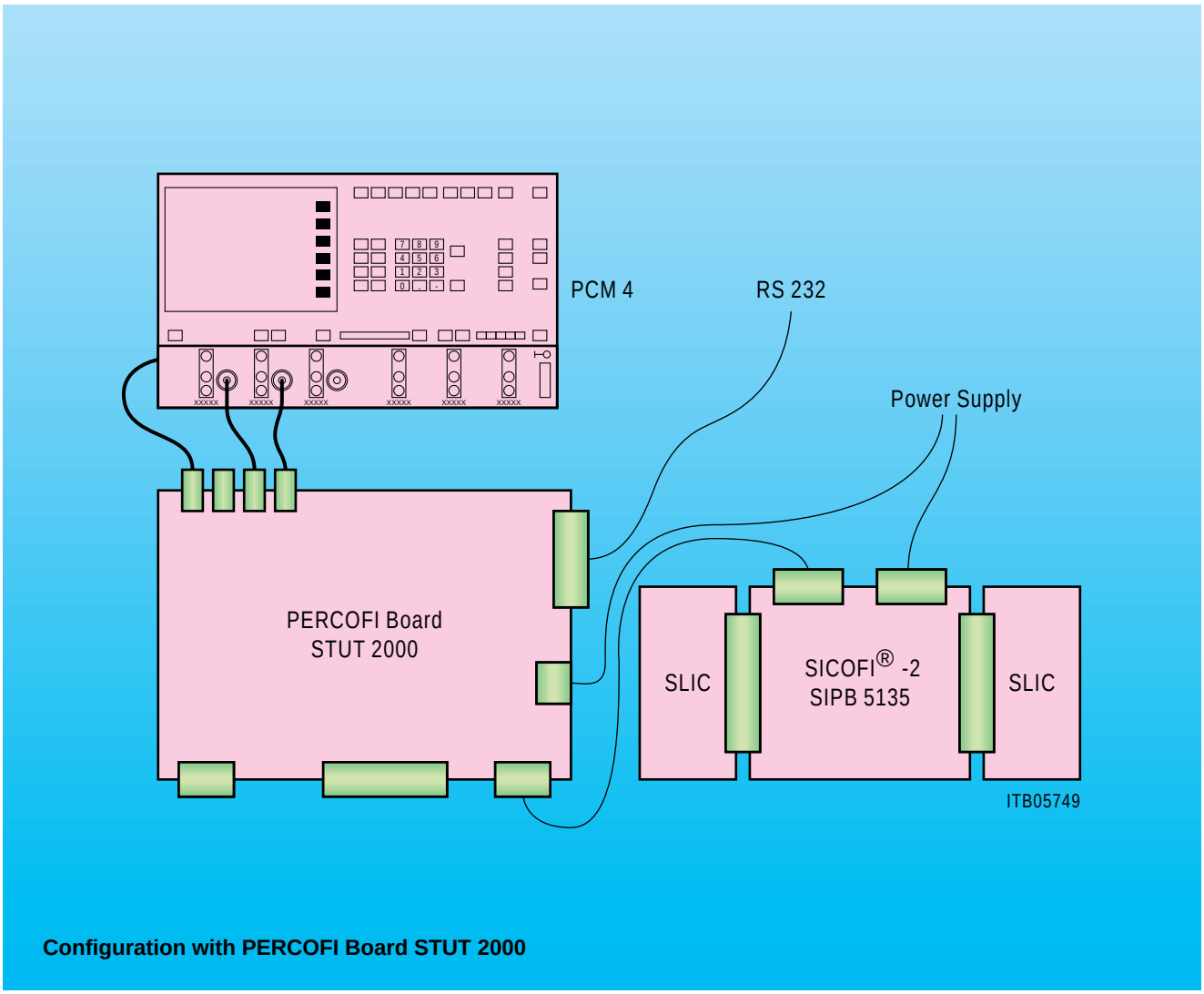
Set-Up to Measure Transfer Characteristics

1.3.2 Using the PERCOFI Board STUT 2000

The PERCOFI Board is an universally usable board to measure the SlCOFI-2 SICOFI-4 or SLICOFI. The PERCOFI Board is not only to replace the SICOFI testboard STUT 2060, but also to allow critical performance measurements.

The following configuration shows a typical line card application using the STUT 2000 PERCOFI Board and the SICOFI-2 Board SIPB 5135. The PERCOFI Board is programmed via the RS232 interface by using the same trackfiles that are used with the Mainboard SIPB 5000 and the Line Card Module SIPB 5121 to program the codec devices.

Instead of using the SICOFI-2 Board SIPB 5135 also the SICOFI-4 Board STUT 2465 or the SLICOFI Board STUT 3065 may be connected to the PERCOFI Board STUT 2000 via IOM interface.



Configuration with PERCOFI Board STUT 2000

1.3.3 Using the SICOFI® Test Board STUT 2060

The SICOFI test board STUT 2060 is a stand-alone board which offers the possibility of connecting any external customer specific SLICs with the SICOFI PEB 2060/2260 for evaluation of customer specific combinations of SLIC and SICOFI. The next figure shows a set-up that allows measurements and tests covering the transfer functions of the complete subscriber line module.

The board is programmable via an RS232 interface by a terminal or PC. The registers of the PBC or PIC and SICOFI can be accessed and therefore the SLIC can be controlled.

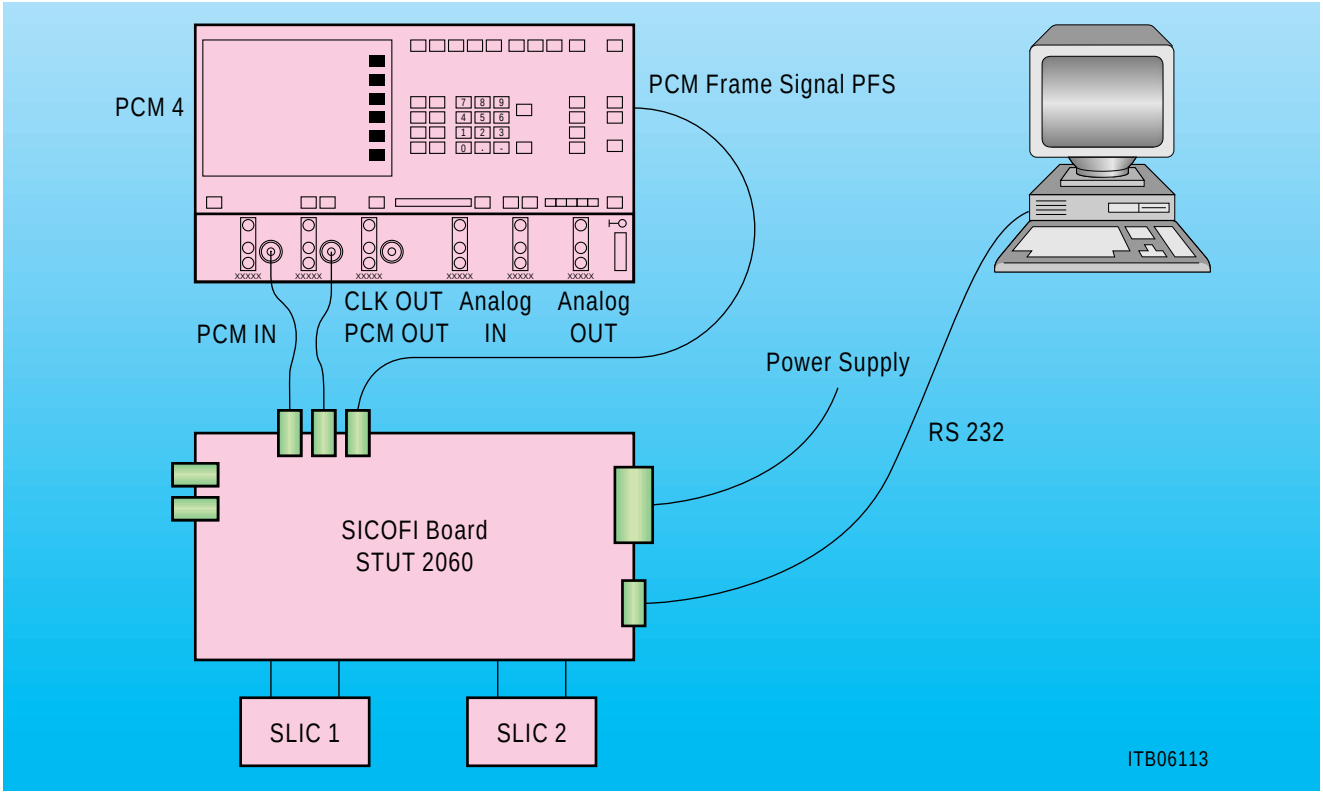
With the SICOFI testboard the SICOFI PEB 2060 and SICOFI-2 PEB 2260 codec filter devices can be tested. The PCM interface of the board can be connected directly to a PCM4 Wandel & Goltermann test equipment. This set-up allows to test the SLIC hardware and to verify the programmed coefficients, which are calculated with the SICOFI coefficients program.

Different customer specific SLICs or ready designed SLIC boards available from Siemens Semiconductor may be connected to the SICOFI test board STUT 2060 via a 64-pin connector.

1.3.4 SLIC Boards to be used with the SICOFI® Family

A collection of SLIC babyboards has been designed to be used with the SICOFI PEB 2060, SICOFI-2 PEB 2260 or SICOFI-4 PEB 2465.

Codec	Available SLIC Module	Part Number
PEB 2060/ 2260	Transformer SLIC Board	STUS 1001
PEB 2060/ 2260	STM L3000 + L3030 SLIC	STUS 3030
PEB 2060/ 2260	STM L3000 + L3090 SLIC	STUS 3090
PEB 2060/ 2260 PEB 2465	Ericsson PBL 3736 SLIC	STUS 3736
PEB 2060/ 2260 PEB 2465	Ericsson PBL 3762/64 SLIC	STUS 3762
PEB 2060/ 2260 PEB 2465	Harris SLIC HC5502	STUS 5502
PEB 2060/ 2260 PEB 2465	Harris SLIC HC5509	STUS 5509



2 Tools for ISDN Basis Rate Line Card Designs

2.1 U Transceiver Development Tool (2B1Q)

Together with the SIPB 5121 Line Card Module the IEC-Q Reference Board SIPB 2091 constitutes the layer-1 functionally needed for the evaluation of various digital line card architectures using 2B1Q technique for interfacing with the U-reference point.

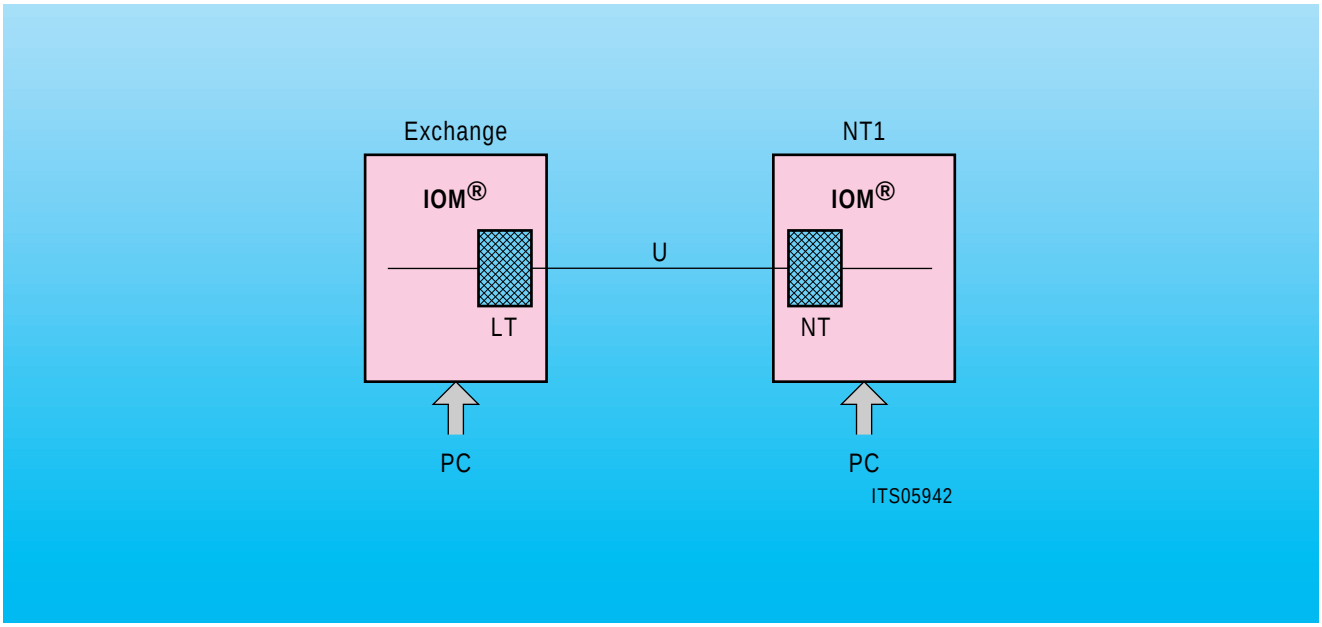
2.2 Introduction to the IEC-Q Reference Board SIPB 2091, SIPB 2092 and SIPB 2092-H

The IEC-Q Reference Board was developed to demonstrate the performance of the Siemens IEC-Q (PEB 2091) U-interface transceiver IC. The IEC-Q (ISDN Echo Cancellation Circuit) uses 2B1Q code for transmission on U. A single board can be configured by the user to suit multiple operation modes such as LT and NT modes. Test points allow for comfortable monitoring of relevant signals. This enables the developer to quickly comprehend both the IC- and U-interface-related signals.

The IEC-Q Reference Board interfaces ISDN transmission lines and terminal areas providing echo cancellation and message recovery using digital techniques. Hence the main use of the IEC-Q Reference Board is to accomplish performance measurements i.e. bit error rate (BER) measurements on the ETSI and ANSI defined loops.

The optimized layout of the Reference Board allows for performance measurements in all operation modes available with the IEC-Q. The so called hybrid was developed to reach optimum loop lengths and to cover all 15 ANSI loops as well as the 8 ETSI defined loops. The figure below shows a typical configuration with LT and NT 1 where the interconnection between the two U-transceiver devices is established with means of a dual lead copper wire (U).

The SIPB 2092 additionally supports the stand-alone (IOM-2) mode and the µP-interface mode. SIPB 2092-H is identical to SIPB 2092 except that a P-TQFP-64 package socket instead of a P-LCC-44 socket is provided. For stand-alone operation of the IEC-Q, both SIPB 2091 and SIPB 2092 are equally suited.



2.3 Bit-Error-Rate Measurement with SIPB 5000 Main Board

For bit-error-rate (BER) measurements on U the following add-on modules are required on the LT side in addition to the LT IEC-Q Reference Board:

ISDN Terminal Adaptor Module (ITAC®) SIPB 5140

LAYER-2 Module SIPB 5120-2

Bit Error Adaptor Module (BEAM) SIPB 5312

The following modules are required for BER measurement on the NT side in addition to the NT IEC-Q Reference Board:

LAYER-2 Module SIPB 5120-2

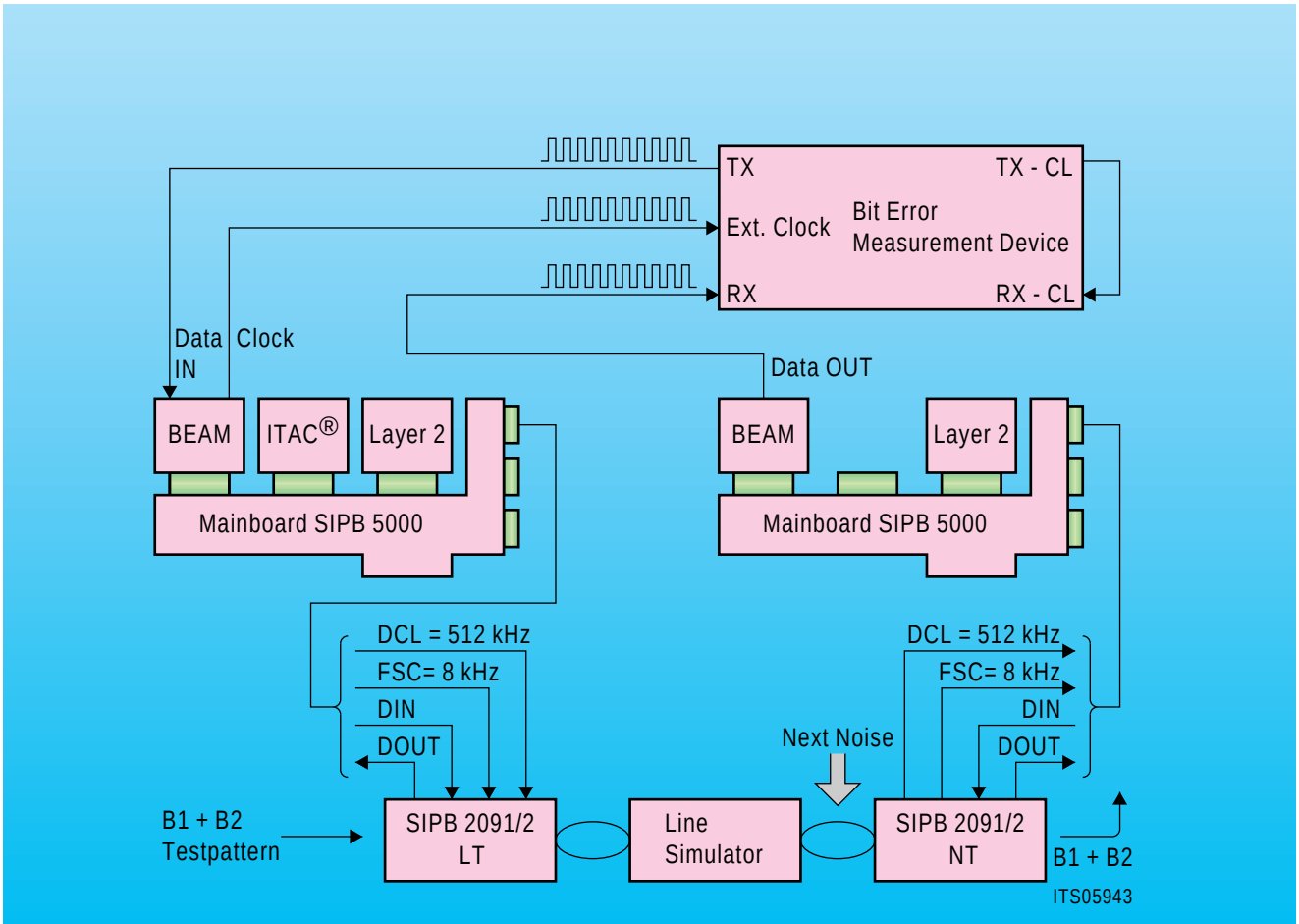
Bit-Error-Adaptor Module (BEAM) SIPB 5312

The configuration below describes the use of standard LT/NT applications for the purpose of BER measurements when supplemented with two BEAM modules. The figure shows the complete SIPB system set-up for a BER measurement in LT-NT direction.

Comments:

For the bit-error-rate measurement the LT is configured in the LT-512-kHz mode since the BEAM module only supports a 512-kHz-DCL clock rate.

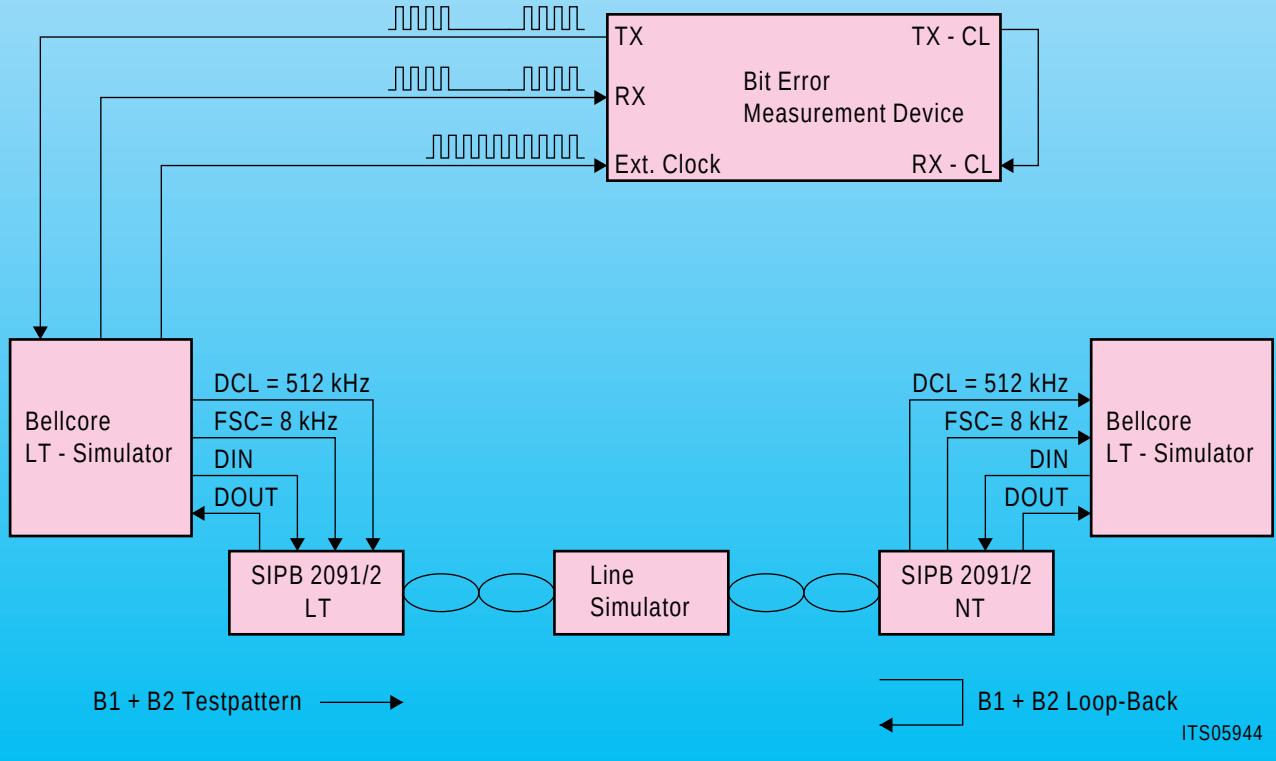
With means of the two BEAM modules the BER test equipment can be synchronized to the IOM clock rate as well as insert and extract B1/B2 channel data via IOM. BER measurement is then accomplished by comparing the inserted with the extracted data. A line simulator is used for emulating lines and loops including NEXT noise impairments in order to run performance tests according to the relevant specifications (ETSI/ANSI).



Set-Up for Bit-Error-Rate Measurements Using SIPB 5000 System

2.4 Bit-Error-Rate Measurements with Bellcore Board (BELL 2091)

In conjunction with two IEC-Q Reference Boards, the so called Bellcore Boards provide the most comfortable method to evaluate the PEB 2091 and perform BER measurements. No PC is needed for simulating 2B1Q U-transmission configuration.



Set-Up for Bit-Error-Rate Measurements Using Bellcore Board (BELL 2091)

3 Tools for PCM Control and Switching System Designs

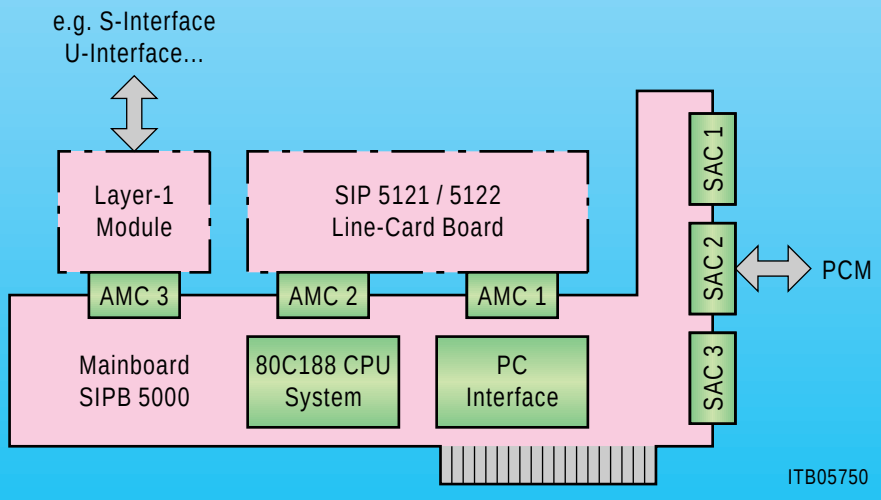
3.1 Development Environment

3.1.1 A Typical Development Environment for Subscriber Line Cards

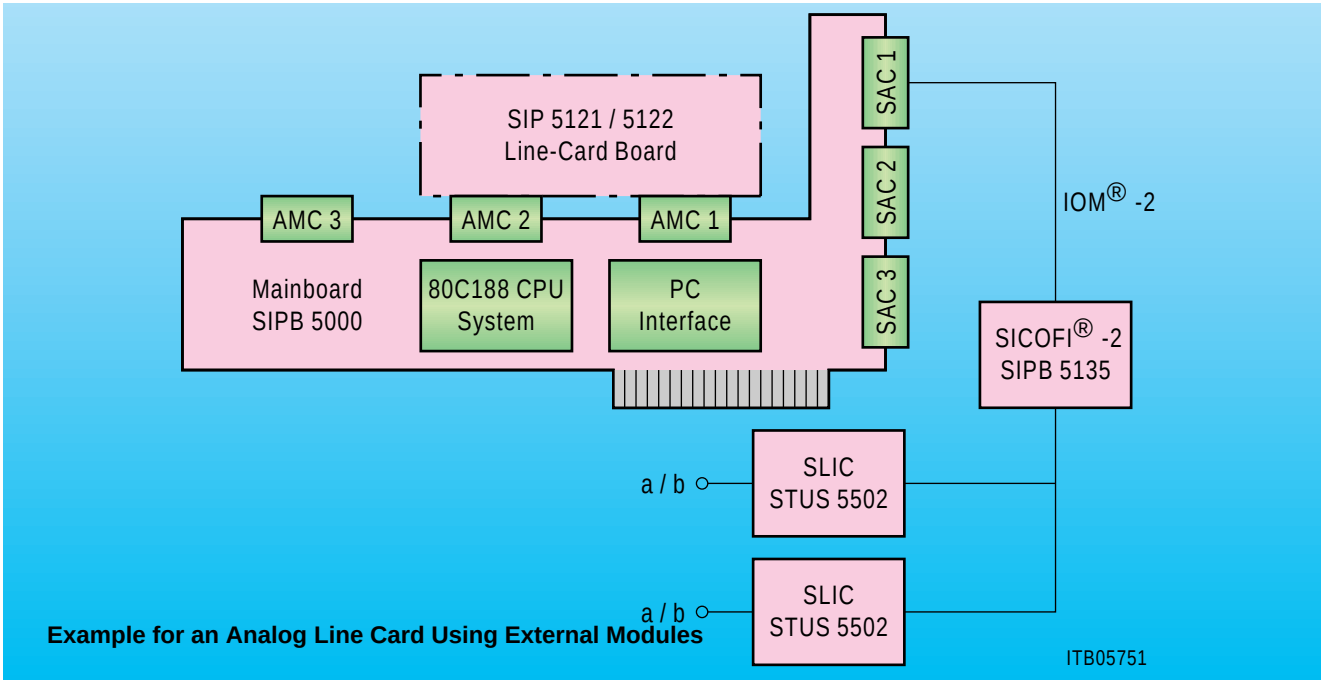
When using the SIPB 5000 ISDN PC-Userboard system in conjunction with a line card module, an engineer is capable of designing his own digital or analog line card board.

The basic module needed to build a line card is either SIPB 5121 or SIPB 5122. Depending on the requirements for layer-1 interface (for digital line cards) and/or CODEC filter (analog line cards) additional modules have to be connected. The following modules may be combined with the line card module:

Interface	Required Module	Part Number	Connection
Analog	SICOFI®-2 Module SLIC	SIPB 5135 e.g. STUS 5502	External
Analog	SICOFI®-4 Board SLIC	STUT 2465/2466 e.g. STUS 5502	External
Analog	SLICOFI® Board (SLICOFI® + HV-SLIC)	STUT 3065	External
S interface	S-Access Module (ISAC®-S)	SIPB 5100-0	SIPB 5000
S interface	SBCX Layer-1 Module	SIPB 5116	SIPB 5000
S interface	QUAT®-S Board	SIPB 5117-S	External
U_{k0}	U_{k0}-Layer-1 Module (IEC-Q)	SIPB 2091/2	SIPB 5000
U_{k0}	QUAT U_{k0} Board (AFE + DFE-Q / DFE-T)	SIPB 2490/1	External
U_{P0}	U_{P0}-Access Module (ISAC®-P)	SIPB 5104	SIPB 5000
U_{P0}	OCTAT®-P Board	SIPB 5117-P	External
U_{P0}	U_{P0} Layer1-Module (IBC)	SIPB 5113	SIPB 5000



Realization of a Digital Line Card



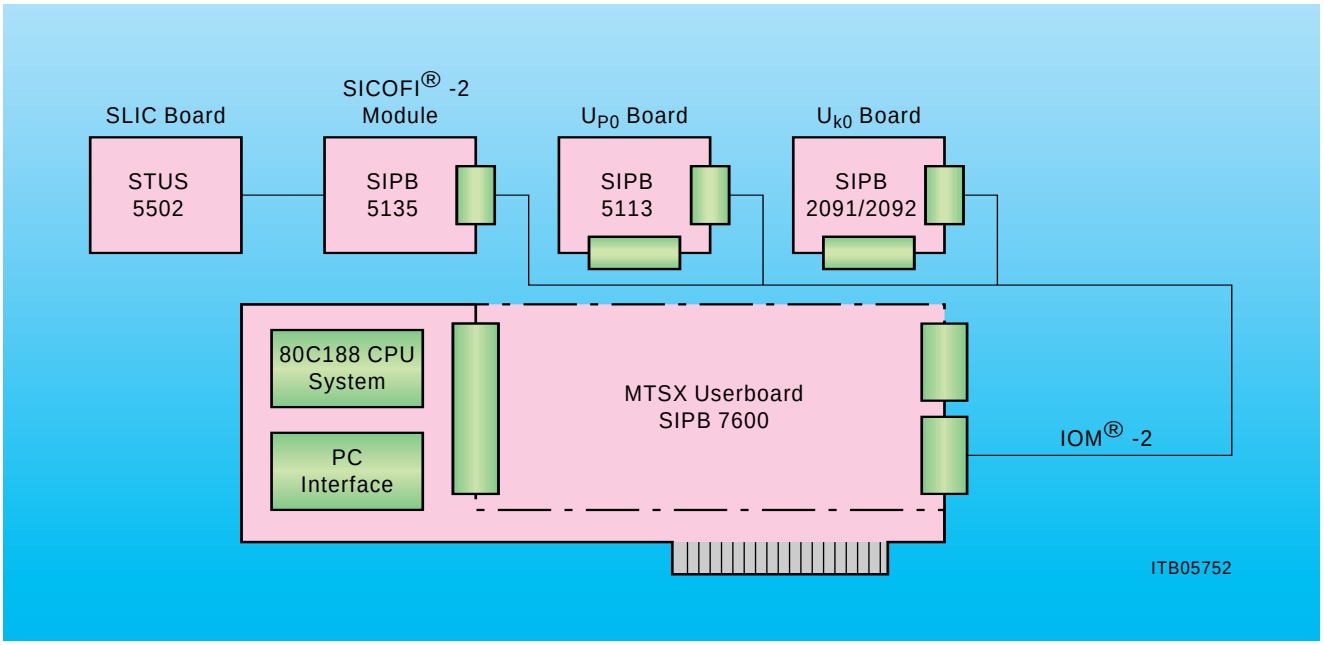
Example for an Analog Line Card Using External Modules

3.1.2 A Typical Development Environment for a Switching System

The SIPB 7600 Memory Time Switching Board is a PC/XT/AT based development tool that helps engineers to get familiar with switching and conferencing ICs.

Test patterns may be generated on board and put as an input to the switching and conferencing circuits. When working with continuous data streams additional modules (layer-1 modules) have to be connected via a 9-pin-flat cable to the IOM-2 interface.

The figure below shows an example how to connect analog as well as digital subscribers to the SIPB 7600:



3.2 The Different Steps in Development

3.2.1 Designing the Hardware

The SIPB 5000 system can be used as a platform for all development steps. In a later stage it is of course necessary to make a cost optimized design. For this a subset of the board design can be used. All the wiring diagrams are shipped with the board to speed up this process.

3.2.2 Developing the Software

In a premature stage of a development it is very useful to verify the design by running program sequences on a similar hardware platform. To manage this task Siemens offers a very comfortable menu-driven testing and debugging software. The package delivered with the userboard allows a direct access to the chip registers by symbolic names. Subsequent accesses may be written to a file and run as a trackfile.

Example trackfiles for different configurations are delivered in the package and will be a great help to the user in getting started and to speed up his software development.

4 Tools for ISDN Basic Rate Terminal Designs

4.1 A Typical Development Environment for an ISDN Phone or TA

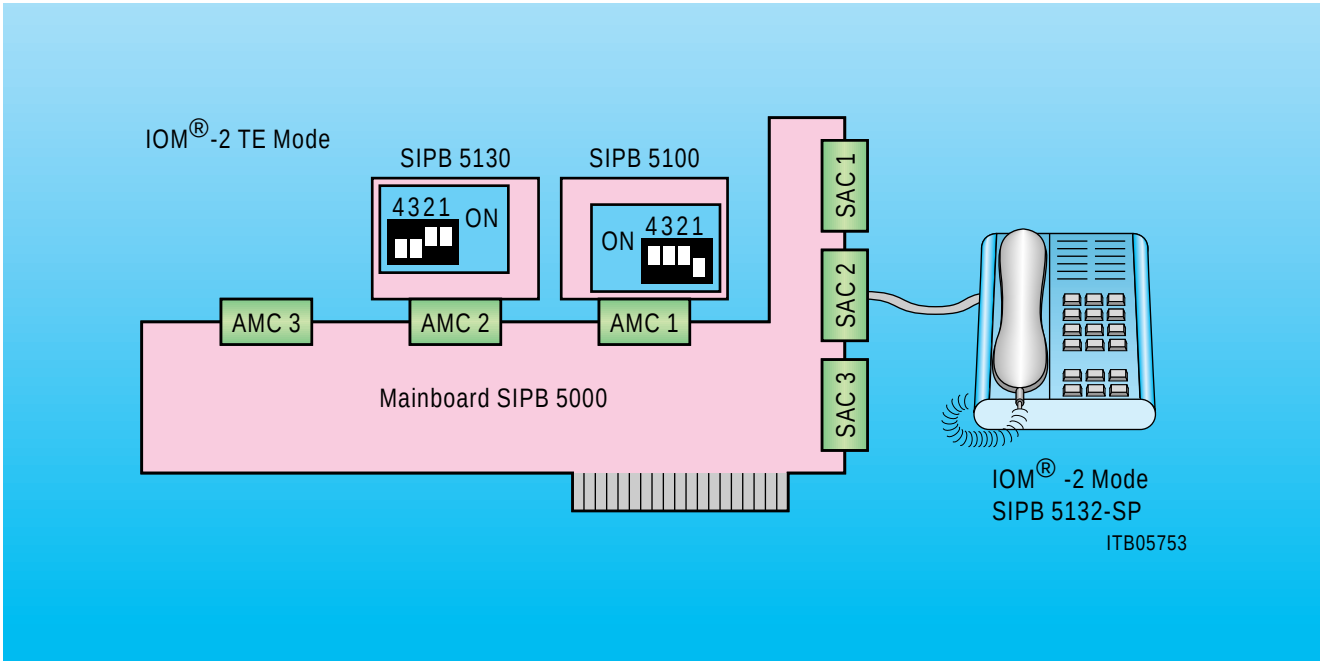
The Siemens ISDN PC Board Kit SIPB 7011A is based on a very modular tool environment. This allows to configure every existing application just by replacing some modules. The system can be configured as either a terminal itself or as a network simulator. It can be used to program and evaluate the chips but it can also be used to run real software (see IOS).

The ISDN Telephone Development Board SIPB 8051 is a more or less ready to copy environment to demonstrate the terminal system in silicon using the ARCOFI-SP (PSB 2163), the ISAC-S TE (PSB 2186) and the one-chip controller SAB 80515 with the ISDN protocol software. An ITAC (PSB 2110) for the rate adaption as well as an ISAC-P TE (PSB 2196) for the U_{PN} interface is also onboard.

To set up a development environment for serious developments it is best to use both an SIPB 7011A kit as a network terminator being able to simulate the public ISDN and secondly an SIPB 8051 system as the real development platform. Both systems should be connected and of course a PC should be connected to the SIPB 8051 to run a C-Compiler and to download and debug code.

The Keil C51 professional package (in USA Franklin C51 package) as well as the development package of the Swedish company IAR Systems (in USA Archimedes) have been used with the SIPB 8051. Their high level language debuggers can be used very efficiently with the SIPB 8051.

Both systems should be connected and an 8051 type C-Compiler and high level language debugger should be available. Additionally the IOS software should be used as a very efficient software platform if a public protocol is required. This software is a very compact software solution. It fits on a one chip controller without needing additional memory. For rapid prototyping or PTT approval an E^2PROM version of the 80C515A is also available.



4.2 The Different Steps in Development

4.2.1 Designing the Hardware

The SIPB 8051 can be used as a platform for all development steps. In a later stage it is of course necessary to do a cost optimized design. For this a subset of the SIPB 8051 design can be used. All the wiring diagrams are shipped with the board to speed this process up.

4.2.2 Developing the Protocol Software

A major task in the design work is the development of the public ISDN protocol software. To ease this work Siemens provides the IOS as an almost ready to copy protocol software kernel. IOS has been designed in C and it can be ported in nearly all CPU environments. For the development of ISDN phones or TAs IOS has been ported onto an 80C515. Still it might be necessary to do some modifications or more likely add some features. The board can immediately load code but the use of a high level debugger like the Keil (FRANKLIN) TS51 or the IAR (ARCHIMEDES) C-SPY is recommended. After loading the target system Monitor down to the board the debuggers work perfectly. An emulator is really not required.

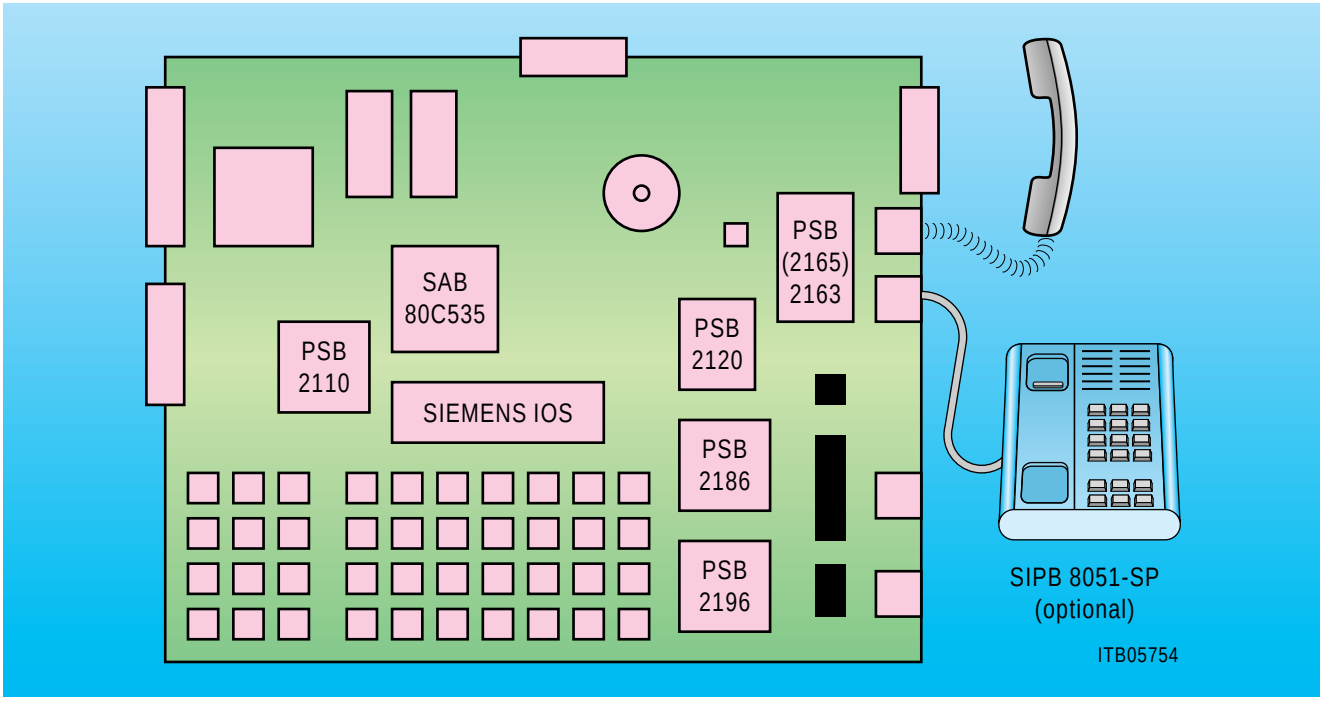
4.2.3 Figuring out the ARCOFI®-SP Coefficients for Speakerphone

Siemens Semiconductor Group offers two dedicated, DSP-based speakerphone realizations ARCOFI-SP PSB 2165 and PSB 2163.

The first digital speakerphone support was implemented in the ARCOFI-SP PSB 2165, which already exists since 1991. A substantial feature of the ARCOFI-SP is to provide means for minimizing feedback in electrical loops and to compensate for acoustical couplings. Therefore ARCOFI-SP offers 23 parameters which are set by software programming. No further external components or trimming are required. This half-duplex mode is based on a two point speech detection, which controls the mode switching within 125 µs.

The speakerphone support of the new ARCOFI-SP PSB 2163 is based on a “Stronger-Wins” algorithm. Two speech comparators, one at the acoustic (AE) and one at the line side (LE), mainly control the switching from one active mode to another one. They compare permanently the signal levels of both signal paths and control the influences caused by the echoes at the acoustic side and at the line side. Once, a speech detector has detected speech activity, the comparator switches immediately to the direction where the speech signal is louder than the other one plus the returned echo.

This offers the advantage of a completely separate programming of the sensitivity and of the echo control. The sensitivity is adjusted by the speech detectors and the speech comparators control the different feedback paths at the acoustic side and at the line side.



The ARCOFI®-SP allows the control of electrical feedbacks. It is recommended, however, to have the majority of the acoustic couplings minimized before, by an optimum design of the telephone case.

For both ARCOFI-SPs there is very comfortable coefficient software called ARCOS-SP PLUS which eases and reduces any optimizations to just a simple task at the PC.

Thanks to the DSP realization, the main operational functions are all parameterized. This technique offers a high level of flexibility and reproducibility. An enormous advantage is the reduction of the optimization time. With a special adaptor[1)] it is possible to optimize the speakerphone system using just one link. The iterated procedure of "Building-up a line → Testing → Deactivating the link → Opening the telephone case → Resoldering some RC elements → Closing the case" is reduced to a comfortable computer session focusing on the real work: the optimization of the switching behaviour. The speakerphone maintenance/test function of the ARCOFI-SP supports the transparency of these modes which are mentioned above (refer to Application Hints for ARCOFI-SP Users).

[1)] Refer to the application Note "Adaptor to program ARCOS-SP in customer hardware with Siemens ISDN PC User Board and ARCOS-SP PLUS"

5 Tools for GSM Telephone Designs

5.1 A Typical GOLDplus Development Environment

The development of a GSM handset splits up into development of GSM hardware and GSM software. Up to a certain stage development will run in parallel converging more and more prior to GSM type approval. Hardware development splits up into development of the baseband part and the RF part with the RF part requiring considerable experience and know-how.

Siemens along with its partners offers support for all stages of both hardware and software development permitting even newcomers to the GSM arena to get started quickly. For application of the GOLDplus chip set Siemens offers local as well as central support from headquarters in Munich. UK based Symbionics offers development of a complete GSM hardware according to customer requirements. For development of the RF hardware they build upon their profound RF experience. Munich based OPTIMAY offers mature GSM software with an easily customizable MMI.

The development of a GSM handset requires both optimum hardware and software development tools to meet time scales in a rapidly moving market.

Hardware Development

GOLDplus Evaluation System

The Siemens GOLDplus evaluation system comprises all parts of a GSM full rate and half rate handset. It consists mainly of the GOLDplusX GSM baseband board and the GOLDplus GSM RF board as shown in **figure 1**.

On the GOLDplusX baseband board all Siemens GOLDplus baseband devices are located including the system controller GOLD-µC (PMB 2706), the signal processor GOLD-SP (PMB 2707), the digital-to-analog conversion device GAIM (PMB 2905) and optionally the half-rate coprocessor GOLD-SX (PMB 2708). All required memory devices like FLASH memory and RAM are also found on this board.

Suitable periphery like LCD display and keypad complete the system to a fully functional handset. The connector to the RF board carries all baseband I- and Q-signals in both receive and transmit direction and all RF-control signals from GOLD-µC.

On the GOLDplus GSM RF board all the Siemens GSM RF devices are located including the transmitter PMB 2240, the receiver PMB 2405, the PLL PMB 2307 and the power amplifier consisting of CGY 92 and CGY 120.

The GOLDplus demo system permits evaluation of all features of the GOLDplus chip set, both for the baseband as well as the RF part. By adding the PMB 2708 half-rate coprocessor the baseband may be upgraded optionally to half-rate operation. Critical parameters like power consumption or equalizer performance can be measured. Cost estimations for a customer handset can be based upon the bill of materials of the board.

GOLDplusX Baseband Board

Software Development Platform

GOLDplusX board permits the customer getting started immediately with his GSM software development without having to wait for his own board prototypes. It provides an optimum debugging platform not only for the GOLD-µC C166 system controller but also for the DSP cores if customer specific features have to be implemented in DSP firmware.

Besides getting quickly acquainted with the baseband functionality the board permits easy and complete control of the RF-chip set using the GOLD-µC controller functions. This is especially useful for evaluation and fine tuning of the RF-board functionality.

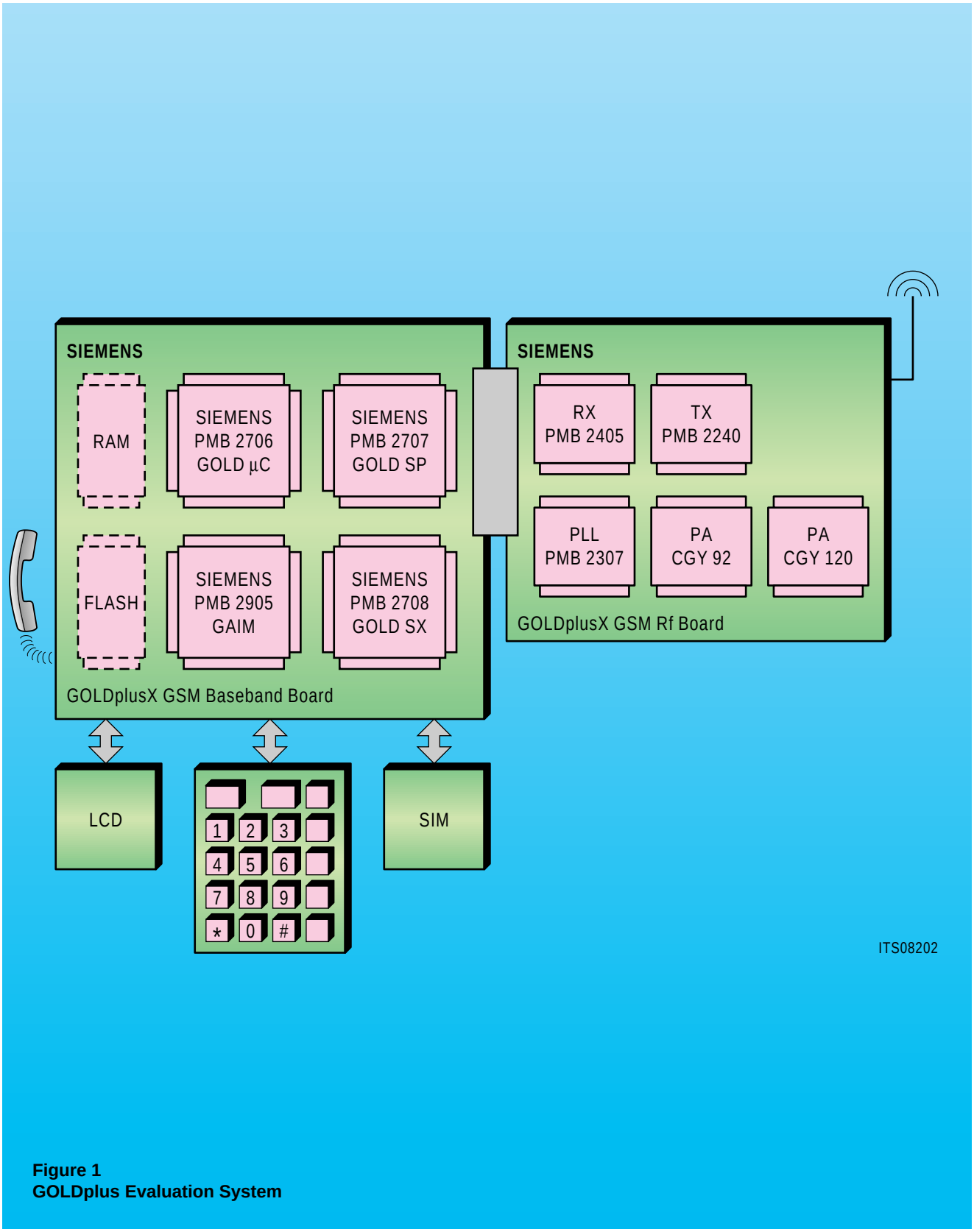


Figure 1
GOLDplus Evaluation System

6 Tools for DECT-Cordless Telephone Designs

6.1 A typical Development Environment for a DECT-Home System

For DECT-home system development projects, there is a complete hardware and software solution available, which was designed to provide a first prototype to the customer. It actually covers all the necessary functional blocks and is fully operational, when connected to an analog telephone network.

The effort was made in order to speed up the development of a DECT-home system and to provide a system hardware for immediate software development. Besides the tremendous know how, especially on the RF part, which is necessary for designing DECT phones, it is now the first time that a european standard protocol has to be matched. The DECT standard actually defines a very complex layered protocol. To implement that standard, a tremendous software development effort has to be made. This part of a DECT project is considered to be done in parallel to the final hardware design. The DECT-user board system provides a hardware development platform today which allows customer's software group to start working immediately.

6.2 Development Steps

6.2.1 Designing the Hardware

In order to speed up this process, all the wiring diagrams are shipped with the boards. Major parts of the hardware shipped can of course be used for the final design. This is especially true for the SWUD 1300 RF board. The SWUD 3020E or SWUD 3025 board respectively has of course to be replaced by the PMB 2720X or PMB 2725X chip along with the E^2PROM and the PMB 2920 chips. However, their interconnection can be taken from of the shipped wiring diagrams of the SWUD board.

The SWUD 1100 board will typically need to be customized because it is very likely that one wants to use a different keyboard layout or a customized display etc.

The major parts of the SWUD 1200 board can again be used to design a real base station telephone line interface.

6.2.2 Developing the Software

A major task in the design work is the development of the DECT-protocol software. The effort is considered to be several man years. The SWUD 3500 setup is designed to support software development projects. The memory layout has been designed in close cooperation with Compiler and Debugger suppliers, with the result that C51 Debuggers can run in this environment.

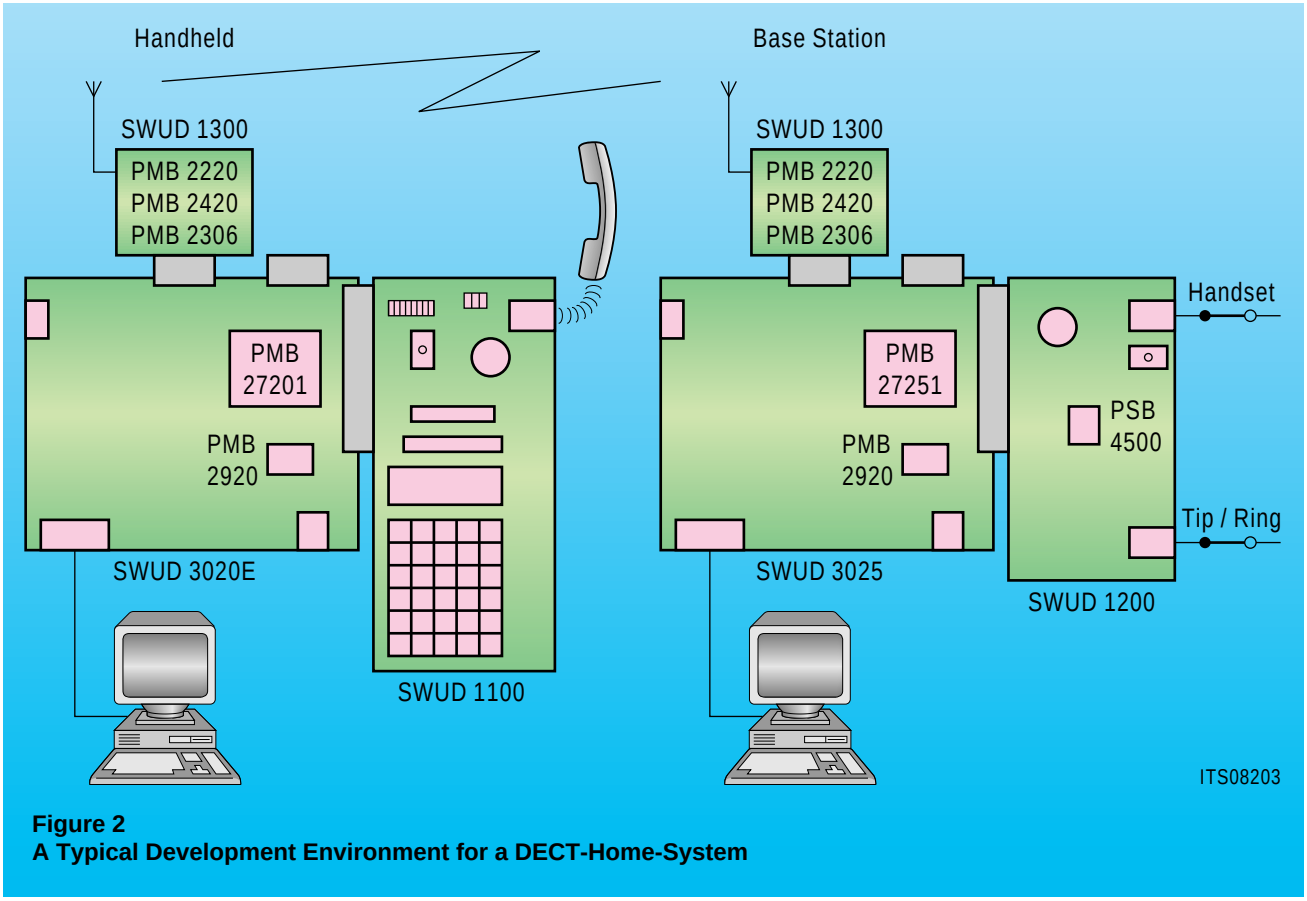


Figure 2
A Typical Development Environment for a DECT-Home-System

The board can immediately load software, but the use of a high-level language debugger like the Keil (Franklin) TS51 is recommended. The monitor program of this third party software package is already shipped with the board to get user started more quickly. For most of the software debugging, an emulator is not really required. But in addition to the described software monitoring by a software debugger, there is also a hardware emulator available from Kleinhenz Electronic. It seems to be a good approach to use the software debugger for most of the daily work, but to have one emulator available for tricky real-time debugging and for final target system software implementations.

Besides hardware, there is also code available to support the development. There is a low level device driver software available which controls the chips.

In addition to that, the source code package PRODECT adds a complete software implementation for a typical home system. This includes all the layers and saves the above-mentioned several man years. PRODECT is marketed as a one time buy out license. It implements the complete DECT standard, and by using PRODECT the customer's software effort is decreased to about 10% for customized modifications.

7 Tools for Universal RF Circuit Designs

For the various RF circuits there are test boards available for evaluation. For distinct applications like the DECT-system-oriented family of user boards a complete RF application has been put together to complete the baseband tool set as a system solution.

8 Tools for ISDN Primary Rate System Designs

The Evaluation System for Primary Rate Interface SIPB 7520 comprises a modular hardware and software architecture. It contains a typical Primary Rate Interface system application based on the Siemens devices HSCX (SAB 82525), ACFA (PEB 2035) and the new PRACT (PEB 22320).

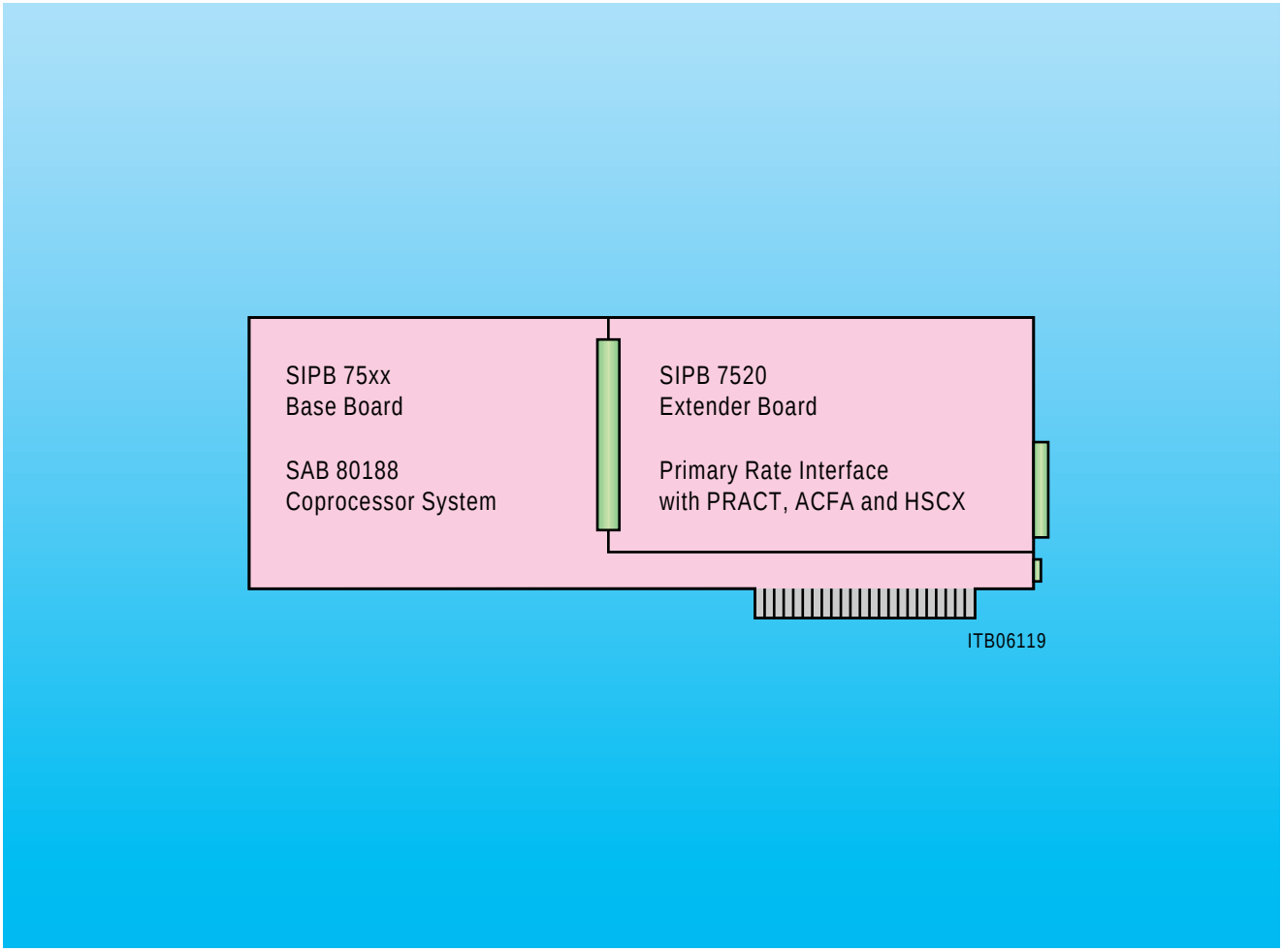
8.1 SIPB 7520 Hardware

The SIPB 7520 hardware consists of a PC base board equipped with an 80188 coprocessor system and an extender board, the new PRACT Evaluation Board, as shown in the following figure.

The base board comprises an 80188 microcontroller, 128 Kbyte local RAM and a DP RAM-based interface to the PC. The PRACT Evaluation Board itself can be used in all applications using E1 or T1 transmission systems. It reflects the features of the Siemens components for a typical application like Primary Access TE, especially the new PRACT device, which contains in addition to the line transceiver a powerful clock generator with PLL. Signaling procedures like CAS or CCS as well as bit-robbed signaling can also be performed.

8.2 SIPB 7520 Software

The SIPB 7520 software comprises the PC Evaluation Software, which realizes the general user access to the Primary Rate Interface system and the Device Driver Software for the Siemens Communication ICs, which can be downloaded onto the SIPB 7520 PC Board. The Device Driver Software contains in addition to a standard HDLC Device Driver Module for the HSCX two new Device Driver Modules for the ACFA V4.1 and PRACT supporting E1 (CRC4) and T1 (ESF, CRC6) systems.



8.3 Primary Rate Extender Board

The block diagram of the Primary Rate Extender Board of figure above shows the main parts of the SIPB 7520 PRACT User Board:

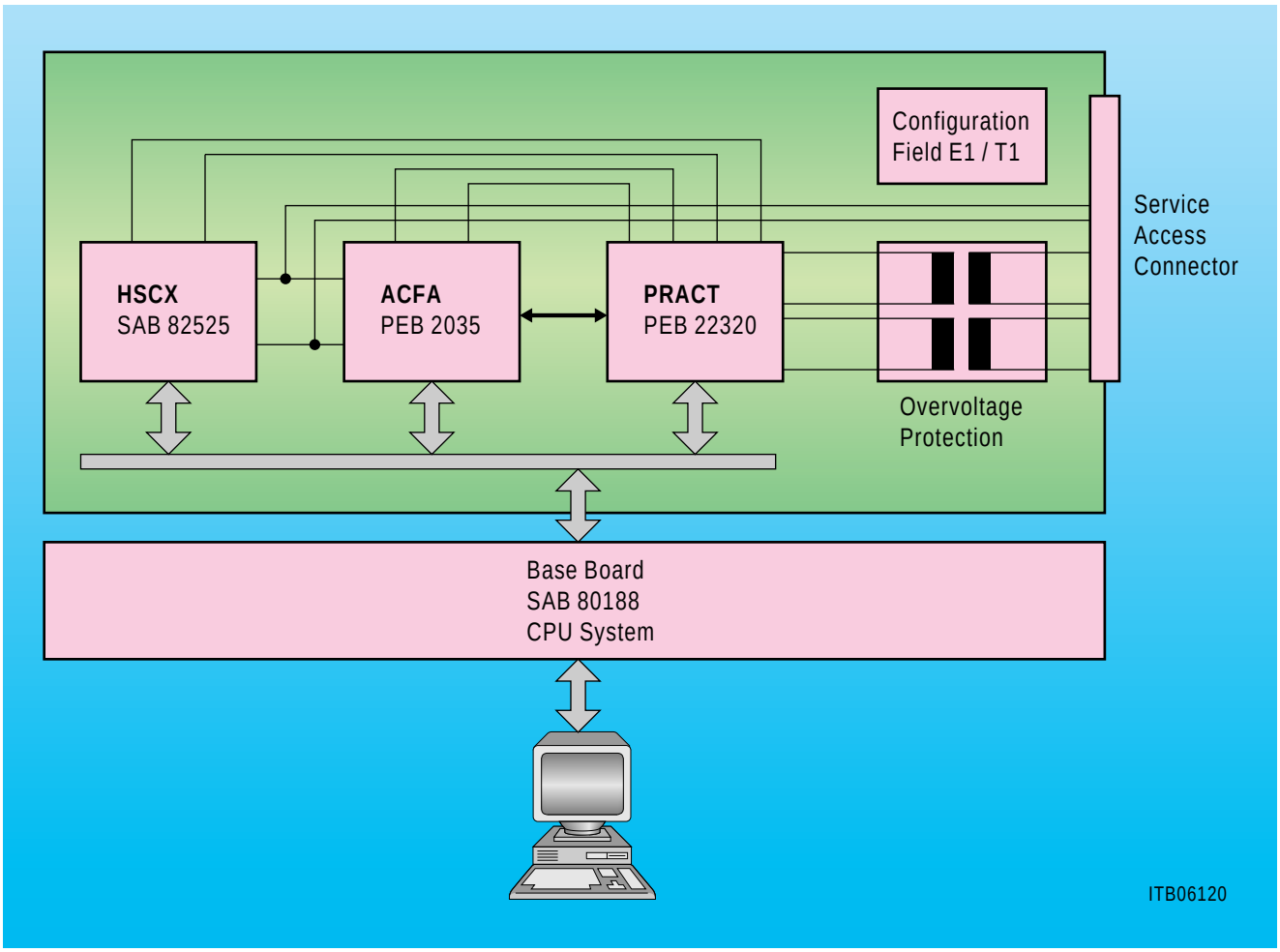
- ISDN Primary Access Clock Generator and Transceiver (PRACT) PEB 22320
- Advanced CMOS Frame Aligner (ACFA) PEB 2035
- High-level Serial Communications Controller eXtended (HSCX) SAB 82525
- Microprocessor System based on SAB 80188
- Configuration field for E1/T1 applications
- Service Access Connector to physical line and for external measurements
- Extender Board Connector
- PC Interface Connector

The most important devices of the SIPB 7520 PRACT Evaluation Board are the Advanced CMOS Frame Aligner (ACFA), the ISDN Primary Access Clock Generator and Transceiver (PRACT) and the High level Serial Communications Controller eXtended (HSCX).

The ACFA contains the main parts of the layer-1 functions of the Primary Rate Interface and performs frame alignment to the incoming data stream. Its activity is supported by the PRACT linking the dual rail interface of the ACFA to E1 or T1 transmission lines which may be accessed via the Service Access Connector (SAC). A dedicated overvoltage protection circuitry is included and screens against voltage surges on the physical line.

The HSCX supports optimized high speed data transmission on DMA or interrupt request using HDLC protocols. It is employed as signaling controller as well as controller for data transmission in time-slot oriented transmission systems. Both channels A and B of the HSCX can be used either for signaling or for data transmission.

All clocks required by the ACFA and the HSCX are generated by the integrated clock PLL of the PRACT.



9 Tools for Communication Networks System Designs

9.1 Datacom Application Board EASY532

The Evaluation & Development System EASY532 provides a hardware and software development tool for communication system applications with the serial communication controller SAB 82532 (ESCC2) using the PC as interface to the user. The relevant features of the SAB 82532 (ESCC2) are supported.

Due to its original concept the Datacom ESCC2-Userboard EASY532 assists an engineer in developing his own applications. It reduces greatly the time spent for hardware and software development in offering not only a ready-to-use circuitry but also a plain and reliable software for operating, modifying, and testing the hardware according to one's own pretensions and requirements. Thus using the Datacom ESCC2-Userboard EASY 532 in a short time leads to a stable hardware development; it provides level-1 and level-2 software support while creating and testing own application software.

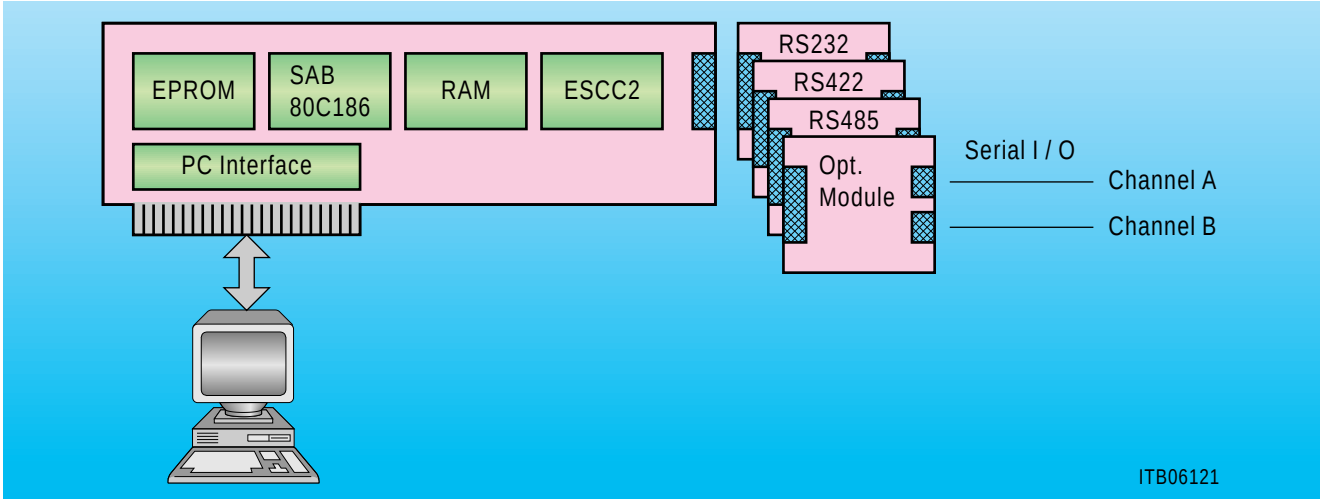
The hardware is designed such as to fit into an expansion slot any PC/XT/AT or compatible. Thus after some simple configuring procedures (e.g. selecting I/O address by means of switches) and insertion of the board into the PC the circuit is just ready for use.

This Datacom Application System comprises an SDA 80186 coprocessor system, a PC Interface with 2-Kbyte Dual Port RAM and the Communication IC ESCC2 from Siemens.

Software for EASY 532

The main features of this powerful integrated Evaluation and Development Software System are:

- The Device Driver Software consists of a **Device Driver System**, including the start-up sode and a run-time library for the EASY 532 80186-coprocessor system. Over 95% of the Device Driver Software is written in C and available in source code.
- The Device Driver Software contains optimized **Device Driver Modules** especially written for the Communication IC ESCC2 from Siemens. These modules demonstrate the features, power and flexibility of the Siemens Communication ICs. The Device Driver Modules are completely written in C. They support the different protocol modes of the ESCC2, e.g. ASYNC, BISYNC, HDLC/ SDLC.
- An **Application Program Interface** (API) for the C language helps writing individual application software for the PC, communicating via a standard interface (C/I Mailbox Interface) with Device Driver Software on the coprocessor board. The program **EXAMPLE** gives a first idea of how to apply the C/I Mailbox API in a simple PC-application program.
- The **EASY532** tool comprises Downland, Debugging and Single Step test features, as well as Sequential Test capabilities. Its main purpose is to simplify the control and verification of Device Driver Software developed on the PC. This driver software can directly be downloaded on the coprocessor board for real-time applications. Furthermore the window driven Register Access Editor presents the Siemens Communication IC ESCC2 in a user-friendly manner. The time, that has to be spent for learning how the chip architecture looks like and how the chip works in principle is reduced to a minimum.
- Application specific software can be developed by the user using so called **"application modules"** (→ apm.c, apm.h). This modules are linked to the Device Driver Software and downloaded on the Datacom Board, thus providing a high performance real time data communication system.
- **Line drivers** like RS232-, RS422-, RS485-drivers, or even optical modules can be connected to the EASY 532 board. Using such drivers or modules different system configurations can be supported, e.g. Master Slave, Multi-Master, Point To Point.



9.2 EASY320 Evaluation System for MUNICH32

General Overview

The Evaluation System for the MUNICH32 comprises modular hardware and software components especially optimized to demonstrate the excellent performance of the MUNICH32 device in a real communication subsystem.

The hardware is divided into a 32-bit CPU base board and an appropriate extender board, which contains an individual system application with the MUNICH32 (e.g. Primary Rate Interface).

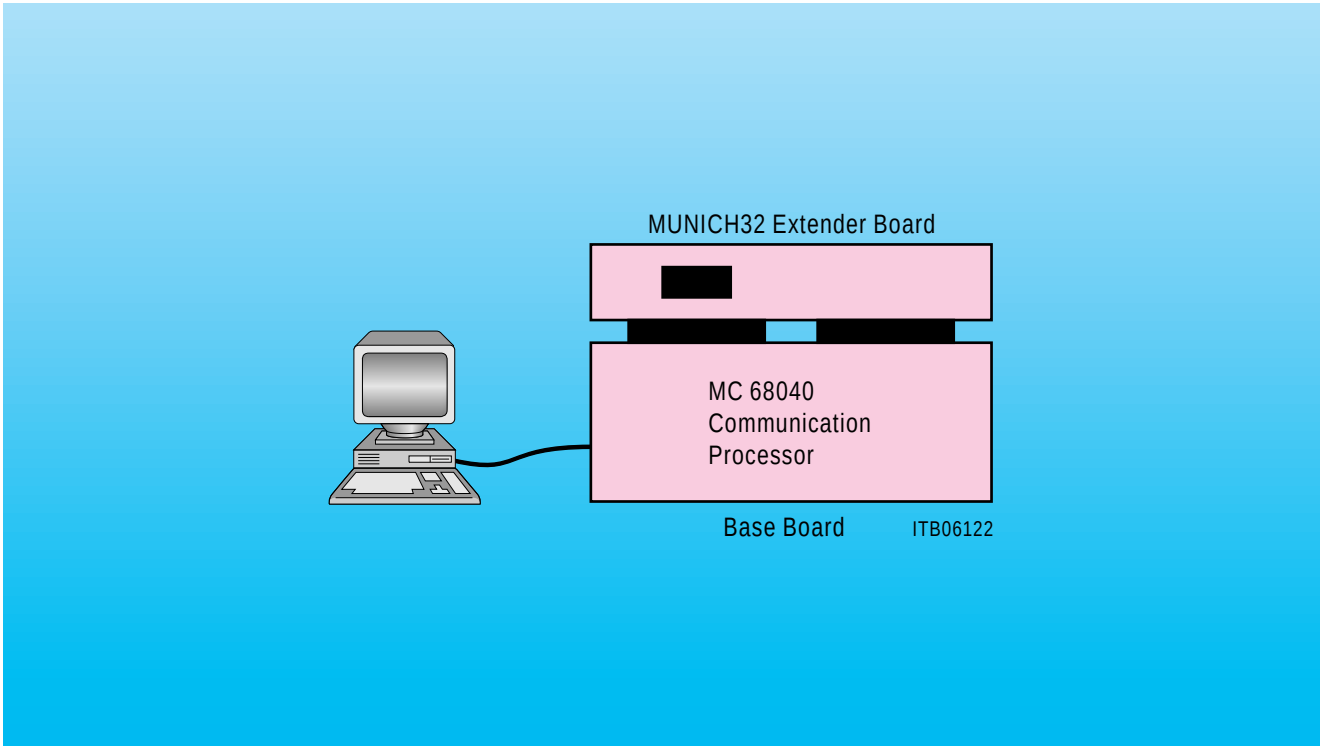
The associated software structure for use with this hardware architecture consists of dedicated device driver software running on the communication subsystem and the corresponding Evaluation Software EASY320 on the PC host system.

The device driver software is available in C source code. With a standard C cross development package for the 32-bit CPU it is possible to generate executable code which can be downloaded onto the communication subsystem with the EASY320 download utility.

For a quick start using the MUNICH32 device in such a minimum reference system a sophisticated Windows user interface is built into the EASY320 PC-Evaluation Software especially designed for the MUNICH32 shared memory data structures. This user interface simplifies the direct access to the MUNICH32 device by mapping the MUNICH32 data structures to corresponding window structures on the PC.

Applications

- Intuitive learning by doing “How the MUNICH32 behaves in a real system”
- Realization of individual system applications
- Development and test of individual MUNICH32 device driver software

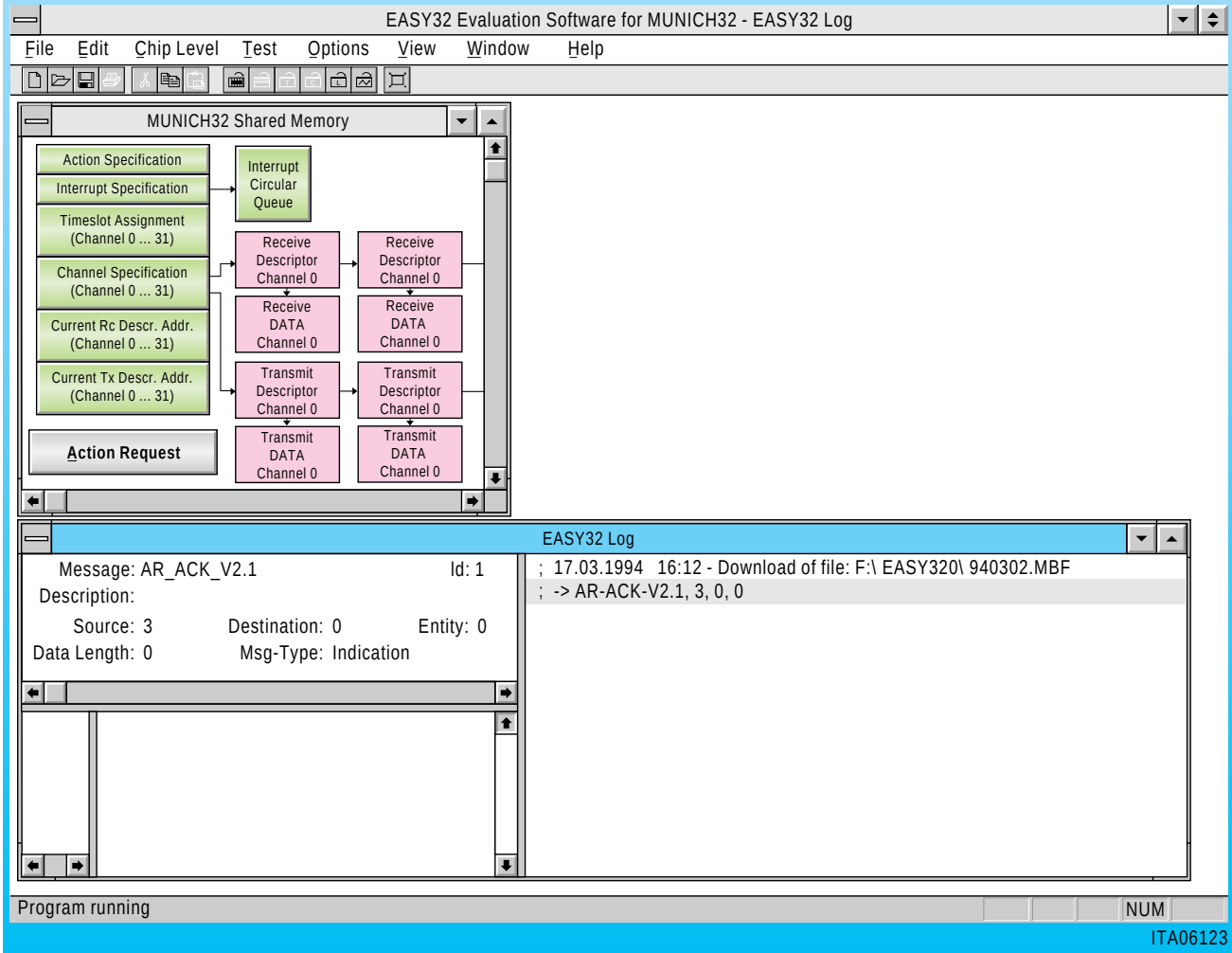


PC Evaluation Software EASY320

The PC Evaluation Software EASY320 is a single MS-Windows application program containing mainly the following functional modules:

- Download of communications software onto the EASY320 communication subsystem
- Single Step Test of downloaded communications software via the exchange of C/I Messages
- Direct Chip Level Access to MUNICH32 shared memory data structures

The initial screen view is illustrated in the following figure.



EASY320 Initial Screen View

Package Information

Package Outlines of the desribed Products are shown in our Databook “Package Information”

Package Information

Datenbuch „Gehäuse Information“

Der Bereich Halbleiter stellt dem interessierten Leser, praktischen Anwender und Kunden seine Gehäusevielfalt vor und gibt zusätzlich Informationen zu den Themen, die im Gesamtzusammenhang mit Gehäusen stehen.

Die Gehäusethematik gewinnt nicht nur für den Halbleiterhersteller als Folge größer werdender Chips sowie steigender Arbeitsfrequenz immer mehr an Bedeutung, sondern gerade auch für den Verarbeiter und Kunden, der mit einer ständig wachsenden Vielfalt an Gehäusen hinsichtlich Pinzahl, Anschlußraster und Gehäuseabmessungen konfrontiert wird. Aus diesem Grunde sollte die Auswahl der Produkte nicht nur auf den Chip, sondern auch auf die Gehäuse und damit auf die spätere Verarbeitung bezogen werden, um die Machbarkeit und Wirtschaftlichkeit sicherzustellen.

Das Einführungskapitel behandelt die weltweite Gehäusestruktur und deren Trend für die Zukunft und die sich aus der zunehmenden Diversifizierung an Gehäusen ergebende Problematik für den Verarbeiter.

Die Kapitel 2 bis 4 behandeln detailliert Abmessungen, Kenngrößen und Beschriftungen der typischen Gehäuse des Bereichs Halbleiter

Der Verpackung haben wir wegen ihrer steigenden Bedeutung als Bindeglied zwischen Halbleiterhersteller und Verarbeiter ein eigenes Kapitel (5) gewidmet.
Nützliche Hinweise zur Verarbeitung von Bauelementen enthält Kapitel 6. Die einzelnen Prozeßschritte werden beschrieben und die Vor- und Nachteile der unterschiedlichen Verfahren diskutiert. Auf die Verarbeitung feuchteempfindlicher ICs sowie auf elektrostatisch gefährdeter Bauelemente ESD wird gesondert eingegangen .

Ein Gehäuseverzeichnis rundet das Gehäuse-Datenbuch ab

Bestell-Nr.: B192-H6636-G1-X-7400
(Siehe auch Abschnitt „Literaturhinweise“)

Databook “Package Information”

The Siemens Semiconductor Group wishes to introduce interested readers, practical users, and its customers to its numerous packages, and to present information on the subjects directly associated with packages.

Packaging is becoming increasingly important as a consequence of larger chips and higher operating frequencies, not only for the semiconductor manufacturer but specifically for processors and customers confronted with a steadily growing variety of packages with regard to pin count, pin raster and package sizes. For this reason, product selection should involve not just the chip but also the packages and, consequently, subsequent processing in order to ensure feasibility and economy

The opening section deals with the worldwide pattern of packages and their future trend, while special mention is made of the problems facing processors as a result of increasing package diversification.

Sections 2 to 4 present a detailed discussion of dimensions, characteristics, and markings of typical packages from the Semiconductor Group.

In view of its rising importance as a link between the manufacturer of semiconductors and their processors a whole chapter (5) has been devoted to packing.

Useful advice on processing devices is contained in Section 6. The different process stages are described, and the pros and cons of the different methods are discussed. Special mention is made of processing humidity-sensitive ICs and anti-ESD measures.

A list of packages, completes the Package Data Book.

Ordering No.: B192-H6636-G1-X-7400
(see refer section “Information on Literature”)

Summary of Types

Summary of Types in Alphanumerical Order

Type	Short Title	Function	Page
PEB 2025-N	lEPC	ISDN Exchange Power Controller (SMD)	121
PEB 2025-P	lEPC	ISDN Exchange Power Controller	121
PEB 2026T-P	IHPC	ISDN High Voltage Power Controller (SMD)	106
PEB 2026T-S	IHPC	ISDN High Voltage Power Controller (SMD)	106
PEB 20320-H	MUNICH32	Multichannel Network Interface Controller for HDLC (SMD)	167
PEB 2035-N	ACFA	Advanced CMOS Frame Aligner (SMD)	132
PEB 2035-P	ACFA	Advanced CMOS Frame Aligner	132
PEB 2045-N	MTSC	Memory Time Switch CMOS (SMD)	147
PEB 2045-P	MTSC	Memory Time Switch CMOS	147
PEB 2046-N	MTSS	Memory Time Switch Small (SMD)	150
PEB 2046-P	MTSS	Memory Time Switch Small	150
PEB 2047-16-N	MTSL-16	Memory Time Switch Large (SMD)	153
PEB 2047-N	MTSL	Memory Time Switch Large (SMD)	151
PEB 2052-N	PIC	PCM Interface Controller (SMD)	89
PEB 2054-N	EPIC®-S	Extended PCM Interface Controller-Small (SMD)	90
PEB 2055-N	EPIC®-1	Extended PCM Interface Controller (SMD)	91
PEB 20550-H	ELIC®	Extended Line Card Controller (SMD)	92
PEB 20560	DOC	DSP Oriented PBX Controller (SMD)	122
PEB 2060-N	SICOFI®	Signal Processing Codec Filter (SMD)	94
PEB 2060-P	SICOFI®	Signal Processing Codec Filter	94
PEB 2070-N	ICC	ISDN Communications Controller (SMD)	107
PEB 2070-P	ICC	ISDN Communications Controller	107
PEB 2075-N	IDEC®	ISDN D-Channel Exchange Controller (SMD)	109
PEB 2075-P	IDEC®	ISDN D-Channel Exchange Controller	109
PEB 2080-N	SBC	S-Bus Interface Circuit (SMD)	110
PEB 2080-P	SBC	S-Bus Interface Circuit	110
PEB 2081-N	SBCX	S/T-Bus Interface Circuit Extended (SMD)	111
PEB 2084-H	QUAT®-S	Quadruple S/T-Transceiver (SMD)	112
PEB 2085-N	ISAC®-S	ISDN Subscriber Access Controller (SMD)	61
PEB 2085-P	ISAC®-S	ISDN Subscriber Access Controller	61
PEB 2086-H	ISAC®-S	ISDN Subscriber Access Controller (SMD)	61
PEB 2086-N	ISAC®-S	ISDN Subscriber Access Controller (SMD)	61
PEB 20901-N	IEC-T	ISDN Echo Cancellation Circuit (SMD)	114
PEB 20901-P	IEC-T	ISDN Echo Cancellation Circuit	114
PEB 20902-N	IEC-T	ISDN Echo Cancellation Circuit (SMD)	114
PEB 20902-P	IEC-T	ISDN Echo Cancellation Circuit	114
PEB 2091-N	IEC-Q	ISDN Echo Cancellation Circuit (SMD)	113
PEB 2095-N	IBC	ISDN Burst Transceiver Circuit (SMD)	119
PEB 2095-P	IBC	ISDN Burst Transceiver Circuit	119
PEB 20950-N	ISAC®-P	ISDN Subscriber Access Controller (SMD)	63
PEB 20950-P	ISAC®-P	ISDN Subscriber Access Controller	63
PEB 2096	OCTAT®-P	Octal Transceiver for U_{PN} Interfaces (SMD)	120
PEB 22320-N	PRACT	Primary Access Clock and Transceiver Component (SMD)	139
PEB 2236-N	IPAT®-2	ISDN Primary Access Transceiver (SMD)	134
PEB 2236-P	IPAT®-2	ISDN Primary Access Transceiver	134

Summary of Types in Alphanumerical Order

Type	Short Title	Function	Page
PEB 2254-H	FALC™54	Frame And Line Interface Component (SMD)	136/178
PEB 2260-N	SICOFI®-2	Dual Channel Codec Filter (SMD)	96
PEB 2445-N	MUSAC™-A	Multipoint Switching and Conferencing Unit Attenuation (SMD)	154
PEB 2465-H	SICOFI®-4	Signal Processing Codec Filter (SMD)	97
PEB 2466-H	SICOFI®-4 µC	Signal Processing Codec Filter (SMD)	99
PEB 24901	Quad IEC DFE-T	4 Channel ISDN Echo-Cancellation Digital Front End (SMD)	116
PEB 24902	Quad IEC AFE	Quad ISDN Echo-Cancellation Circuit Analog Front End (SMD)	117
PEB 24911	Quad IEC DFE-Q	Quad ISDN 2B1Q Echocanceller Digital Front End (SMD)	118
PEB 3035-N	PRISM	Primary Rate Interface Signaling and Maintenance Controller (SMD)	135
PEB 3035-P	PRISM	Primary Rate Interface Signaling and Maintenance Controller	135
PEB 3065-N	SLICOFI®	Signal Processing Subscriber Line Interface Codec Filter (SMD)	100
PEB 4065-T	HV-SLIC	High Voltage Subscriber Line (SMD)	101
PEF 2026T-P	IHPC	ISDN High Voltage Controller (SMD)	106
PEF 2026T-S	IHPC	ISDN High Voltage Controller (SMD)	106
PEF 20320-H	MUNICH32	Multichannel Network Interface Controller for HDLC (SMD)	167
PEF 2035-N	ACFA	Advanced CMOS Frame Aligner (SMD)	132
PEF 2035-P	ACFA	Advanced CMOS Frame Aligner	132
PEF 2045-N	MTSC	Memory Time Switch CMOS (SMD)	147
PEF 2045-P	MTSC	Memory Time Switch CMOS	147
PEF 2054-N	EPIC®-S	Extended PCM Interface Controller-Small (SMD)	90
PEF 2055-N	EPIC®-1	Extended PCM Interface Controller (SMD)	91
PEF 2070-N	ICC	ISDN Communication Controller (SMD)	107
PEF 2075-N	IDEC®	ISDN D-Channel Exchange Controller (SMD)	109
PEF 2080-N	SBC	S-Bus Interface Circuit (SMD)	110
PEF 20901-N	IEC-T	ISDN Echo Cancellation Circuit (SMD)	114
PEF 20902-N	IEC-T	ISDN Echo Cancellation Circuit (SMD)	114
PEF 2091-N	IEC-Q	ISDN Echo Cancellation Circuit (SMD)	113
PEF 2236-N	IPAT®-2	ISDN Primary Access Transceiver (SMD)	134
PEF 2236-P	IPAT®-2	ISDN Primary Access Transceiver	134
PEF 2260-N	SICOFI®-2	Dual Channel Codec Filter (SMD)	94
PEF 24902	Quad IEC AFE	Quad ISDN Echo-Cancellation Circuit Analog Front End (SMD)	117
PEF 24911	Quad IEC DFE-Q	Quad ISDN 2B1Q Echocanceller Digital Front End (SMD)	118
PEF 3035-N	PRISM	Primary Rate Interface Signaling and Maintenance Controller (SMD)	135
PEF 3035-P	PRISM	Primary Rate Interface Signaling and Maintenance Controller	135
PEF 3065-N	SLICOFI®	Signal Processing Subscriber Line Interface Codec Filter (SMD)	100
PEF 4065-T	HV-SLIC	High Voltage Subscriber Line (SMD)	101
PMB 2200-S		Direct Vector Modulator (SMD) (Shrink)	37
PMB 2200-T		Direct Vector Modulator (SMD)	37
PMB 2201-R		Direct Vector Modulator + Mixer (SMD)	38
PMB 2202-R		Direct Vector Modulator + Mixer (SMD)	38
PMB 2205-S		Direct Vector Modulator (SMD) (Shrink)	41
PMB 2205-T		Direct Vector Modulator (SMD)	41
PMB 2207-R		Direct Vector Modulator + Upconverter Mixer (SMD) (Shrink)	42
PMB 2220-S		DECT Transmitter (SMD) (Shrink)	33
PMB 2240-F		GSM Transmitter (SMD)	21

Summary of Types in Alphanumerical Order

Type	Short Title	Function	Page
PMB 2245-F		PCN Transmitter (SMD)	21
PMB 2247-F		PCS Transmitter (SMD)	21
PMB 2302-R		1.25-GHz Dual PLL with Prescaler (SMD) (Shrink)	45
PMB 2303-R		2.5-GHz Dual PLL with Prescaler (SMD) (Shrink)	45
PMB 2306-R		PLL Frequency Synthesizer (SMD) (Shrink)	47
PMB 2306-T		PLL Frequency Synthesizer (SDM)	47
PMB 2307-R		PLL Frequency Synthesizer (SMD) (Shrink)	47
PMB 2308-R		1.25-GHz PLL with Prescaler (SMD) (Shrink)	49
PMB 2309-R		2.5-GHz PLL with Prescaler (SMD) (Shrink)	49
PMB 2313-T		1.1-GHz Prescaler (SMD)	51
PMB 2314-T		2.1-GHz Prescaler (SMD)	51
PMB 2330-T		2.0-GHz Mixer (SMD)	52
PMB 2331-T		2.0-GHz Mixer (SMD)	52
PMB 2332-R		1.1-GHz LNA + Mixer (SMD) (Shrink)	53
PMB 2333-R		3-GHz LNA/Driver + Mixer (SMD) (Shrink)	54
PMB 2401-S		Receiver/Demodulator Circuit (SMD) (Shrink)	43
PMB 2401-T		Receiver/Demodulator Circuit (SMD)	43
PMB 2402-S		Broadband Receiver/Vector Demodulator (SMD)	44
PMB 2405-F		GSM Receiver (SMD)	23
PMB 2407-F		PCN/PCS Receiver (SMD)	23
PMB 2420-S		DECT Receiver (SMD) (Shrink)	34
PMB 2705-F	GOLD	GSM One-Chip Logic Device (SMD)	14
PMB 2706-F	GOLD-µC	GOLD System Controller (SMD)	16
PMB 2707-F	GOLD-SP	GOLD Signal Processor (SMD)	18
PMB 2708-F	GOLD-SX	GSM Co-Processor for Advanced Features (SMD)	18
PMB 27201		DECT Digital Circuit for Handhelds (SMD)	28
PMB 27202		DECT Digital Circuit for Handhelds (SMD)	28
PMB 27251		DECT Digital Circuit for Basestations (SMD)	29
PMB 27252		DECT Digital Circuit for Basestations (SMD)	29
PMB 2727-H		DECT Multichannel Burst Mode Controller (SMD)	30
PMB 2728-H		DECT PBX (SMD)	31
PMB 2900-H	GBBC	GSM Baseboard Codec (SMD)	19
PMB 2905-F	GAIM	GSM Analog Infterfacing Module (SMD)	20
PMB 2920-S		DECT Analog Circuit (SMD) (Shrink)	32
PSB 2110-H	ITAC®	ISDN Terminal Adaptor Circuit (SMD)	74
PSB 2110-N	ITAC®	ISDN Terminal Adapter Circuit (SMD)	74
PSB 2110-P	ITAC®	ISDN Terminal Adaptor Circuit	74
PSB 21525-H	HSCX-TE	High-Level Serial Communications Controller for Terminals (SMD)	75
PSB 21525-N	HSCX-TE	High-Level Serial Communications Controller for Terminals (SMD)	75
PSB 2160-N	ARCOFI®	Audio Ringing Codec Filter (SMD)	68
PSB 2160-P	ARCOFI®	Audio Ringing Codec Filter	68
PSB 2161	ARCOFI®-BA	Audio Ringing Codec Filter Basic Function (SMD)	69
PSB 2163-N	ARCOFI®-SP	Audio Ringing Codec Filter (SMD)	70
PSB 2163-P	ARCOFI®-SP	Audio Ringing Codec Filter	70
PSB 2163-T	ARCOFI®-SP	Audio Ringing Codec Filter (SMD)	70

Summary of Types in Alphanumerical Order

Type	Short Title	Function	Page
PSB 2165-N	ARCOFI®-SP	Audio Ringing Codec Filter (SMD)	71
PSB 2165-P	ARCOFI®-SP	Audio Ringing Codec Filter	71
PSB 2186-H	ISAC®-S TE	ISDN Subscriber Access Controller for Terminals (SDM)	62
PSB 2186-N	ISAC®-S TE	ISDN Subscriber Access Controller for Terminals (SMD)	62
PSB 2186-P	ISAC®-S TE	ISDN Subscriber Access Controller for Terminals	62
PSB 2196-H	ISAC®-P TE	Subscriber Access Controller for U_{PN}-Interface Terminals (SMD)	64
PSB 2196-N	ISAC®-P TE	ISDN Subscriber Access Controller for U_{PN}-Interface Terminals (SMD)	64
PSB 2197-T	SmartLink-P	Subscriber Access Controller for U_{PN}-Interface Terminals (SMD)	66
PSB 7110-F	ISAR	ISDN Data Access Controller (SMD)	73
PSB 7280-H	JADE	Joint Audio Decoder/Encoder (SMD)	76
PXB 4110	SARE™	Segmentation and Reassembly Element (SMD)	180
PXB 4220	IWE™	Interworking Element (SMD)	179
PXB 4230	UTPT™	Unshielded Twisted Pair Transceiver (SMD)	181
PXB 4240	SDHT	SDH/SONET Transceiver (SMD)	182
PXB 4310	ASM™	ATM-Switching Matrix	183
PXB 43201	ASP™-up	ATM-Switching Preprocessor Chip Set	184
PXB 43202	ASP™-down	ATM-Switching Preprocessor Chip Set	184
SAB 82525-H	HSCX	High-Level Serial Communication Controller Extended (SMD)	162
SAB 82525-N	HSCX	High-Level Serial Communication Controller Extended (SMD)	162
SAB 82526-N	HSCX	High-Level Serial Communication Controller Extended (SMD)	162
SAB 82532-N	ESCC2	Enhanced Serial Communication Controller (SMD)	163
SAB 82532-N-10	ESCC2	Enhanced Serial Communication Controller (SMD)	163
SAB 82538-H	ESCC8	Enhanced Serial Communication Controller (SMD)	165
SAB 82538-H-10	ESCC8	Enhanced Serial Communication Controller (SMD)	165
SAB 82C257-1-N	ADMA	Advanced DMA Controller for 16-Bit Microcomputer Systems (SMD)	169
SAB 82C258A-12-N	ADMA	Advanced DMA Controller for 16-Bit Microcomputer Systems (SMD)	169
SAB 82C258A-20-N	ADMA	Advanced DMA Controller for 16-Bit Microcomputer Systems (SMD)	169
SAF 82525-N	HSCX	High-Level Serial Communication Controller Extended (SMD)	162
SAF 82526-N	HSCX	High-Level Serial Communication Controller Extended (SMD)	162

Schule für Mikroelektronik

Gehen Sie auf Erfolgskurs!

Programm SS 1996 der Schule für Mikroelektronik

Das Angebot: ca. 130 Kurse von April bis Ende September 1996 zu aktuellen Themen der Mikroelektronik. Praxisorientierte Ausrichtung, modernste Ausstattung, pädagogisch aufbereitetes Kursmaterial und die intensive Betreuung durch Fachdozenten garantieren den Lernerfolg.

Highlights aus dem Kursprogramm:

- 8-bit MC-Familie 8051/C500
- 16-bit MC-Familie C166
- Fuzzy-Logic
- ISDN, Telecom
- Rechnerfamilie 80x86/Pentium
- Hardwarebeschreibungssprache VHDL
- BLS Board Level Simulation
- Software:
  Sprachen C, C++
  Betriebssysteme RMOS, Windows, UNIX
  – Windows Programmierung
- Personalcomputer
- Netze, LWL
- EMV
- Leistungshalbleiter
- Halbleitertechnologie

Auf Wunsch
„maßgeschneiderte“ Kurse in deutscher und englischer Sprache in Ihrer Firma!

Programmübersicht erhalten Sie kostenlos bei:

MicroConsult GmbH
Schule für Mikroelektronik
Rosenheimer Str. 143 b

Frau Kandlbinder

D-81671 München

Tel. (089) 4506 17-0
Fax (089) 4506 17-17

Leistungsbeweis ’95: 2.400 Kurs-Teilnehmer!

Microelectronics Training Center

Hit the Road to Success!

SS 1996 Program of the Microelectronics Training Center

What is offered: e.g. 130 courses from April through to the end of September 1996 on current topics from the field of microelectronics. Practical orientation, the very latest aids, course material devised to modern pedagogic guidelines and intensive support from specialist lectures guarentee learning with success.

Program highlights:

- 8-bit MC family 8051/C500
- 16-bit MC family C166
- Fuzzy logic
- ISDN, telecom
- 80x86/Pentium computer family
- VHDL hardware description language
- BLS Board Level Simulation
- Software:
  C, C++ languages
  RMOS, Windows, UNIX operating systems
  – Windows programming
- Personal computers
- Networks, fiber optics
- EMC
- Power semiconductors
- Semiconductor technology

On request
“tailored” courses on your premises!

Call or write for a free syllabus:

MicroConsult GmbH
Schule für Mikroelektronik
Rosenheimer Str. 143 b

Frau Kandlbinder

D-81671 München

Tel. (089) 4506 17-0
Fax (089) 4506 17-17

Popularity curve: 2.400 course participants in 1995!

Literaturhinweise

Information on Literature