TS4851

1W LOUDSPEAKER & 2x160mW HEADSET BTL DRIVERS WITH DIGITAL VOLUME CONTROL

ADVANCE DATA

- OPERATING FROM V_{cc} **= 3V to 5.5V**
- RAIL TO RAIL **INPUT/OUTPUT**
- **1W :** OUTPUT POWER @ Vcc=5V, THD+N=1%, F=1kHz, 8Ω LOAD
- **160mW :** OUTPUT POWER @ Vcc=5V, THD+N=1%, F=1kHz, 32Ω LOAD
- **HEADSET :** 30mW inStereo @ Vcc=3V
- **THD+N < 0.5%** Max @ 20mW into 32Ω BTL, 50Hz<Frequency<20kHz
- **DIGITAL VOLUME CONTROL :** 32 steps from **-34.5dB to +12dB**
- **+6dB** Power Up Volume & full STDBY
- **OUTPUT MODE:** 8 different selections
- POP & CLICK REDUCTION CIRCUITRY
- LOW SHUTDOWN CURRENT (< 100nA)
- THERMAL SHUTDOWN PROTECTION
- **FLIP CHIP Package** 18 X300µm Bumps

DESCRIPTION

The TS4851 is consisted of an Audio Power Amplifier capable of delivering 400mW (typ) of continuous RMS. output power into 8Ω load with 1% THD+N value and a headset driver featuring 30mW (Typ) per channel of continuous average power into stereo 32Ω bridged tied load with 0.5% THD+N @ 3.3V.

This device features 32 steps digital volume control and 8 differents output selections. The digital volume and output modes are controlled thru a SPI interface bus consisted of three digits.

APPLICATIONS

- Mobile Phones

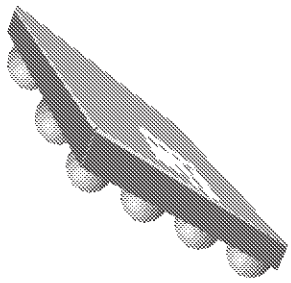
ORDER CODE

Part Number	Temperature Range	Package
		J
TS4851IJT	-40, +85°C	•

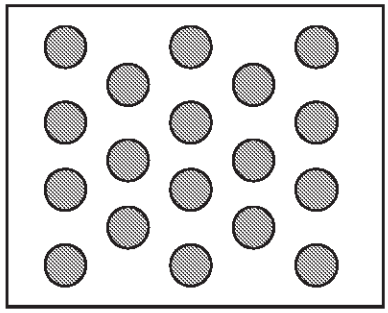
J = Flip Chip Package - only available in Tape & Reel (JT))

PIN CONNECTIONS (top view)

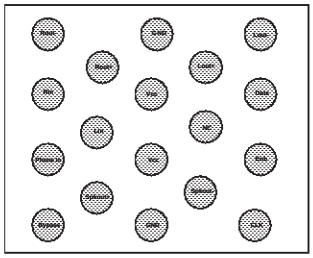
TS485IJT - Flip CHip 18 Bumps



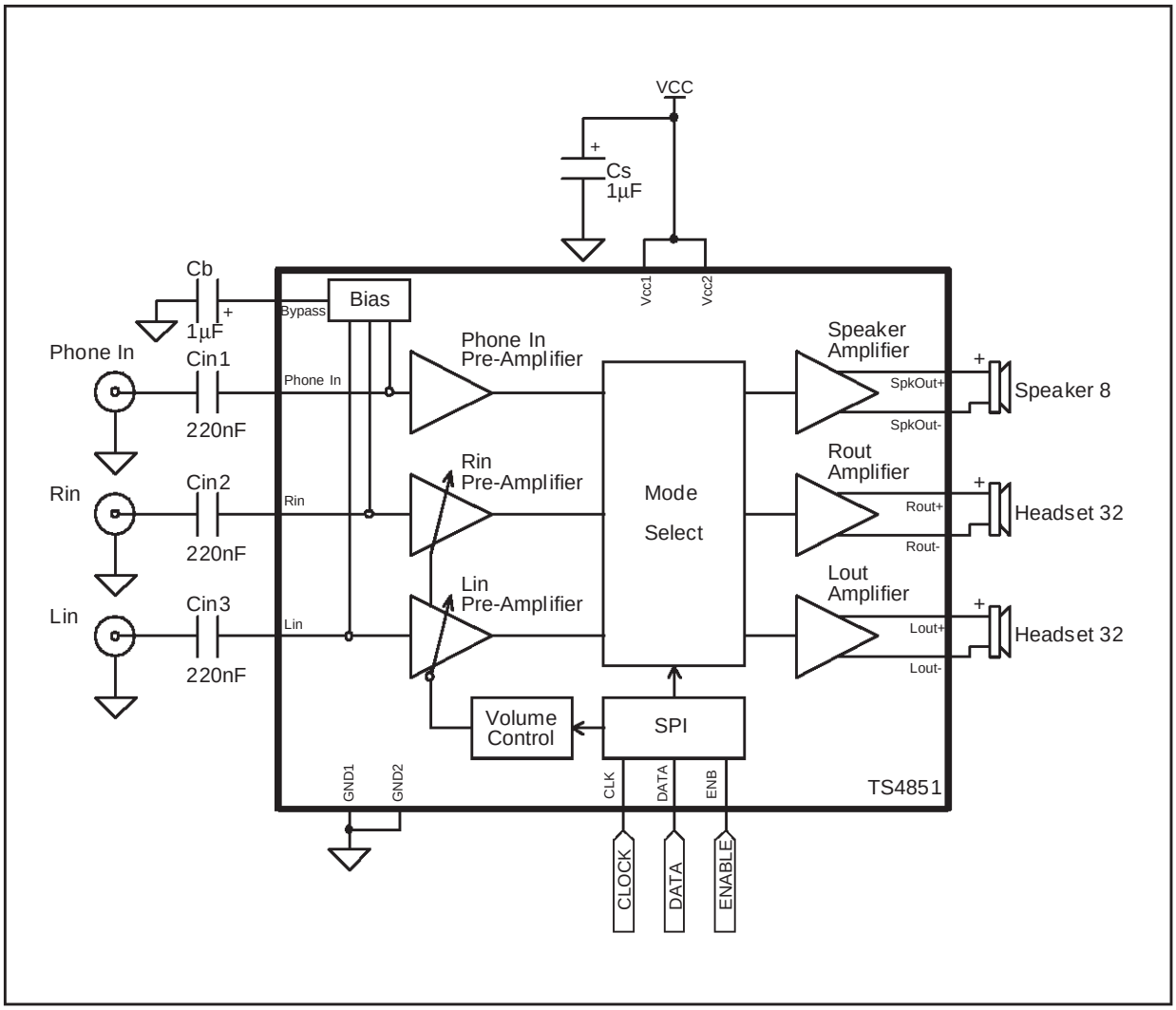
ASYMETRIC Bumping



Pin Out (top view)



TYPICAL APPLICATION



External components Description

Component	Functional Description
C_{in}	This is the input coupling capacitor. It blocks the DC voltage at, and couples the input signal to the amplifier's input terminals. Cin, also creates a highpass filter with the internal input impedance Zin at Fc =1/ (2pixZinxCin).
C_S	This is the Supply Bypass capacitor. It provides power supply filtering.
C_B	This is the Bypass pin capacitor. It provides half-supply filtering.

SPI BUS INTERFACE : Pin Description

Pin	Functional Description
DATA	This is the serial data input pin
CLK	This is the clock input pin
ENB	This is the SPI enable pin active at high level

SPI OPERATION DESCRIPTION

The serial data bits are organized into a field containing 8 bits of data defined by TABLE 1 showed below. The DATA 0 to DATA 2 bits determine the output mode of the TS4851 as shown in the TABLE 2. The DATA 3 to DATA 7 bits determine the gain level setting as illustrated by TABLE 3. For each SPI transfer, the data bits are written to the DATA pin with the least significant bit (LSB) first. All serial data are sampled at the rising edge of the CLK signal. Once all the data bits have been sampled, ENB transitions from logic-high to logic low to complete the SPI sequence. All 8 bits must be received before any data latch can occur. Any excess CLK and DATA transitions will be ignored after the height rising clock edge has occured. For any data sequence longer than 8 bits, only the first 8 bits will get loaded into the shift register and the rest of the bits will be disregarded.

Table 1: Bit Allocation

	DATA	MODES
LSB	DATA 0	Mode 1
	DATA 1	Mode 2
	DATA 2	Mode 3
	DATA 3	gain 1
	DATA 4	gain 2
	DATA 5	gain 3
	DATA 6	gain 4
MSB	DATA 7	gain 5

Table 2: Ouput Mode Selection : K from -34.5dB to + 12dB (by step of 1.5dB)

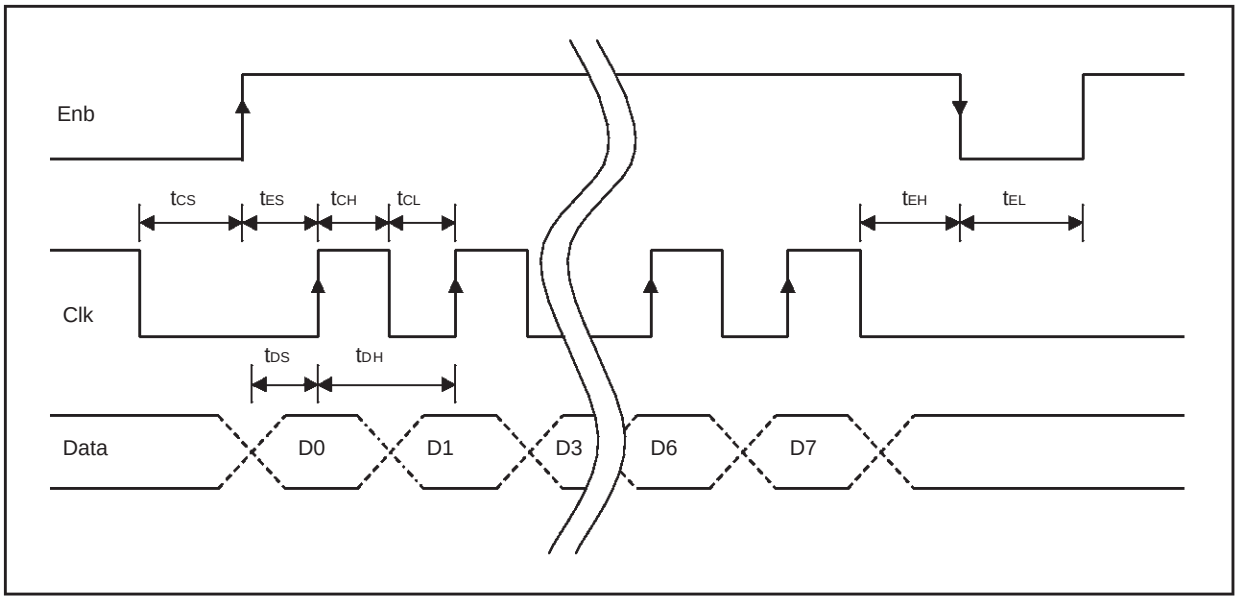
Output Mode #	DATA 2	DATA 1	DATA 0	SPKERout	Rout	Lout
0	0	0	0	SD	SD	SD
1	0	0	1	6dBxP	SD	SD
2	0	1	0	SD	0dBxP	0dBxP
3	0	1	1	Kx(R+L)	SD	SD
4	1	0	0	SD	KxR	KxL
5	1	0	1	Kx(R+L) +6dBxP	SD	SD
6	1	1	0	SD	KxR+0dBxP	KxL+0dBxP
7	1	1	1	6dBxP	KxR+0dBxP	KxR+0dBxP

(SD = Shutdown Mode)

Table 3: Volume Control Settings

K : Gain (dB)	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3
-34.5	0	0	0	0	0
-33.0	0	0	0	0	1
-31.5	0	0	0	1	0
-30.0	0	0	0	1	1
-28.5	0	0	1	0	0
-27.0	0	0	1	0	1
-25.5	0	0	1	1	0
-24.0	0	0	1	1	1
-22.5	0	1	0	0	0
-21.0	0	1	0	0	1
-19.5	0	1	0	1	0
-18.0	0	1	0	1	1
-16.5	0	1	1	0	0
-15.0	0	1	1	0	1
-13.5	0	1	1	1	0
-12.0	0	1	1	1	1
-10.5	1	0	0	0	0
-9.0	1	0	0	0	1
-7.5	1	0	0	1	0
-6.0	1	0	0	1	1
-4.5	1	0	1	0	0
-3.0	1	0	1	0	1
-1.5	1	0	1	1	0
0.0	1	0	1	1	1
1.5	1	1	0	0	0
3.0	1	1	0	0	1
4.5	1	1	0	1	0
6	1	1	0	1	1
7.5	1	1	1	0	0
9	1	1	1	0	1
10.5	1	1	1	1	0
12	1	1	1	1	1

SPI Timing Diagram



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Flip Chip Thermal Resistance Junction to Ambient [2]	?	°C/W
Pd	Power Dissipation	Internally Limited	
ESD	Human Body Model	2	kV
ESD	Machine Model	100	V
	Latch-up Immunity	Class A	
	Lead Temperature (soldering, 10sec)	250	°C

1. All voltages values are measured with respect to the ground pin.
2. Device is protected in case of over temperature by a thermal shutdown active @ 150°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	3 to 5.5	V
V_{phin}	Maximum Phone In Input Voltage	G_{ND} to V_{CC}	V
V_{Rin}/V_{Lin}	Maximum Rin & Lin Input Voltage	G_{ND} to V_{CC}	V

ELECTRICAL CHARACTERISTICS

V_{CC} = **+3.3V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current Output Mode 7, Vin = 0V, Io = 0A All other output modes, Vin = 0V, Io = 0A		7.5 4.5	10	mA
$I_{STANDBY}$	Standby Current Output Mode 0		0.1		µA
Voo	Output Offset Voltage (differential) Vin = 0V		10		mV
Vil	"Logic low" input Voltage	0		0.6	V
Vih	"Logic high" input Voltage	1.4	1.8		V
Po	Output Power SPKERout, RL = 8Ω, THD = 1%, f = 1kHz Rout & Lout, RL = 32Ω, THD = 0.5%, f = 1kHz	350 20	400 30		mW
THD + N	Total Harmonic Distortion + Noise Rout & Lout, Po = 20mW, f = 1kHz, RL = 32Ω SPKERout, Po = 350mW, f = 1kHz, RL = 8Ω Rout & Lout, Po = 20mW, 50Hz < f < 20kHz, RL = 32Ω SPKERout, Po = 350mW, 700Hz < f < 20kHz, RL = 8Ω		0.5 2	0.2 1	%
SNR	Signal To Noise Ratio A-Weighted, f = 1kHz		80		dB
PSRR	Power Supply Rejection Ratio [12dBx(R+L)+6dBxP] [1] Vripple=200mV Vpp, F = 217Hz, Input Floating Vripple=200mV Vpp, F = 217Hz, Input Terminated 50Ω		70 40		dB
K	Digital Volume Range - Rin & Lin minimum gain maximum gain		-34.5 +12		dB

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Digital volume stepsize		1.5		dB
	Stepsize K > -20dB K < -20dB		 ± 0.5 ± 0.6		dB
	Phone In Volume BTL gain from Phone In to SPKERout BTL gain from Phone In to Rout & Lout		 6 0		dB
Zin	Phone In Input Impedance	15	20	25	kΩ
Zin	Rin & Lin Input Impedance (all gain setting)	37.5	50	62.5	kΩ
tes	Enable Stepup Time - ENB	20			ns
teh	Enable Hold Time - ENB	20			ns
tel	Enable Low Time - ENB	30			ns
tds	Data Setup Time- DATA	20			ns
tdh	Data Hold Time - DATA	20			ns
tcs	Clock Setup time - CLK	20			ns
tch	Clock Logic High Time - CLK	50			ns
tcl	Clock Logic Low Time - CLK	50			ns
fclk	Clock Frequency - CLK	DC		10	MHz

1. Dynamic measurements [20xlog(rms(Vout)/rms(Vripple)]. Vripple is the surimposed sinus signal to Vcc @ F = 217Hz

ELECTRICAL CHARACTERISTICS

V_{CC} = **+3.0V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current Output Mode 7, Vin = 0V, Io = 0A All other output modes, Vin = 0V, Io = 0A		 7.5 4.5	 10	mA
$I_{STANDBY}$	Standby Current Output Mode 0		 0.1		µA
Voo	Output Offset Voltage (differential) Vin = 0V		 10		mV
Vil	”Logic low” input Voltage	0		0.6	V
Vih	”Logic high” input Voltage	1.4	1.8		V
Po	Output Power SPKERout, RL = 8Ω, THD = 1%, f = 1kHz Rout & Lout, RL = 32Ω, THD = 0.5%, f = 1kHz	 290 20	 330 30		mW
THD + N	Total Harmonic Distortion + Noise Rout & Lout, Po = 20mW, f = 1kHz, RL = 32Ω SPKERout, Po = 350mW, f = 1kHz, RL = 8Ω Rout & Lout, Po = 20mW, 50Hz < f < 20kHz, RL = 32Ω SPKERout, Po = 350mW, 700Hz < f < 20kHz, RL = 8Ω		 0.5 2	 0.2 1	%
SNR	Signal To Noise Ratio A-Weighted, f = 1kHz		 80		dB

Symbol	Parameter	Min.	Typ.	Max.	Unit
PSRR	Power Supply Rejection Ratio [12dBx(R+L)+6dBxP][1)] Vripple=200mV Vpp, F = 217Hz, Input Floating Vripple=200mV Vpp, F = 217Hz, Input Terminated 50Ω		 70 40		dB
K	Digital Volume Range - Rin & Lin minimum gain maximum gain		 -34.5 +12		dB
	Digital volume stepsize		1.5		dB
	Stepsize K > -20dB K < -20dB		 ± 0.5 ± 0.6		dB
	Phone In Volume BTL gain from Phone In to SPKERout BTL gain from Phone In to Rout & Lout		 6 0		dB
Zin	Phone In Input Impedance	15	20	25	kΩ
Zin	Rin & Lin Input Impedance (All Gain Setting)	37.5	50	62.5	kΩ
tes	Enable Stepup Time - ENB	20			ns
teh	Enable Hold Time - ENB	20			ns
tel	Enable Low Time - ENB	30			ns
tds	Data Setup Time- DATA	20			ns
tdh	Data Hold Time - DATA	20			ns
tcs	Clock Setup time - CLK	20			ns
tch	Clock Logic High Time - CLK	50			ns
tcl	Clock Logic Low Time - CLK	50			ns
fclk	Clock Frequency - CLK	DC		10	MHz

1. Dynamic measurements [20xlog(rms(Vout)/rms(Vripple)]. Vripple is the surimposed sinus signal to Vcc @ F = 217Hz

Fig. 1 : Speaker : Pout vs Supply Voltage @ THD + N = 1%

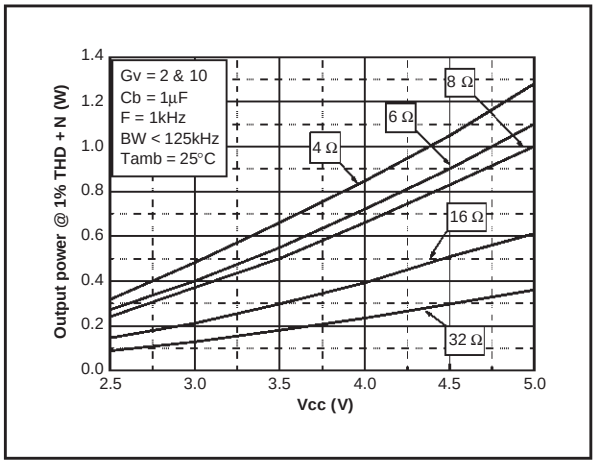


Fig. 2 : Rin or Lin to Rout or Lout : Pout vs Supply Voltage @ THD + N = 1%

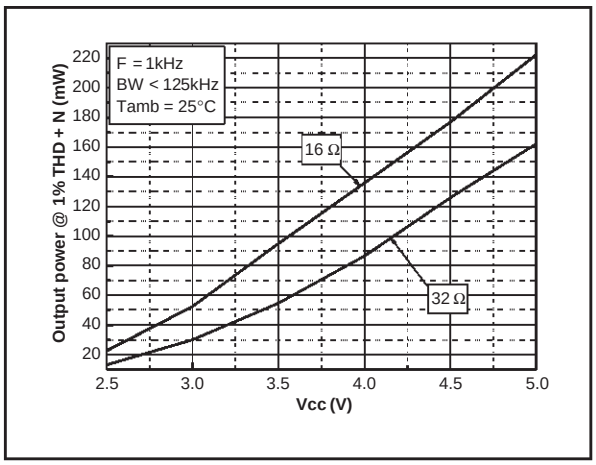


Fig. 3 : Phone in to Rout or Lout : Pout vs Supply Voltage @ THD + N = 1%

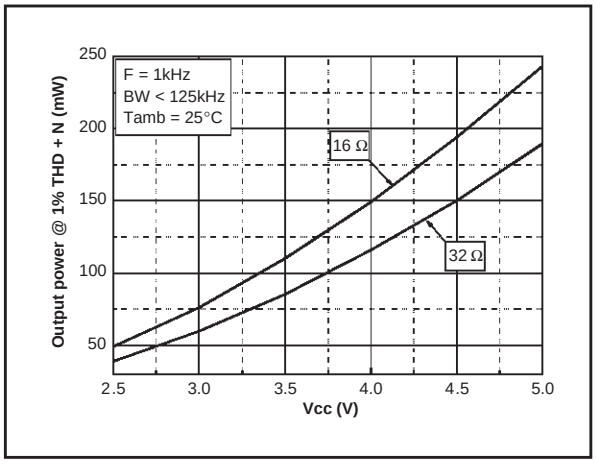


Fig. 4 : THD + N vs Output Power, Mode 1, 5, 7. Phone in to Speaker (+6dB)

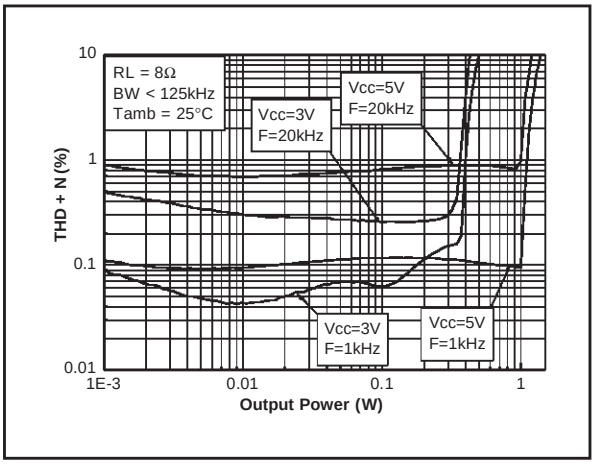


Fig. 5 : THD + N vs Output Power, Mode 2, 6, 7. Phone in to Rout or Lout (0dB)

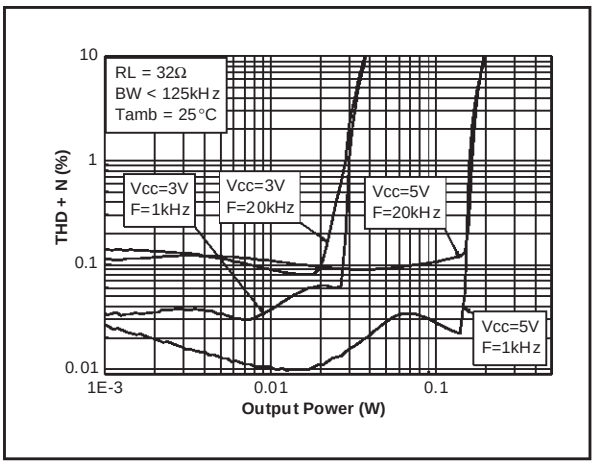


Fig. 6 : THD + N vs Output Power, Mode 4, 6, 7. Rin or Lin to Rout or Lout (k = +6dB)

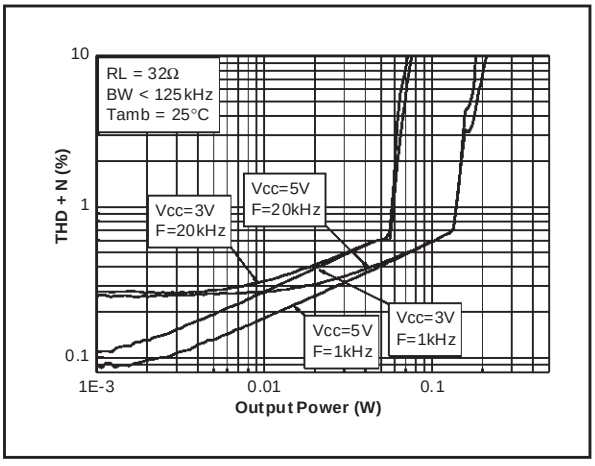


Fig. 7 : THD + N vs Output Power, Mode 3, 5. Rin or Lin to Speaker (k = +6dB)

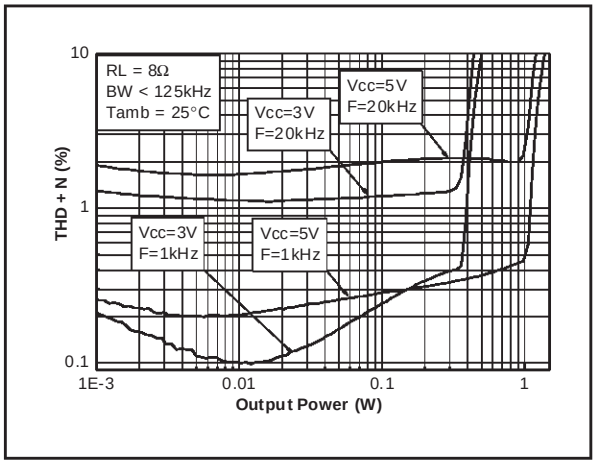


Fig. 8 : THD + N vs frequency, Mode 1, 5, 7. Phone in to Speaker (+6dB)

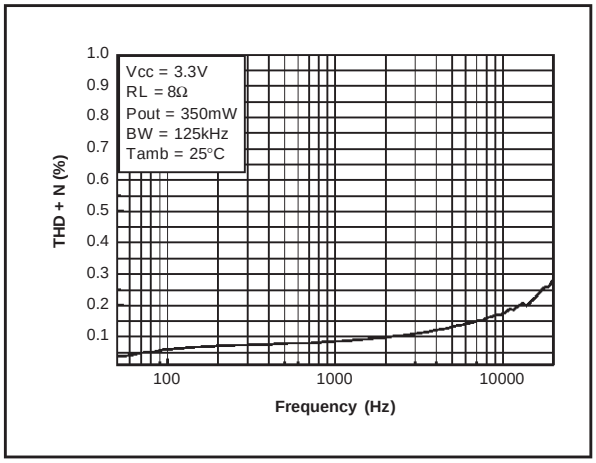


Fig. 9 : THD + N vs Frequency, Mode 2, 6, 7. Phone in to Rout or Lout (0dB)

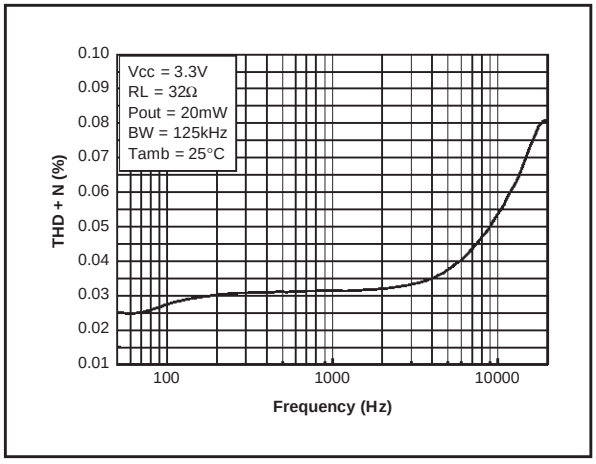


Fig. 10 : THD + N vs Frequency, Mode 4, 6, 7. Rin or Lin to Rout or Lout (k = +6dB)

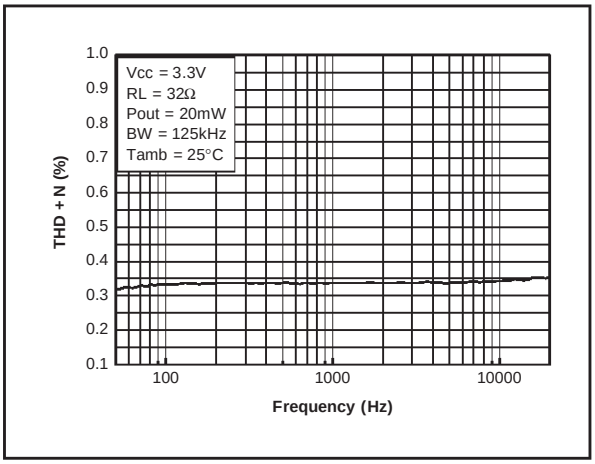


Fig. 11 : THD + N vs Frequency, Mode 3, 5. Rin or Lin to Speaker (k = +6dB)

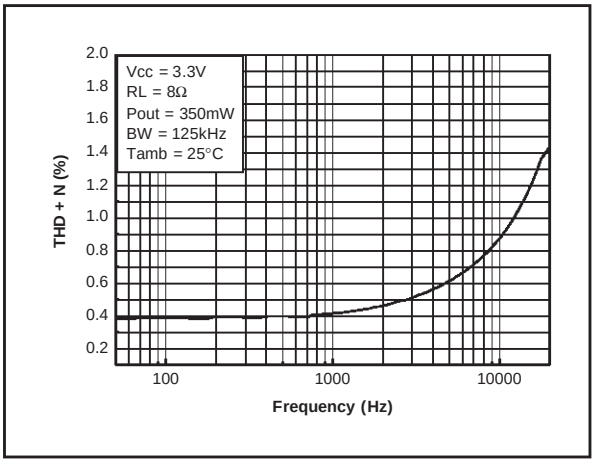


Fig. 12 : Signal to noise Ratio on Headset. Unweighted Filter, BW = 20Hz to 20kHz

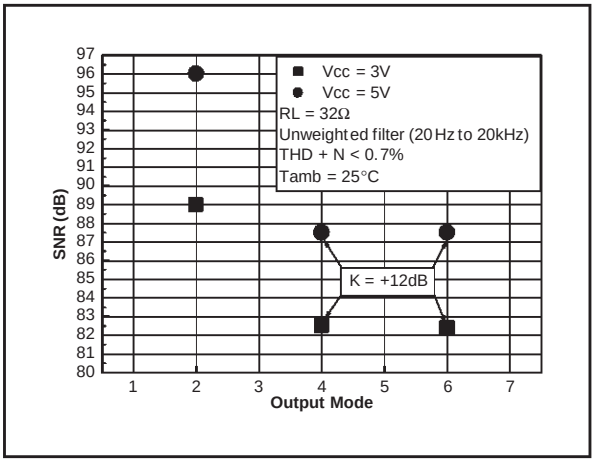


Fig. 13 : Signal to noise Ratio on Speaker. Unweighted Filter, BW = 20Hz to 20kHz

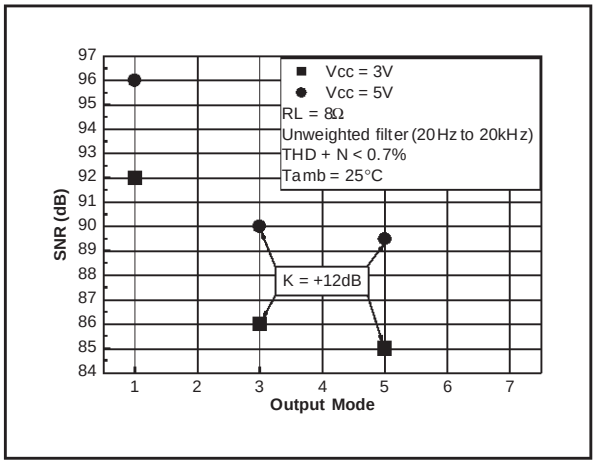


Fig. 14 : Signal to noise Ratio on Speaker. Weighted Filter type A, BW = 20Hz to 20kHz

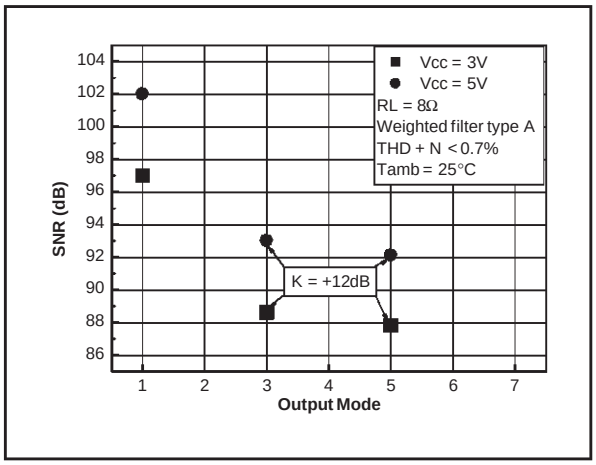


Fig. 15 : Current Consumption vs Power. Supply Voltage

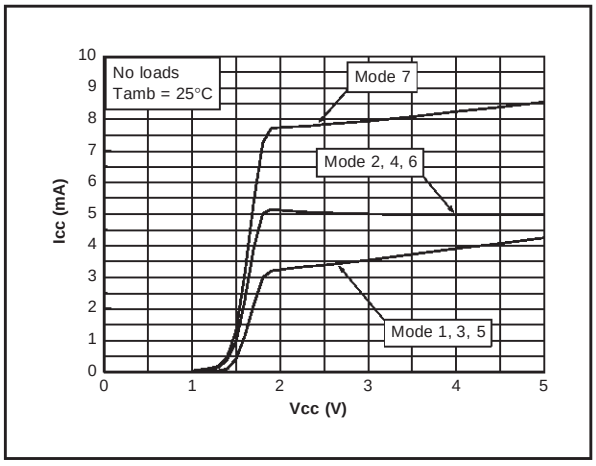
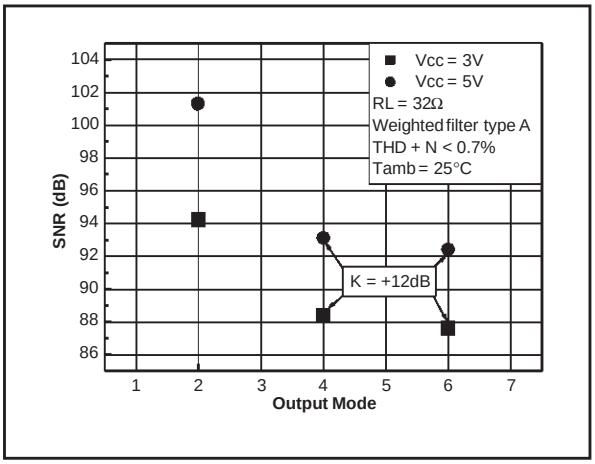


Fig. 16 : Signal to noise Ratio on Headset. Weighted Filter type A, BW = 20Hz to 20kHz



APPLICATION INFORMATION

■ BTL Configuration Principle

The TS4851 integrated 3 monolithic power amplifier with a BTL output type. BTL (Bridge Tied Load) means that each end of the load is connected to two single ended output amplifiers. Thus, we have :

Single ended output 1 = Vout1 = Vout (V)
Single ended output 2 = Vout2 = -Vout (V)

And Vout1 - Vout2 = 2Vout (V)

The output power is:

$$Pout = \frac{(2\,Vout_{RMS})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

■ Power dissipation and efficiency

Hypothesis :

- Voltage and current in the load are sinusoidal (Vout and Iout)
- Supply voltage is a pure DC source (Vcc)

Regarding the load we have:

$$V_{OUT} = V_{PEAK} \sin\omega t \ (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} \ (A)$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} \ (W)$$

Then, the average current delivered by the supply voltage is:

$$I_{CC\ AVG} = 2\frac{V_{PEAK}}{\pi R_L} \ (A)$$

The power delivered by the supply voltage is
Psupply = Vcc Icc_{AVG} (W)

Then, the **power dissipated by each amplifier** is
Pdiss = Psupply - Pout (W)

$$P_{diss} = \frac{2\sqrt{2}\,V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT} \quad (W)$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{OUT}} = 0$$

and its value is:

$$Pdissmax = \frac{2Vcc^2}{\pi^2 R_L} (W)$$

Remark : This maximum value is only depending on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{Psupply} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when Vpeak = Vcc, so

$$\frac{\pi}{4} = 78.5\%$$

The TS4851 has 3 independent power amplifiers. Each amplifier produces heat due to their power dissipate. The maximum temperature of the die is reach when it has the maximum of the sum power dissipation. So we have :

Pdiss Speaker = Power dissipation due to the speaker power amplifier.
Pdiss Head = Power dissipation due to the Headphone power amplifier

Total Pdiss = Pdiss Speaker + Pdiss Head1 + Pdiss Head2 (W)

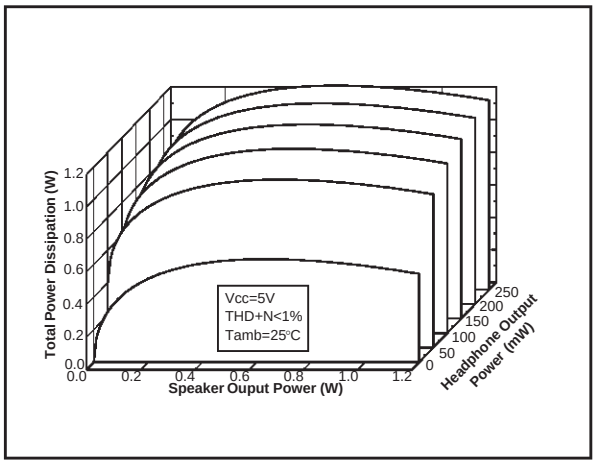
In many cases, Pdiss Head1 = Pdiss Head 2 so,

Total Pdiss = Pdiss Speaker + 2xPdiss Head (W)

$$Total P_{diss} = \frac{2\sqrt{2}\,V_{CC}}{\pi}\left[\sqrt{\frac{P_{OUT\ SPEAKER}}{R_{L\ SPEAKER}}} + 2\sqrt{\frac{P_{OUT\ HEAD}}{R_{L\ HEAD}}}\right] - [P_{OUT\ SPEAKER} + 2P_{OUT\ HEAD}] \quad (W)$$

The following picture shows an example, of the previous formula, with Vcc=+5V, Rload speaker=8Ω et Rload Headphone=16Ω.

Fig. 17 : Example of Total Power Dissipation vs Speaker and Headphone Output Power



■ Low frequency response

In low frequency region, the effect of Cin starts. Cin with Zin forms a high pass filter with a -3dB cut off frequency.

$$F_{CL} = \frac{1}{2 \pi Zin\ Cin} (Hz)$$

Zin, is the input impedance of the corresponding input :
20kΩ for Phone In input
50kΩ for Rin and Lin inputs

Note : For all inputs, the impedance value remains constant for all gain setting. It means that the lower cut-off frequency doesn't change with gain setting. Note also that 20kΩ and 50kΩ are typical value and there are tolerances around these values (see electrical characteristics).

■ Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4851, a power supply bypass capacitor Cs and a bias voltage bypass capacitor Cb.

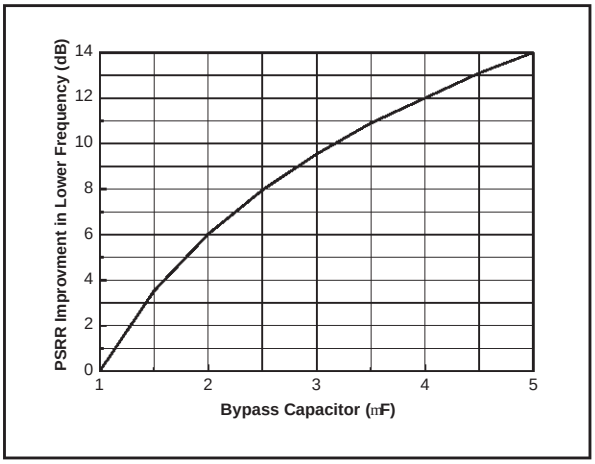
Cs has especially an influence on the THD+N in high frequency (above 7kHz) and indirectly on the power supply disturbances.
With 1µF, you could expect similar THD+N performances like shown in the datasheet.

If Cs is lower than 1µF, THD+N increases in high frequency and disturbances on the power supply rail are less filtered.
To the contrary, if Cs is higher than 1µF, those disturbances on the power supply rail are more filtered.

Cb has an influence on THD+N in lower frequency, but its value is critical on the final result of PSRR with input grounded in lower frequency.

If Cb is lower than 1µF, THD+N increase in lower frequency and the PSRR worsens up
If Cb is higher than 1µF, the benefit on THD+N in lower frequency is small but the benefit on PSRR (≤ 100Hz) could be estimated by the following graph :

Fig. 18 : PSSR Improvment in Lower Frequency (≤ 100Hz) vs Bypass Capacitor



Note that this is a theorical improvment. In the TS4881, we need to take in account of the noise floor.

Startup time

When the TS4851 is controled to switch from the full standby mode (ouput mode 0) to another output mode, a delay is necessary to stabilize the DC bias. This delay depends on the Cb value and could be calculated by the following formulas.

- Typical startup time = 0.0175xCb (s)
- Max startup time = 0.025xCb (s)
  (Cb is in µF in these formulas)

These formulas assume that the Cb voltage is equal to 0V. If the Cb voltage is not equal to 0V, the startup time will be always lower.
The startup time is the delay between the negative

edge of Enable input (see SPI description) and the power ON of the output amplifiers.

Note : When the TS4851 is set in full standy mode, Cb is discharged through an internal resistor. The time to reach 0V of Cb voltage could be calculated by the following formula :

- Tdischarge=3xCb (s)
  Cb must be in µF in this formula

■ Pop and Click performance

The TS4851 has an internal Pop and Click reduction circuitry. The performance is intimately linked with the value of the input capacitor Cin and the bias voltage bypass capacitor Cb.

Value of Cin is due to the lower cut-off frequency value requested. value of Cb is due to THD+N and PSRR requested always in lower frequency.

TS4851 is optimised to have a low pop and click in the typical schematic configuration (page 2).

Note : Cs is not important in pop and click consideration.

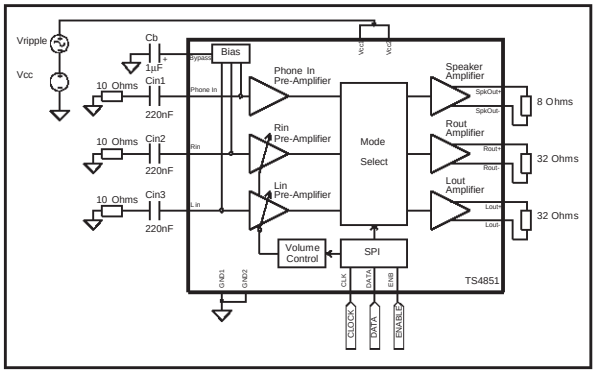
■ Note on PSRR measurement

What is the PSRR ?

The PSRR is the Power Supply Rejection Ratio. It's a kind of SVR in a determined frequency range. The PSRR of a device, is the ratio between a power supply disturbance and the result on the output. We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.

How we measure the PSRR ?

Fig. 19 : PSRR measurement schematic



Principle of operation

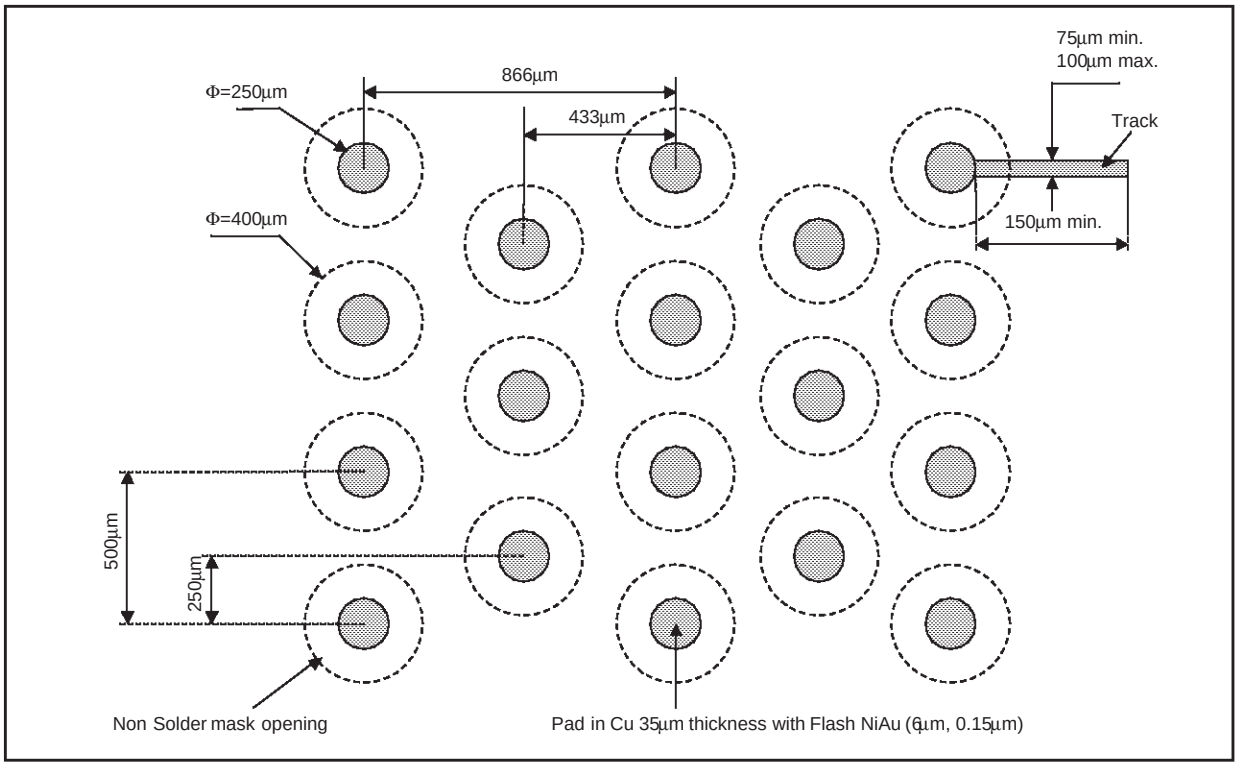
- We fixed the DC voltage supply (Vcc)
- We fixed the AC sinusoidal ripple voltage (Vripple)
- No bypass capacitor Cs is used

The PSRR value for each frequency is:

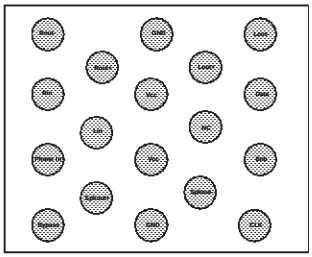
$$PSRR = 20 \times Log\left[\frac{RMS_{(Output)}}{RMS_{(Vripple)}}\right] \quad (dB)$$

Remark : The measure of the Rms voltage is not a Rms selective measure but a full range (2 Hz to 125 kHz) Rms measure. It means that we measure the effective Rms signal + the noise.

Fig. 20 : TS4851 Footprint Recommendation



PIN OUT (top view)

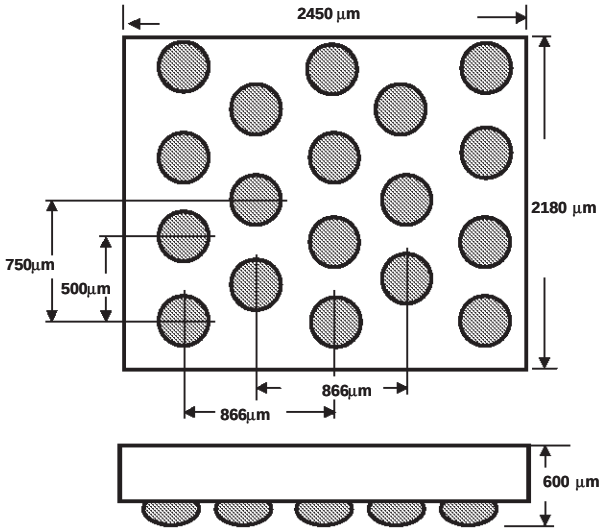


■ Balls are underneath

MARKING (top view)

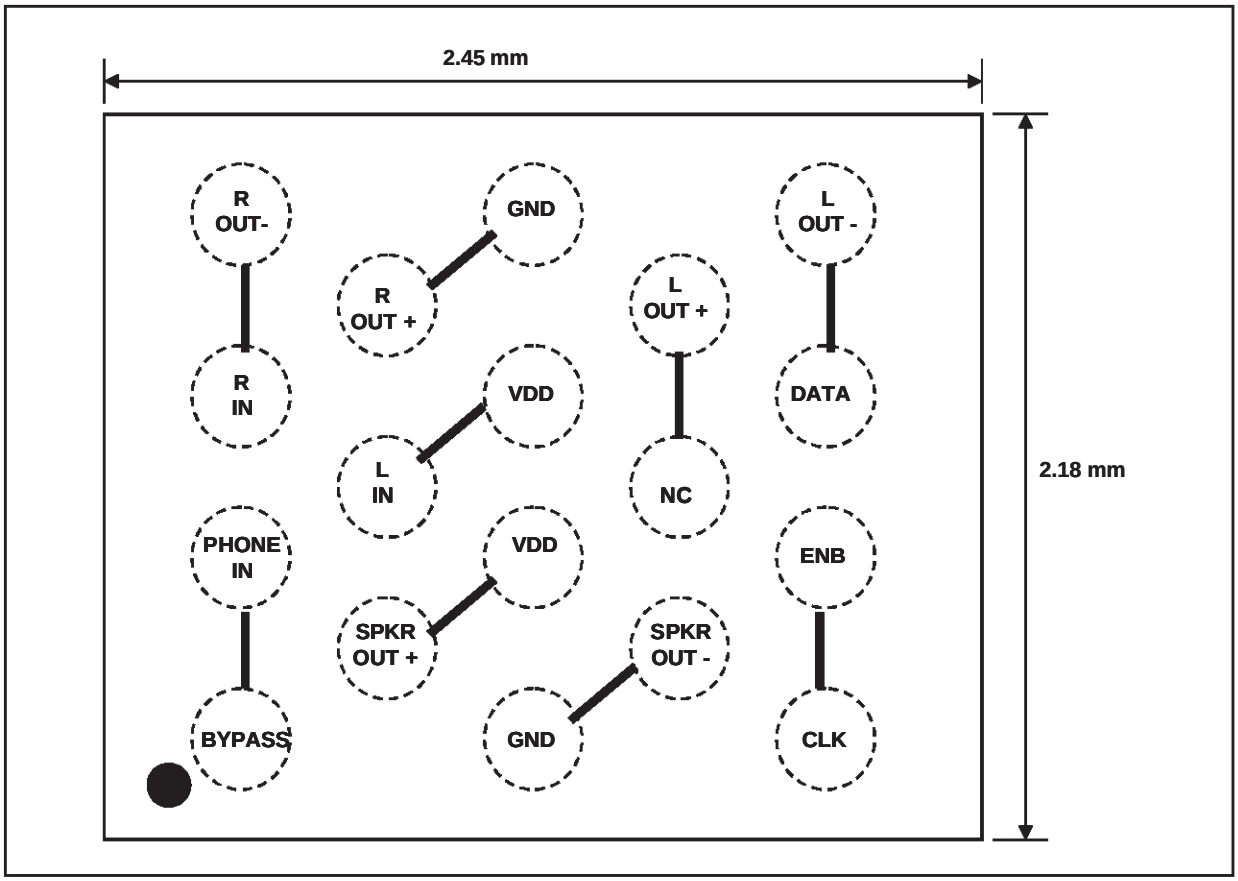
■ ST logo
■ Part Number : A51
■ Three digits Datecode : YWW
■ The dot is for marking the Pin1A

PACKAGE MECHANICAL DATA



■ Die size : ***2180µm x 2450µm***
■ Die height (including bumps) : ***600µm ±30µm***
■ Bumps diameter : 300µm ±15µm
■ Bumps height : 250µm ±15µm
■ Pitch: 500µm ±10µm

DAISY CHAIN MECHANICAL DATA (all drawings dimensions are in millmeters)



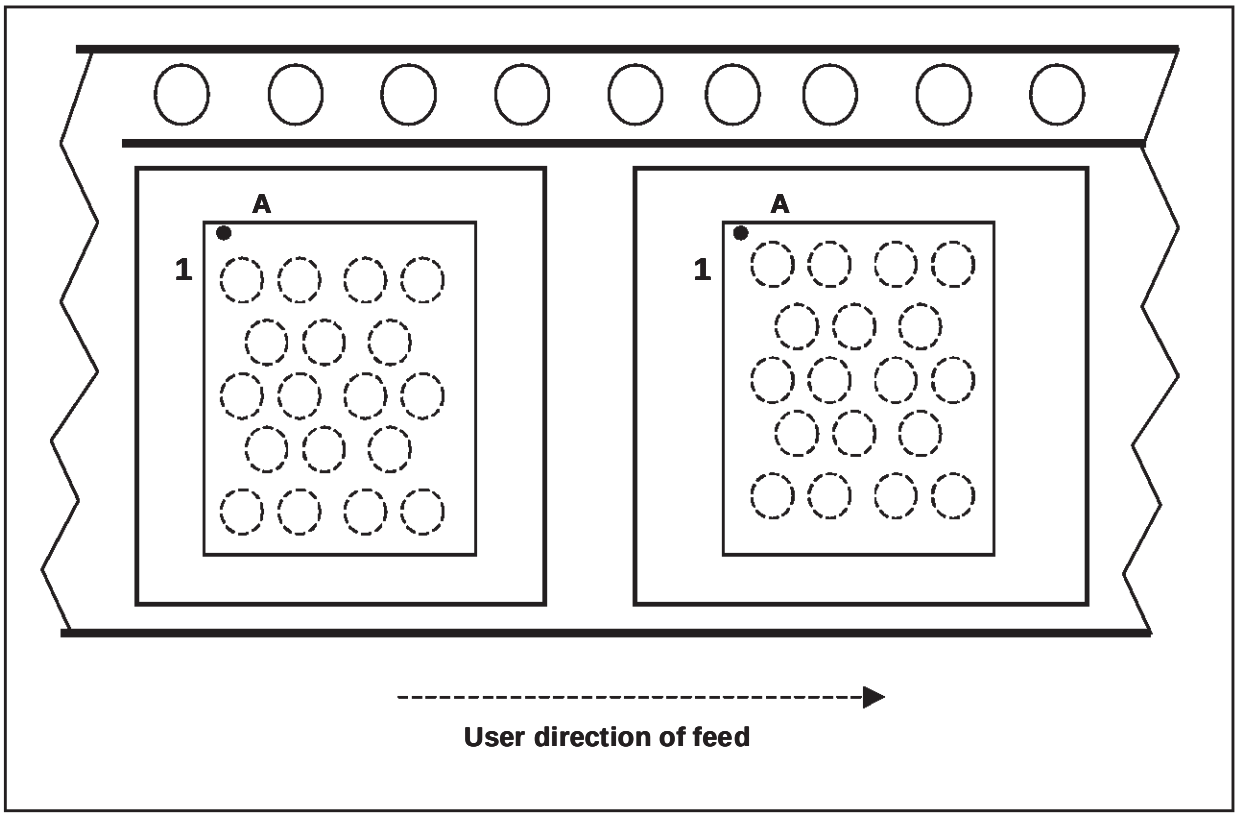
REMARKS

Daisy chain sample is featuring pin connection two by two. The schematic above is illustrating the way connecting pins each others. This sample is used for testing continuity on board. PCB needs to be designed on the opposite way, where pin connections are not done on daisy chain samples. By that way, just connecting a Ohmeter between pin 1A and pin 5A, the soldering process continuity can be tested.

ORDER CODE

Part Number	Temperature Range	Package	Marking
		J	
TSDC02IJT	-40, +85°C	•	DC02

TAPE & REEL SPECIFICATION (top view)



DEVICES ORIENTATION

The devices are oriented in the carrier pocket with pin number 1A adjacent to the sprocket holes.