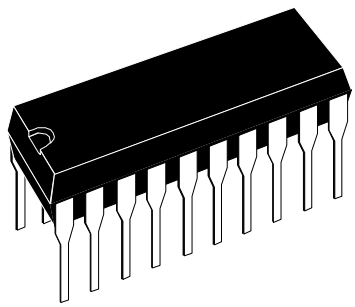
STV9382

OPTIMWATT™ Class-D Vertical Deflection Amplifier for 1.5 Amp TV Applications

Main Features

- **High-Efficiency OPTIMWATT™ Power Amplifier**
- **No Heatsink**
- **Split Supply**
- **Internal Flyback Generator**
- **Output Current up to 1.5 A_{PP}**
- **Suitable for DC Coupling Applications**
- **Few External Components**
- **Protection against Low V_{CC}**



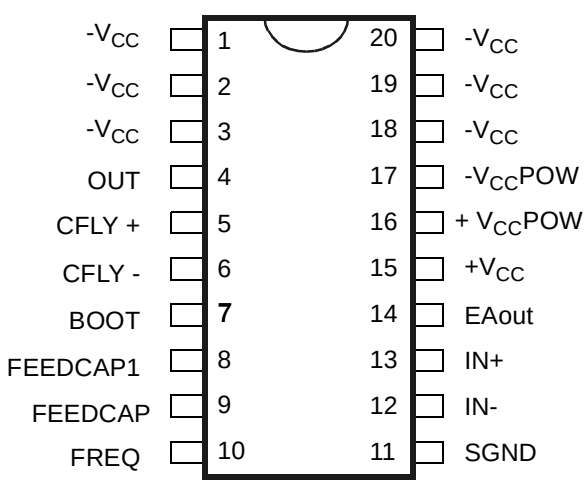
PDIP 20
Order Code: STV9382

Description

Designed for TV applications, the OPTIMWATT™ STV9382 is a Class-D vertical deflection booster assembled in a 20-pin plastic DIP package.

It belongs to the OPTIMWATT™ Class-D vertical deflection booster family.

It operates with supplies up to ±18 V and provides an output current up to 1.5 A_{PP} to drive the yoke. The internal flyback generator avoids the need for an extra power supply.



1 Pin Functions

Table 1: STV9382 Pin Descriptions

Pin	Name	Function	Pin	Name	Function
1	$-V_{CC}$	Negative Supply	11	SGND	Signal Ground
2	$-V_{CC}$	Negative Supply	12	IN-	Error Amplifier Inverting Input
3	$-V_{CC}$	Negative Supply	13	IN+	Error Amplifier Non-inverting Input
4	OUT	PWM Output	14	EA out	Error Amplifier Output
5	CFLY+	Flyback Capacitor	15	$+V_{CC}$	Positive Supply
6	CFLY-	Flyback Capacitor	16	$+V_{CC}$POW	Positive Power Supply
7	BOOT	Bootstrap Capacitor	17	-VccPOW	Negative Power Supply
8	FEEDCAP1	Feed-back Integrating Capacitor	18	$-V_{CC}$	Negative Supply
9	FEEDCAP	Feed-back Integrating Capacitor	19	$-V_{CC}$	Negative Supply
10	FREQ	Frequency Setting Capacitor	20	$-V_{CC}$	Negative Supply

2 Functional Description

The STV9382 is a vertical deflection circuit operating in Class D. Class D is a modulation method where the output transistors work in switching mode at high frequency. The output signal is restored by filtering the output square wave with an external LC filter. The major interest of this IC is the comparatively low power dissipation in regards to traditional amplifiers operating in class AB, eliminating the need of an heatsink.

Except for the output stage which uses Class D modulation, the circuit operation is similar to the one of a traditional linear vertical amplifier.

A (sawtooth) reference signal has to be applied to the circuit which can accept a differential or single ended signal. This sawtooth is amplified and applied as a current to the deflection yoke. This current is measured by means of a low value resistor. The resulting voltage is used as a feedback signal to guarantee the conformity of the yoke current with the reference input signal.

The overvoltage necessary for a fast retrace is obtained with a chemical capacitor charged at the power supply voltage of the circuit. At the flyback moment, this capacitor is connected in series with the output stage power supply. This method, used for several years with the linear vertical boosters and called “internal flyback” or “flyback generator”, avoids the need of an additional power supply, while reducing the flyback duration.

The circuit uses a BCD process that combines Bipolar, CMOS and DMOS devices. The output stage is composed of low-R_{ON} N-channel DMOS transistors.

Figure 1: Test and Application Circuit Diagram

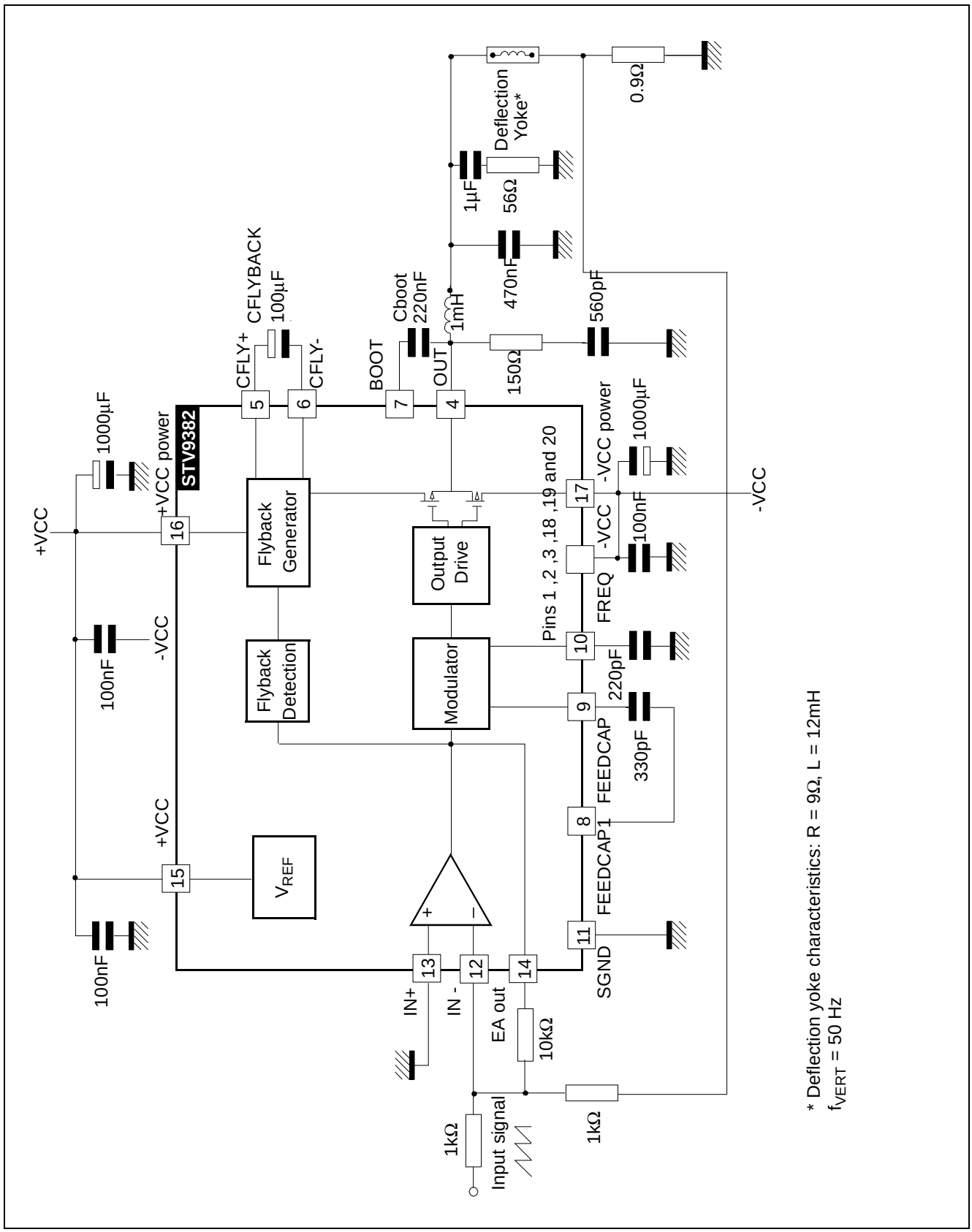
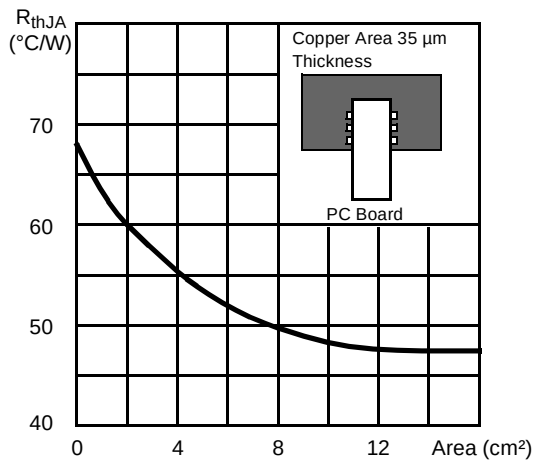


Figure 2: Thermal Resistance with "On-board" Square Heatsink vs. Copper Area



3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	±20	V
T_{STG}, T_J	Storage and Junction Temperature	-40 to +150	°C
T_{OP}	Operating Temperature Range	0 to +70	°C
V_{ESD}	ESD Susceptibility - Human Body Model (100 pF discharge through 1.5 kΩ) (see Note 1)	±2	kV
I_{OUT}	Output current	±1	A
V_{OUT}	Maximum output voltage (pin 4) with respect to -Vcc (pins 1, 2, 3, 18, 19 and 20) and during flyback (see Note 2)	80	V

Note: 1 Except pin 6 (+1.4kV/-2kV)

2 During the flyback with V_{CC} = ±18 V, the maximum output voltage (pin 4) is close to 72 V, with respect to -V_{CC} (pins 1, 2, 3, 18, 19 and 20).

4 Thermal Data

Symbol	Parameter	Value	Unit
R_{thJA}	Junction-to-Ambient Thermal Resistance	70	°C/W

Pins 1, 2, 3, 18, 19 and 20 are internally connected together and participate in heat evacuation.

5 Electrical Characteristics

T_{AMB} = 25° C, V_{CC} = ±12 V and f_{VERT} = 50 Hz unless otherwise specified (refer to Figure 1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$+V_{CC}$	Positive Supply Range		+10		+18	V
$-V_{CC}$	Negative Supply Range		-18		-10	V
ΔV_{CC}	Maximum recommended difference between $+V_{CC}$ and $\|-V_{CC}\|$				±4	V
$V_{CCSTART}$	Low V_{CC} Detection			±6.5		V
I_Q	Quiescent Supply Current	Input Voltage = 0		8.5		mA
I_Y	Maximum Vertical Yoke Current				±0.75	A
I_{13}, I_{12}	Amplifier Input Bias Current			-0.1		µA
V_{OS}	Output Offset Voltage	Note 1	-50		+50	mV
SVR	Supply Voltage Rejection	Note 2		70		dB
Fly_{THR}	Flyback Detection Threshold (Positive Slope)	V(14)		1.5		V
Fly_{THF}	Flyback Detection Threshold (Negative Slope)	V(14)		0.5		V
P_D	Integrated Circuit Dissipated Power	Note 3		0.6		W
f_{SW}	Switching Frequency	C_{FREQ} = 220 pF	120	155	200	kHz
f_{SW-OP}	Switching Frequency Operative Range		100		220	kHz
C_{FREQ}	Frequency Controller Capacitor Range	Pin 10	180	220	240	pF

Note: 1 Input voltage = 0, measured after the filter (e.g. across the 470 nF filter capacitor)

2 Supply rejection of the positive or negative power supply. V_{CC} ripple =1 V_{PP} and f =100 Hz, measured on the sense resistor.

3 Power dissipated in the circuit in the case of the application from Figure 1 *and the current in the deflection yoke adjusted to 1.5 A_{PP}. The corresponding power dissipated in the vertical deflection yoke is 1.7 W.*

6 I/O Waveforms

The following waveforms are obtained with the schematic diagram given in Figure 1: Test and Application Circuit Diagram:

Figure 3: Current in the Deflection Yoke (Calibration: 0.5 A/div.)

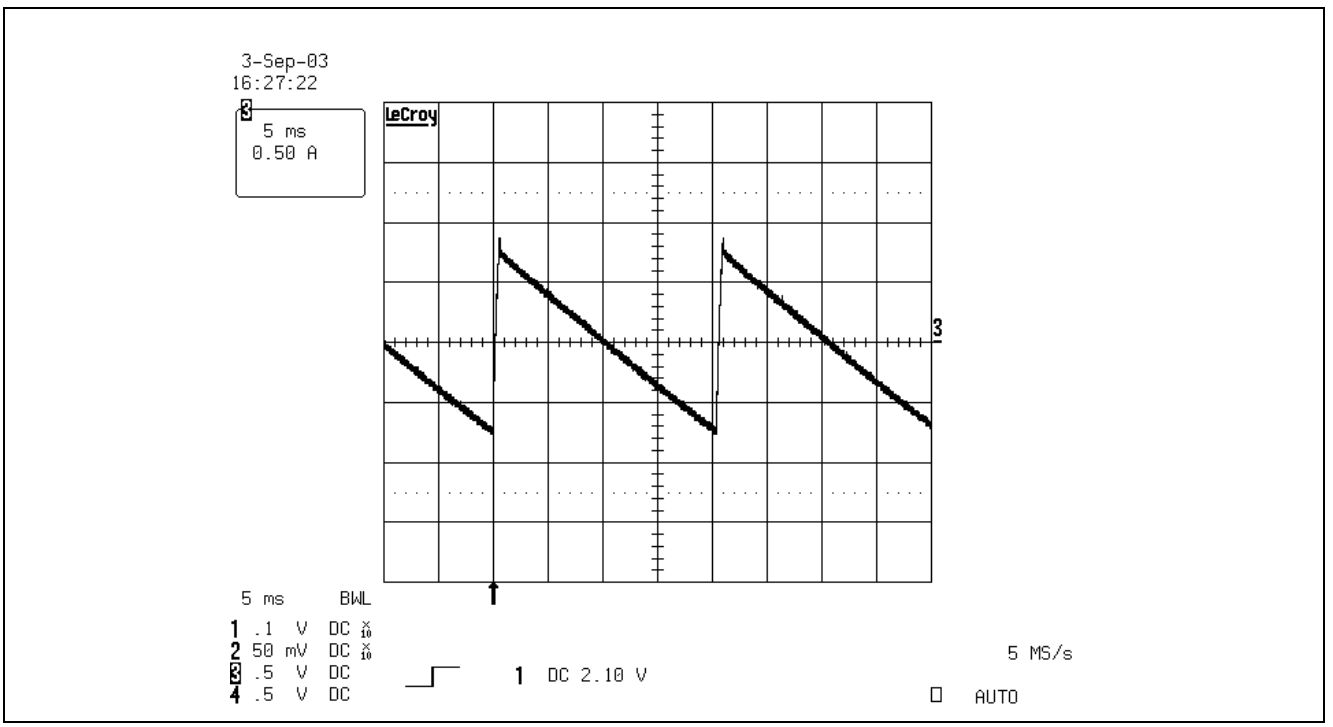


Figure 4: Current and Voltage in the Deflection Yoke during Flyback (Calibration: 0.5A/div, 10 V/div)

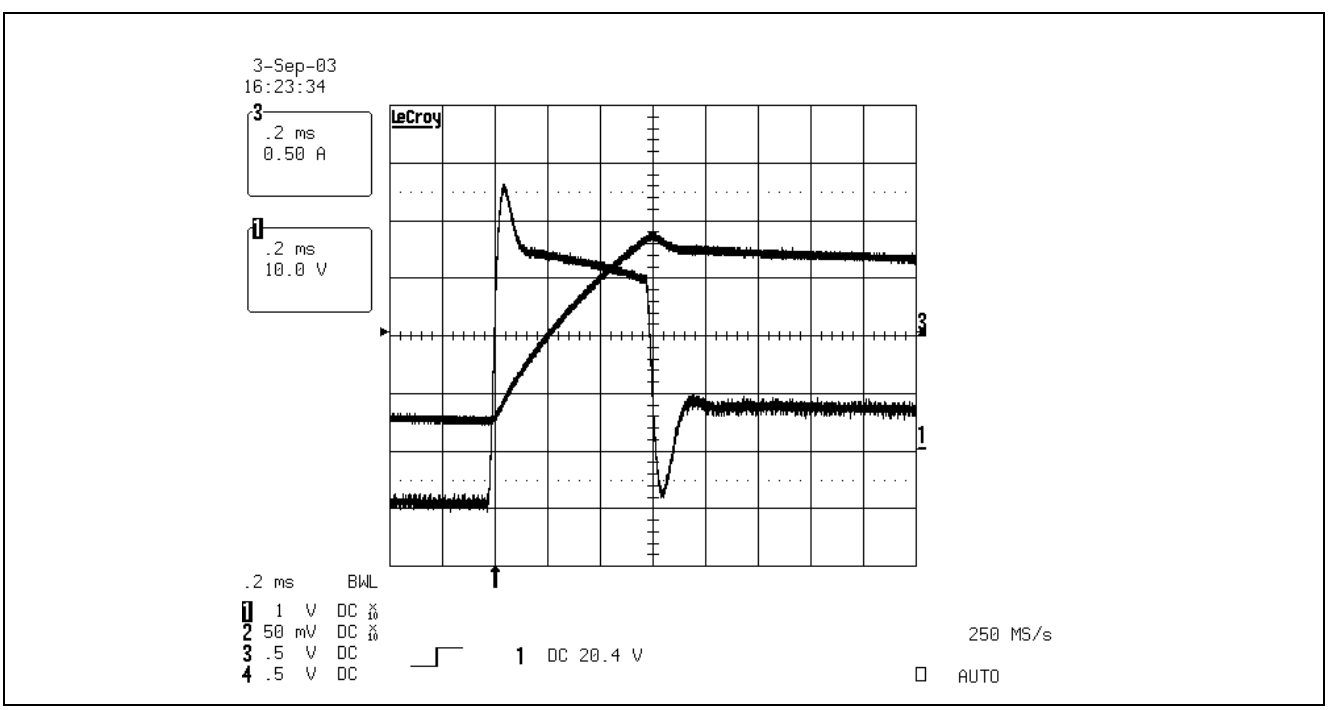


Figure 5: Current in the Deflection Yoke and Voltage at the Error Amplifier Output (pin 14 - STV9382) during Flyback (Calibration: 0.5 A/div, 1 V/div)

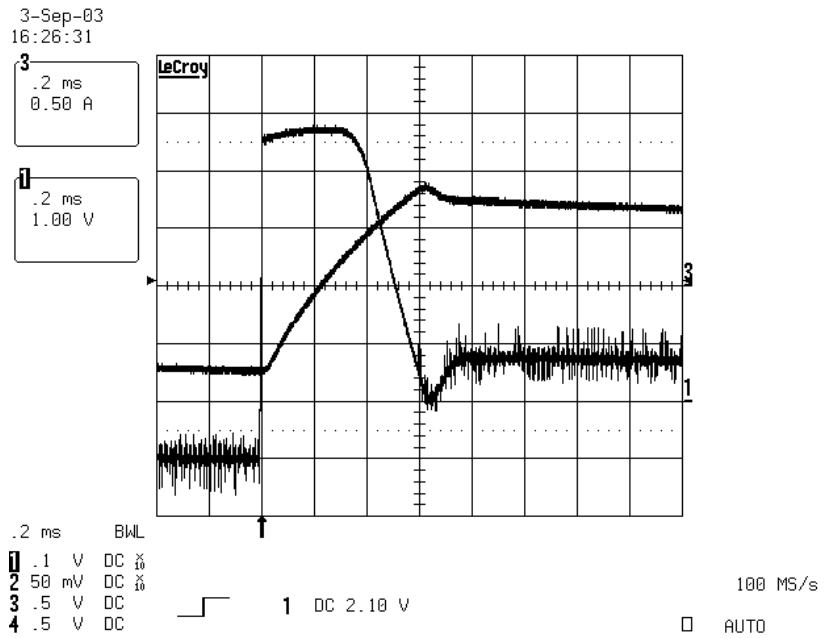
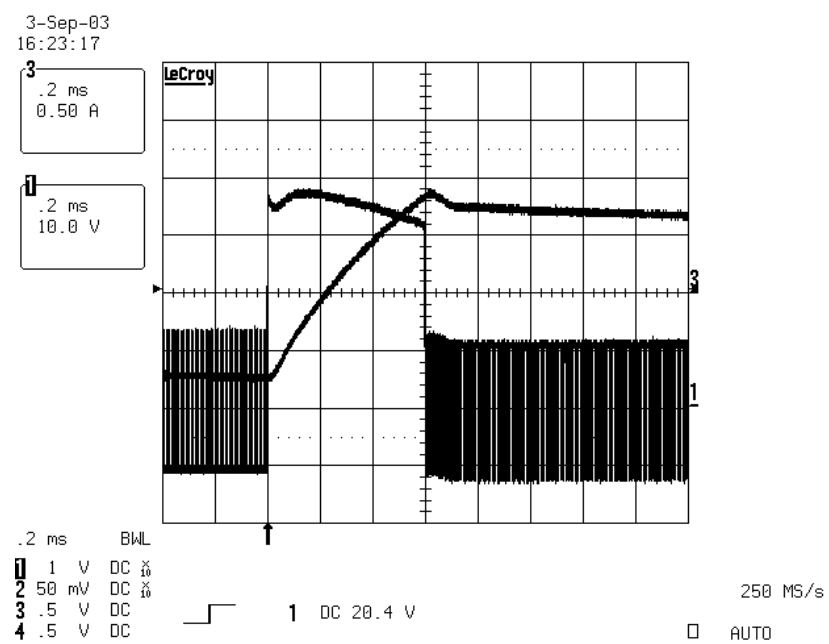


Figure 6: Current in the Deflection Yoke and Voltage at the Output of the STV9382 (pin 4), during the Flyback (Calibration: 0.5 A/div, 10 V/div)



7 Package Mechanical Data

Figure 7: 20-Pin Plastic Dual In-Line Package, 300-mil Width

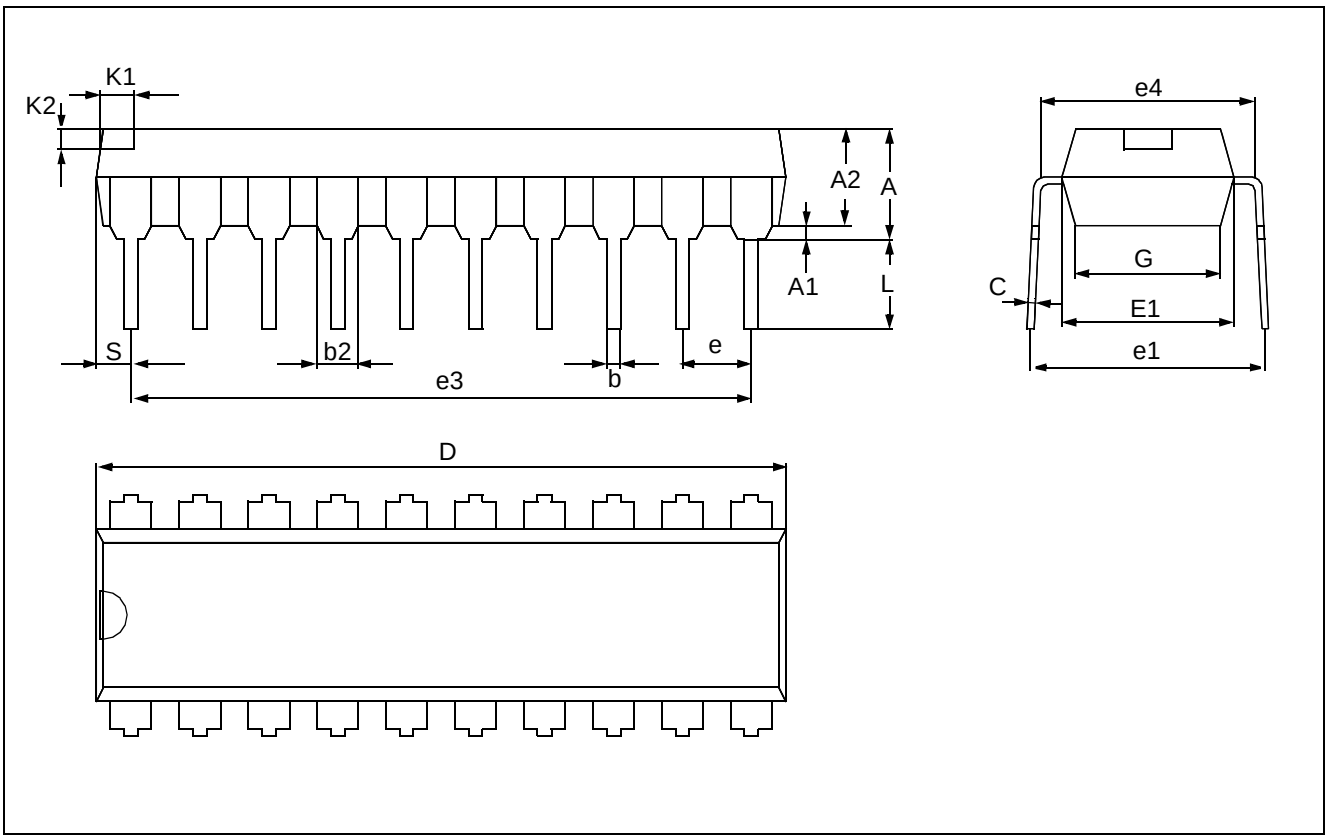
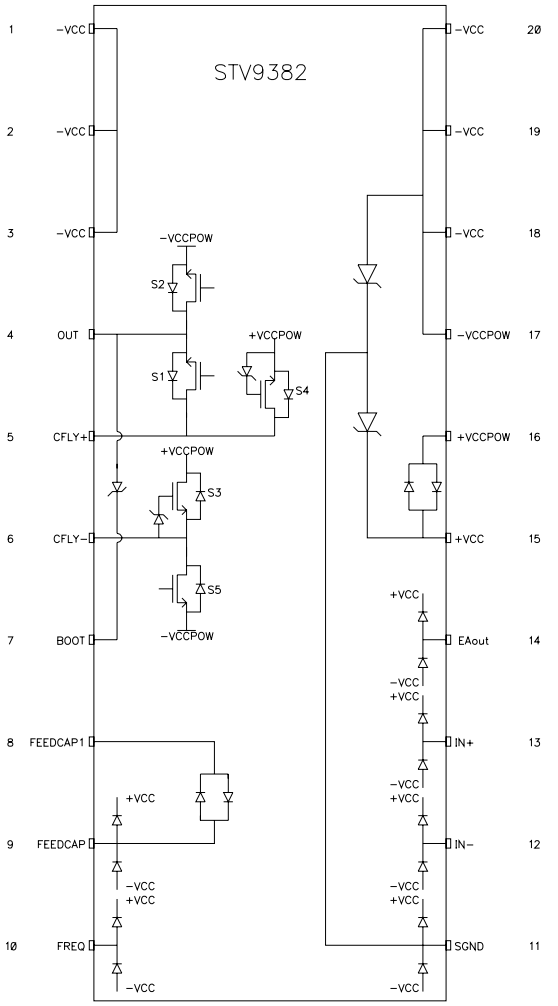


Table 2: DIP20 Package

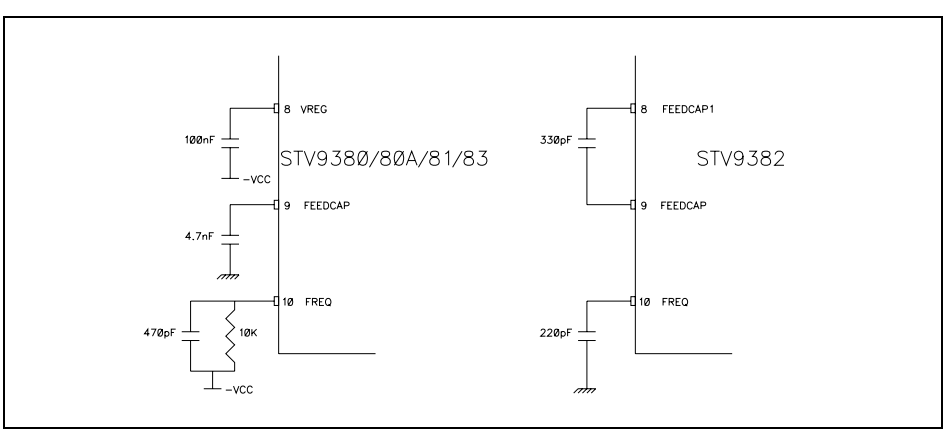
Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	24.89		26.92	0.980		1.060
e		2.54			0.100	
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150
	Number of Pins					
N	20					

Figure 8: ESD Protection Structure



7.1 Change Required on Application Between STV9380/80A/81/83 and STV9382

The STV9380/80A/81/83 and STV9382 are nearly pin to pin compatible except with regards to pins 8,9 and 10. The following application schematic shows the differences:



8 Revision History

Table 3: Summary of Modifications

Version	Date	Description
1.0	May 2002	First Issue.
1.1	14 October 2002	Modification of Figure 1: Test and Application Circuit Diagram and Section 7: Package Mechanical Data.
1.2	23 September 2003	Updated Chapter 5: Electrical Characteristics on page 5. Inclusion of Chapter 6: I/O Waveforms on page 6, Figure 8: ESD Protection Structure on page 9 and Section 7.1: Change Required on Application Between STV9380/80A/81/83 and STV9382 on page 9
1.3	October 2003	Included OPTIMWATT™ information. Added Note 1 on page 4.
1.4	June 2004	Removed all references to Monitors. Removed references to ST Confidential.

OPTIMWATT™ is a ST deposited trademark for product features allowing optimization of power efficiency at chip/application level