STD8NS25

N-CHANNEL 250V - 0.38Ω - 8A DPAK MESH OVERLAY™ MOSFET

PRELIMINARY DATA

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD8NS25	250 V	< 0.45 Ω	8 A

- TYPICAL $R_{DS}(on)$ = 0.38 Ω
- EXTREMELYN HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED

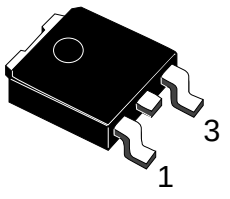
DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performance. The new patented STrip layout coupled with the Company's proprietary edge termination structure, makes it suitable in coverters for lighting applications.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITH MODE POWER SUPPLIES (SMPS)
- DC-DC CONVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT

Figure 1: Package



DPAK

Figure 2: Internal Schematic Diagram

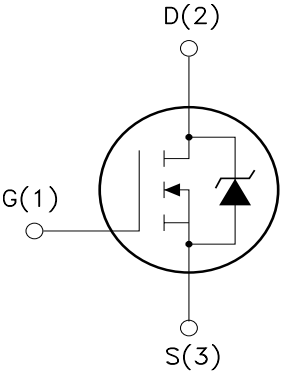


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD8NS25T4	D8NS25	DPAK	TAPE & REEL

Rev. 4

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	250	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	250	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuos) at T_C = 25°C	8	A
I_D	Drain Current (continuos) at T_C = 100°C	5	A
I_{DM} (•)	Drain Current (pulsed)	32	A
P_{TOT}	Total Dissipation at T_C = 25°C	80	W
	Derating Factor	0.64	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	5	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	209	mJ
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area
(1) $I_{SD} \leq$ 8A, di/dt≤300 A/µs, $V_{DD} \leq V_{(BR)DSS}$, Tj≤T_{jMAX}
(2) Starting T_j = 25°C, I_{AR} = 50A, V_{DD}=20 V

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	1.56	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	8	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	300	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 6: Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	250			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$, $I_D = 4$ A		0.38	0.45	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 4A$	7	8		S
C_{iss}	Input Capacitance	$V_{DS} = 25V$, f = 1 MHz, $V_{GS} = 0$		770		pF
C_{oss}	Output Capacitance			118		pF
C_{rss}	Reverse Transfer Capacitance			48		pF

Table 9: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 125$ V, $I_D = 4$ A		13		ns
t_r	Rise Time	$R_G = 4.7\Omega$ $V_{GS} = 10$ V (see test circuit, Figure 3)		18		ns
Q_g	Total Gate Charge	$V_{DD} = 200V$, $I_D = 8$ A, $V_{GS} = 10V$ (see Figure 7)		37	50	nC
Q_{gs}	Gate-Source Charge			5.2		nC
Q_{gd}	Gate-Drain Charge			14.8		nC

Table 10: Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(Voff)}$	Turn-off- Delay Time	$V_{DD} = 125V$, $I_D = 4$ A,		51		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 4)		16		ns
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{clamp} = 200V$, $I_D = 8$ A,		12.5		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10V$		12.5		ns
t_c	Cross-over Time	(see Figure 4)		28		ns

Table 11: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				8	A
I_{SDM} (2)	Source-drain Current (pulsed)				32	A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 8$ A, $V_{GS} = 0$			1.7	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 8$ A, di/dt = 100A/µs		198		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 30V$, $T_j = 150°C$ (see Figure 5)		1.1		µC
I_{RRM}	Reverse Recovery Current			11.3		A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.

Figure 3: Unclamped Inductive Load Test Circuit

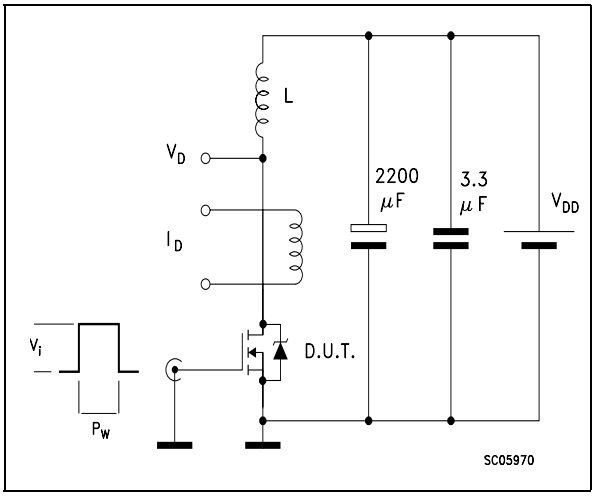


Figure 4: Switching Times Test Circuit For Resistive Load

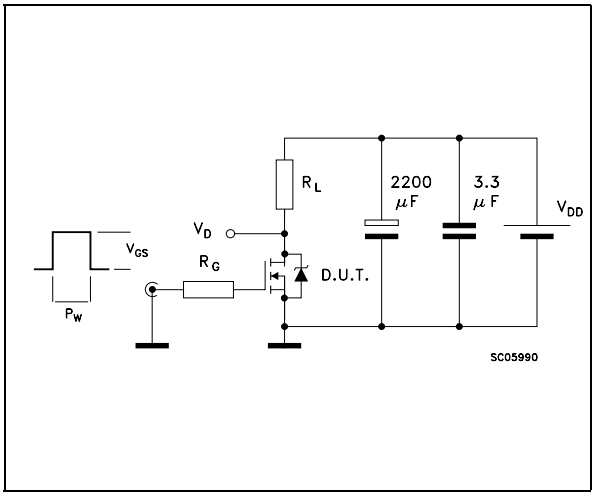


Figure 5: Test Circuit For Inductive Load Switching and Diode Recovery Times

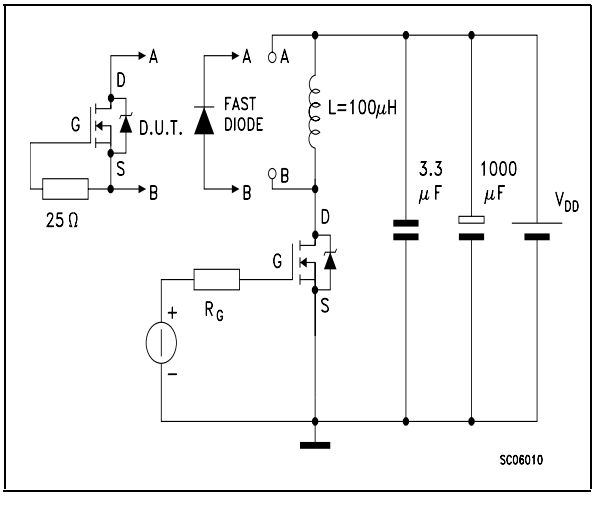


Figure 6: Unclamped Inductive Wafeform

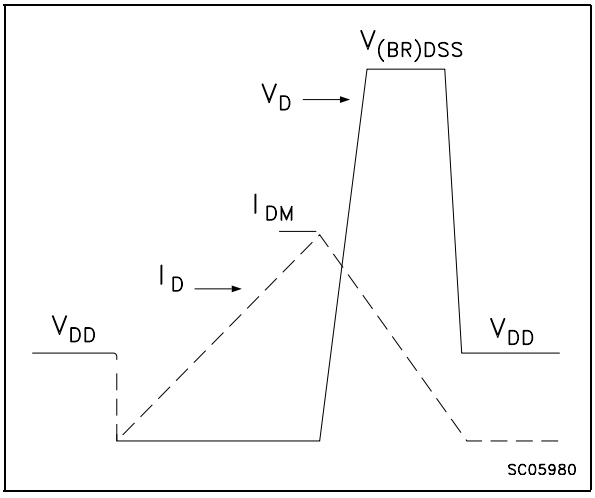
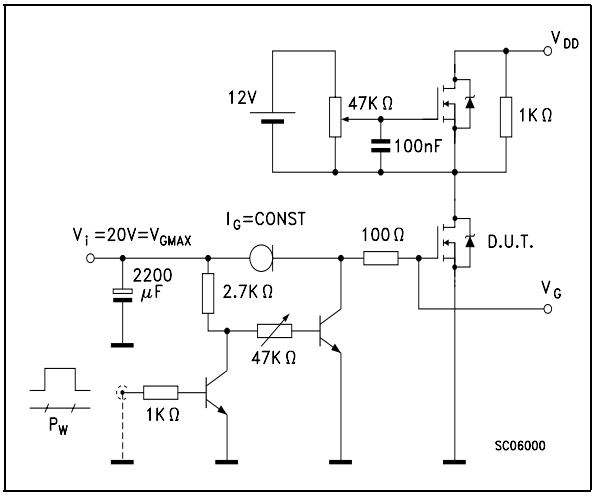
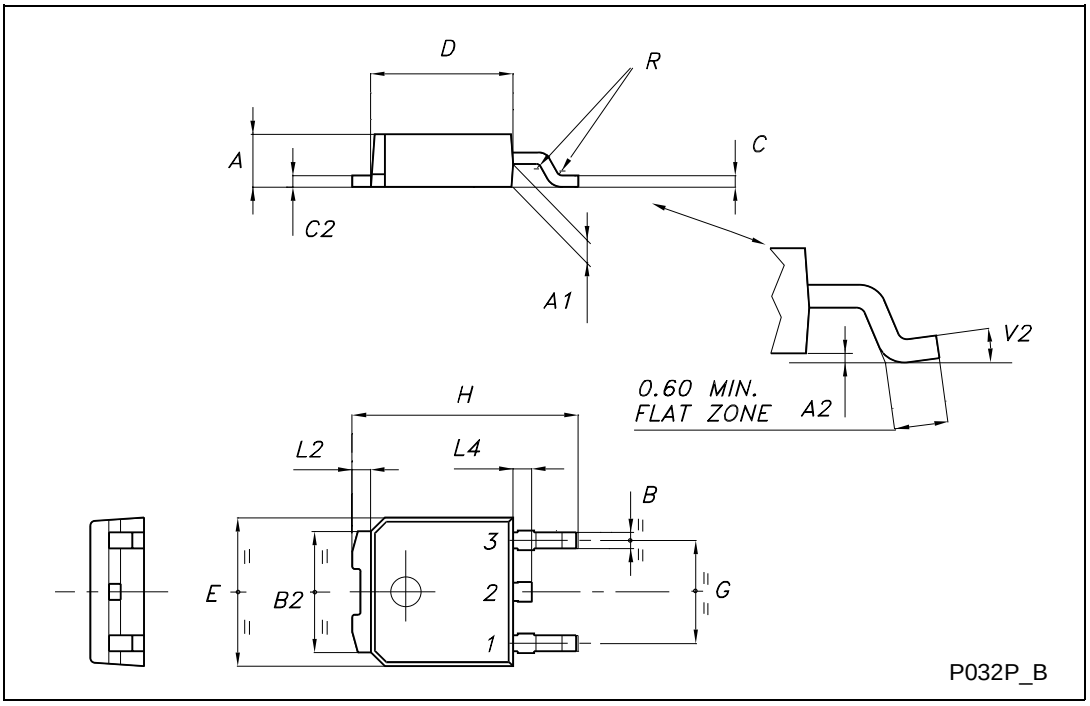


Figure 7: Gate Charge Test Circuit



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0^o		8^o	0^o		0^o



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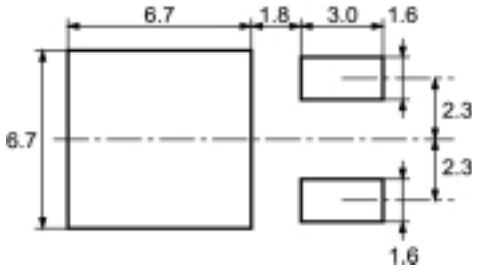
DPAK FOOTPRINT



All dimensions are in millimeters

TUBE SHIPMENT (no suffix)*

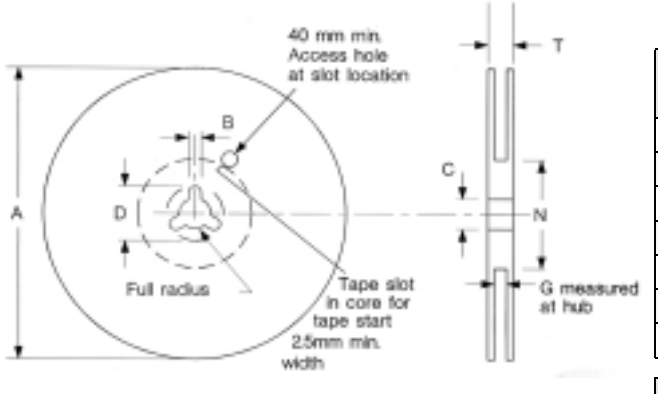
BASE QTY 75

BULK QTY 3000

Tube length 532 (±0.5)

All dimensions are in millimeters

TAPE AND REEL SHIPMENT (suffix "T4")*



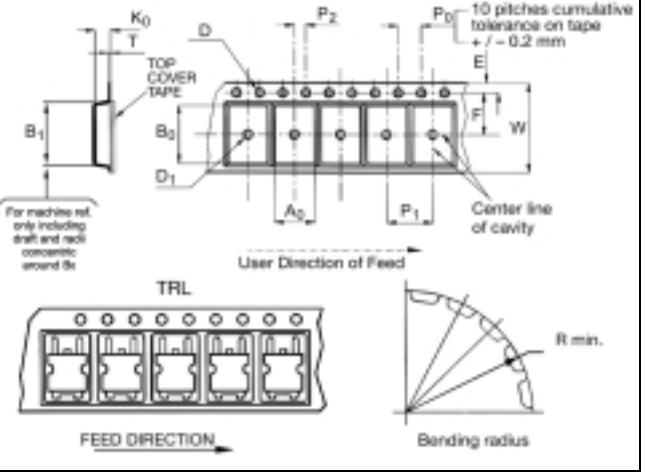
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



* on sales type

Table 12: Revision History

Date	Revision	Description of Changes
20-Sep-2004	4	New Stylesheet. No document change.