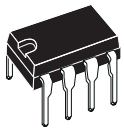
L6565

QUASI-RESONANT SMPS CONTROLLER

- QUASI-RESONANT (QR) ZERO-VOLTAGE-SWITCHING (ZVS) TOPOLOGY
- LINE FEED FORWARD TO DELIVER CONSTANT POWER vs. MAINS CHANGE
- FREQUENCY FOLDBACK FOR OPTIMUM STANDBY EFFICIENCY
- PULSE-BY-PULSE & HICCUP-MODE OCP
- ULTRA-LOW START-UP (< 70µA) AND QUIESCENT CURRENT (< 3.5mA)
- DISABLE FUNCTION (ON/OFF CONTROL)
- 1% PRECISION (@ T_j = 25°C) INTERNAL REFERENCE VOLTAGE
- ±400mA TOTEM POLE GATE DRIVER WITH UVLO PULL-DOWN
- BLUE ANGEL, ENERGY STAR, ENERGY 2000 COMPLIANT

APPLICATIONS

- TV/MONITOR SMPS
- AC-DC ADAPTERS/CHARGERS
- DIGITAL CONSUMER
- PRINTERS, FAX MACHINES, PHOTOCOPIERS AND SCANNERS



DIP8(Minidip)

SO-8

ORDERING NUMBERS:

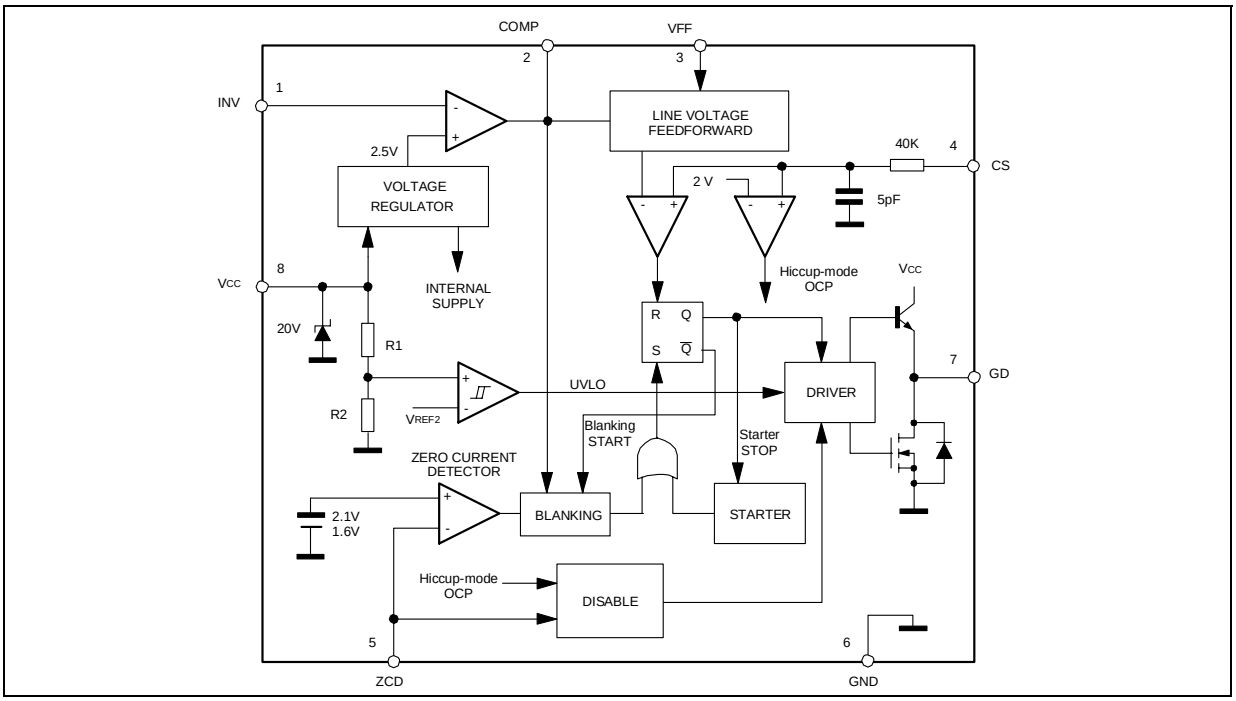
L6565N **L6565D**

DESCRIPTION

The L6565 is a current-mode primary controller IC, specifically designed to build offline Quasi-resonant ZVS (Zero Voltage Switching at switch turn-on) fly-back converters.

Quasi-resonant operation is achieved by means of a transformer demagnetization sensing input that triggers MOSFET's turn-on.

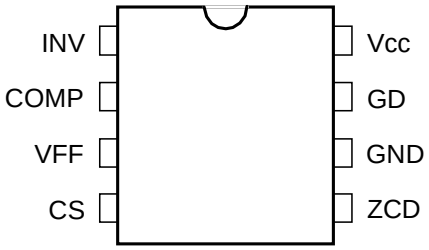
BLOCK DIAGRAM



DESCRIPTION (continued)

Converter's power capability variations with the mains voltage are compensated by line voltage feedforward. At light load the device features a special function that automatically lowers the operating frequency still maintaining the operation as close to ZVS as possible. In addition to very low start-up and quiescent currents, this feature helps keep low the consumption from the mains at light load and be Blue Angel and Energy Star compliant.
The IC includes also a disable function, an on-chip filter on current sense, an error amplifier with a precise reference voltage for primary regulation and an effective two-level overcurrent protection.

PIN CONNECTION (Top view, Minidip and SO8)



PIN DESCRIPTION

N°	Name	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage is fed into the pin through either a resistor divider (primary regulation) or an optocoupler (secondary feedback). This pin can be grounded in some secondary feedback schemes (see pin 2).
2	COMP	Output of the error amplifier. Typically, a compensation network is placed between this pin and the INV pin to achieve stability and good dynamic performance of the voltage control loop. With secondary feedback, the pin can be also driven directly by an optocoupler to control PWM by modulating the current sunk from the pin (with the INV pin grounded).
3	VFF	Line voltage feedforward. The information on the converter's input voltage is fed into the pin through a resistor divider and is used to change the setpoint of the pulse-by-pulse current limitation (the higher the voltage, the lower the setpoint). If this function is not desired the pin will be grounded and the current limitation setpoint will be maximum.
4	CS	Input to the PWM comparator. The primary current is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET's turn-off. The internal reference is clamped at a value, which defines the pulse-by-pulse current limitation setpoint, depending on the voltage at pin VFF. If the signal at the pin CS exceeds 2 V, the gate driver will be disabled (Hiccup-mode OCP).
5	ZCD	Transformer's demagnetization sensing input for Quasi-Resonant operation. Alternately, synchronization input for an external signal. A negative-going edge triggers MOSFET's turn-on. The trigger circuit is blanked for a minimum of 3.5 µs after MOSFET turn-off, for safe operation under short circuit conditions and frequency foldback. If the pin is grounded the IC will be disabled.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 400 mA (source and sink).
8	Vcc	Supply Voltage of both the signal part of the IC and the gate driver. An electrolytic capacitor is connected between this pin and ground. A resistor connected from this pin to the converter's input bulk capacitor will be typically used to start up the device.

THERMAL DATA

Symbol	Parameter	SO8	Minidip	Unit
$R_{th\ j\text{-}amb}$	Max. Thermal Resistance, Junction-to-ambient	150	100	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
I_{Vcc}	8	$I_{CC} + I_Z$	30	mA
I_{GD}	7	Output Totem Pole Peak Current (2 µs)	±700	mA
INV, COMP, VFF, CS	1, 2, 3 4	Analog Inputs & Outputs	-0.3 to 7	V
I_{ZCD}	5	Zero Current Detector	50 (source) -10 (sink)	mA
P_{tot}		Power Dissipation @T_{amb} = 50°C **(Minidip)** **(SO8)**	1 0.65	W
T_j		Junction Temperature Operating range	-40 to 150	°C
T_{stg}		Storage Temperature	-55 to 150	°C

ELECTRICAL CHARACTERISTCS

(T_j = -25 to 125°C, V_{CC} = 12V, C_o = 1nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
V_{cc}	Operating range	After turn-on	10.3		18	
V_{CCOn}	Turn-on threshold		12.5	13.5	14.5	V
V_{CCOff}	Turn-off threshold		8.7	9.5	10.3	V
Hys	Hysteresis		3.65	4	4.3	V
V_Z	Zener Voltage	I_{cc} = 25 mA	18	20	22	V
SUPPLY CURRENT						
$I_{start\text{-}up}$	Start-up Current	Before turn-on, V_{CC} = 12V		45	70	µA
I_q	Quiescent Current	After turn-on		2.3	3.5	mA
I_{CC}	Operating Supply Current	@ 70 kHz		3.5	5	mA
I_q	Quiescent Current	During Hiccup-mode OCP	1.6		3.5	mA
I_q	Quiescent Current	$V_{ZCD} < V_{DIS}$, $V_{CC} > V_{CCOff}$		1.4	2.1	mA
LINE FEEDFORWARD						
I_{VFF}	Input Bias Current	V_{VFF} = 0 to 3 V			-1	µA
V_{VFF}	Operating Range			0 to 3		V
K	Gain	V_{VFF} = 1.5V, V_{COMP} = 4V		0.16		
ERROR AMPLIFIER						
V_{INV}	Voltage Feedback Input Threshold	T_{amb} = 25°C	2.465	2.5	2.535	V
		12V < V_{CC} < 18V	2.44		2.56	
	Line Regulation	Vcc = 12 to 18V		2	5	mV
I_{INV}	Input Bias Current			-0.1	-1	µA

ELECTRICAL CHARACTERISTCS (continued)
(T_j = -25 to 125°C, V_{CC} = 12V, C_o = 1nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_V	Voltage Gain	Open loop	60	80		dB
GB	Gain-Bandwidth Product			1		MHz
I_{COMP}	Source Current	V_{COMP} = 4V, V_{INV} = 2.4 V	-2	-3.5	-5	mA
	Sink Current	V_{COMP} = 4V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper Clamp Voltage	I_{SOURCE} = 0.5 mA	5	5.5		V
	Lower Clamp Voltage	I_{SINK} = 0.5 mA		2.25	2.55	V
CURRENT SENSE COMPARATOR						
I_{CS}	Input Bias Current	V_{CS} = 0		-0.05	-1	µA
$t_{d(H-L)}$	Delay to Output			200	450	ns
V_{CSx}	Current Sense Reference Clamp	V_{COMP} = Upper clamp, V_{VFF} = 0V	1.28	1.4	1.5	V
		V_{COMP} = Upper clamp, V_{VFF} = 1.5V	0.62	0.7	0.78	
		V_{COMP} = Upper clamp, V_{VFF} = 3V		0	0.2	
V_{CSdis}	Hiccup-mode OCP level		1.85	2.0	2.2	V
ZERO CURRENT DETECTOR/ SYNCHRONIZATION						
V_{ZCDH}	Upper Clamp Voltage	I_{ZCD} = 3mA	4.7	5.2	6.1	V
V_{ZCDL}	Lower Clamp Voltage	I_{ZCD} = - 3mA	0.3	0.65	1	V
V_{ZCDA}	Arming Voltage (positive-going edge)	(1)		2.1		V
V_{ZCDT}	Triggering Voltage (negative-going edge)			1.6		V
I_{ZCDb}	Input Bias Current	V_{ZCD} = 1 to 4.5 V		2		µA
I_{ZCDsrc}	Source Current Capability		-3		-10	mA
I_{ZCDsnk}	Sink Current Capability		3		10	mA
V_{DIS}	Disable Threshold		150	200	250	mV
I_{ZCDr}	Restart Current After Disable	V_{ZCD} < V_{DIS}, Vcc > Vcc_{off}	-70	-150	-230	µA
T_{BLANK}	Blanking time after pin 7 high-to-low transition	V_{COMP} ≥ 3.2 V		3.5		µs
		V_{COMP} = 2.5 V		18		
START TIMER						
t_{START}	Start Timer period		250	400	550	µs
GATE DRIVER						
V_{OL}	Dropout Voltage	$I_{GDsource}$ = 200mA		1.2	2	V
		$I_{GDsource}$ = 20mA		0.7	1	
V_{OH}		I_{GDsink} = 200mA			2	V
		I_{GDsink} = 20mA			0.3	
t_f	Current Fall Time			40	100	ns
t_r	Current Rise Time			40	100	ns
I_{GDoff}	I_{GD} sink current	Vcc = 4 V, V_{GD} = 1 V	5	10		mA

(1) Parameters guaranteed by design, not tested in production.

Figure 1. Supply current vs. Supply voltage

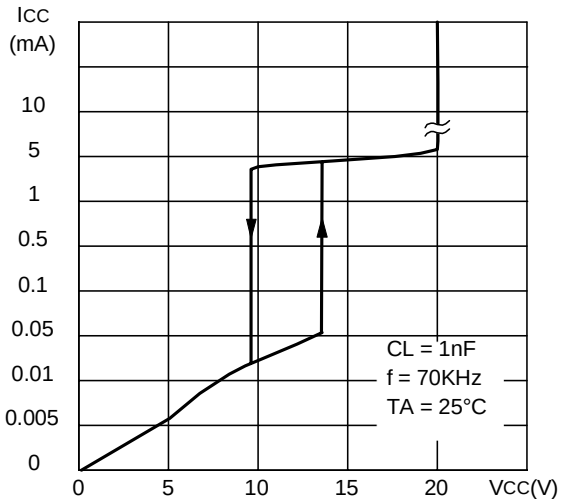


Figure 2. Start-up & UVLO vs. Temperature

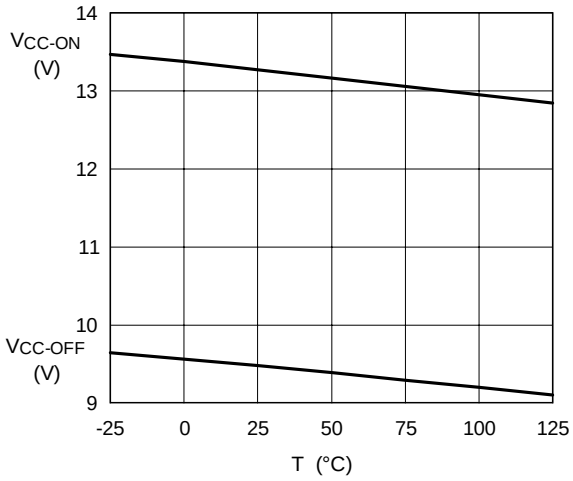


Figure 3. Feedback reference vs. Temperature

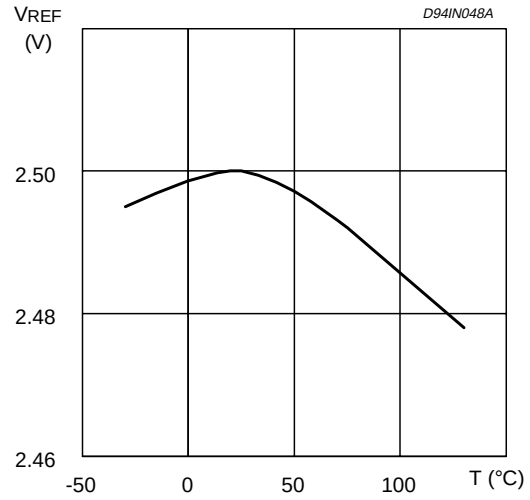


Figure 4. Line feedforward characteristics

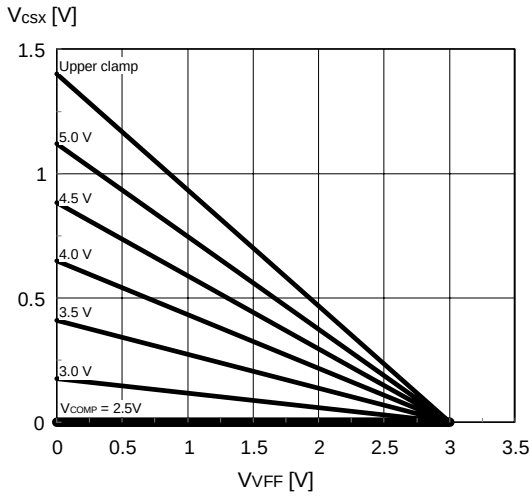


Figure 5. Pin 2 (COMP) V-I characteristics

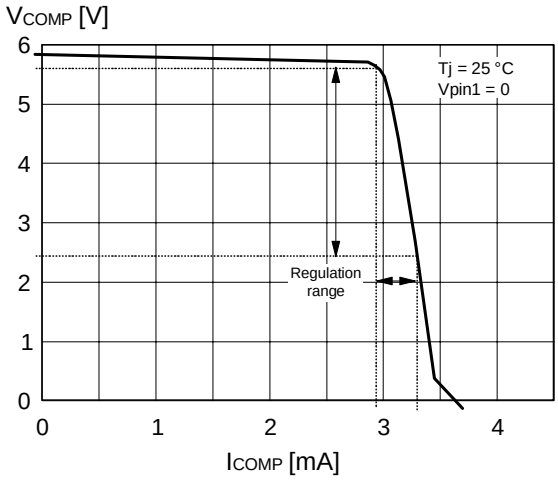


Figure 6. ZCD blanking time vs. COMP voltage

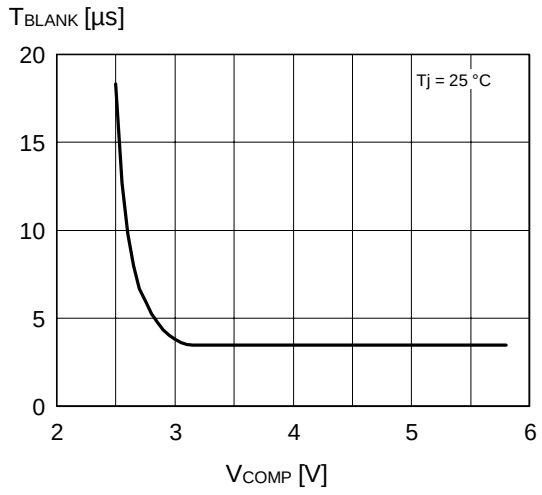


Figure 7. Gate-drive output saturation

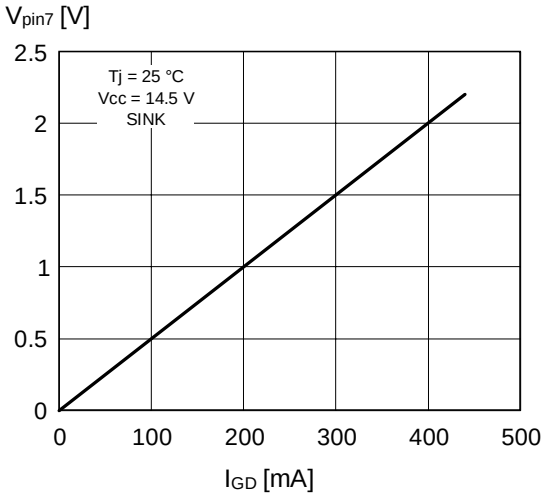


Figure 8. Gate-drive output saturation

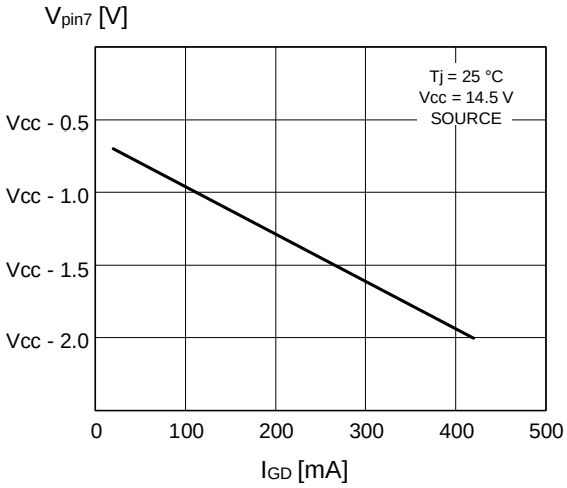


Figure 9. IC consumption vs. temperature

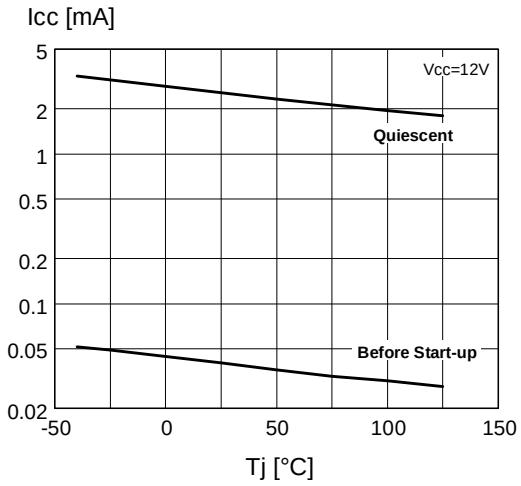


Figure 10. Zener voltage at Vcc pin vs. Tj

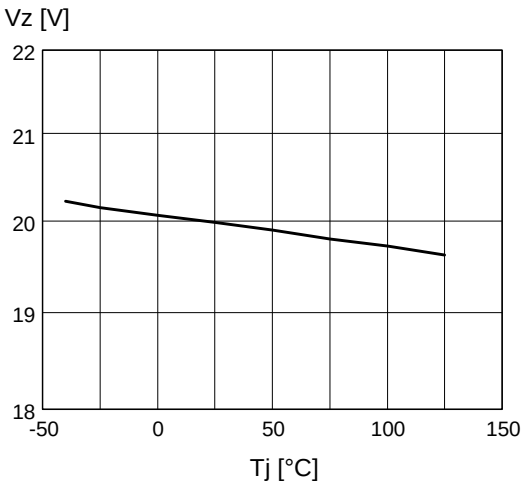
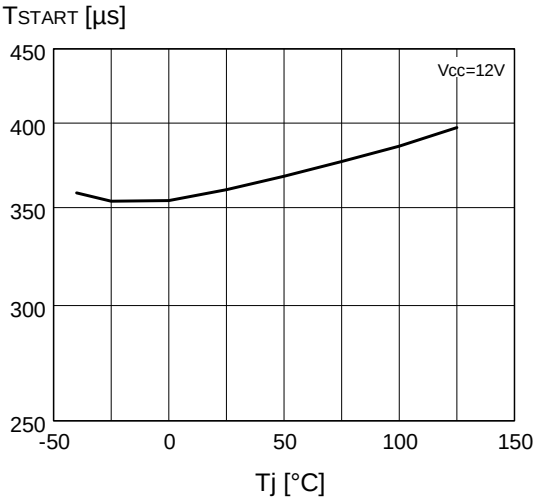


Figure 11. Start-up timer period vs. Tj



APPLICATION INFORMATION

Quasi-resonant operation in offline flyback converters lies in synchronizing MOSFET's turn-on to the transformer's demagnetization. Detecting the resulting negative-going edge of the voltage across any winding of the transformer can do this. The L6565 is provided with a dedicated pin that allows doing the job with a very simple interface, just one resistor.

Variable frequency operation - as a result of different operating conditions in terms of input voltage and output current - is inherent in such functionality. The system always works close to the boundary between DCM (Discontinuous Conduction Mode) and CCM (Continuous Conduction Mode) operation of the transformer. The operation is then identical to that of the so-called self-oscillating or Ringing Choke Converter (RCC).

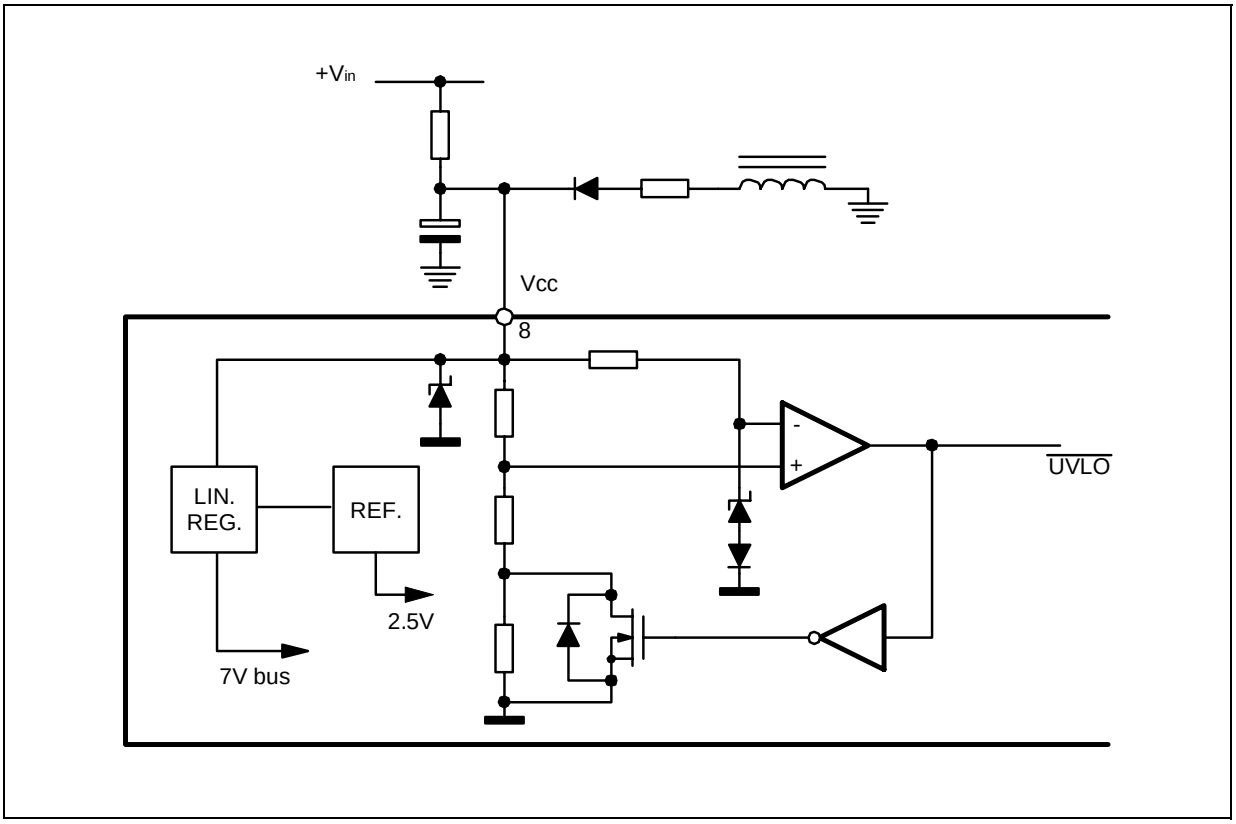
Detailed Device Description

Internal Supply Block (see fig. 12)

A linear voltage regulator supplied by V_{CC} (pin 8) generates an internal 7V rail used for supplying the entire IC, except for the gate driver that is supplied directly from Vcc. In addition, a bandgap circuit generates a precise internal reference (2.5V±1% @ 25°C) used by the control loop to ensure a good regulation with primary feedback technique.

In figure 12 it is also shown the undervoltage lockout (UVLO) comparator with hysteresis used to enable the chip as long as the Vcc voltage is high enough to ensure a reliable operation.

Figure 12. L6565 internal supply block



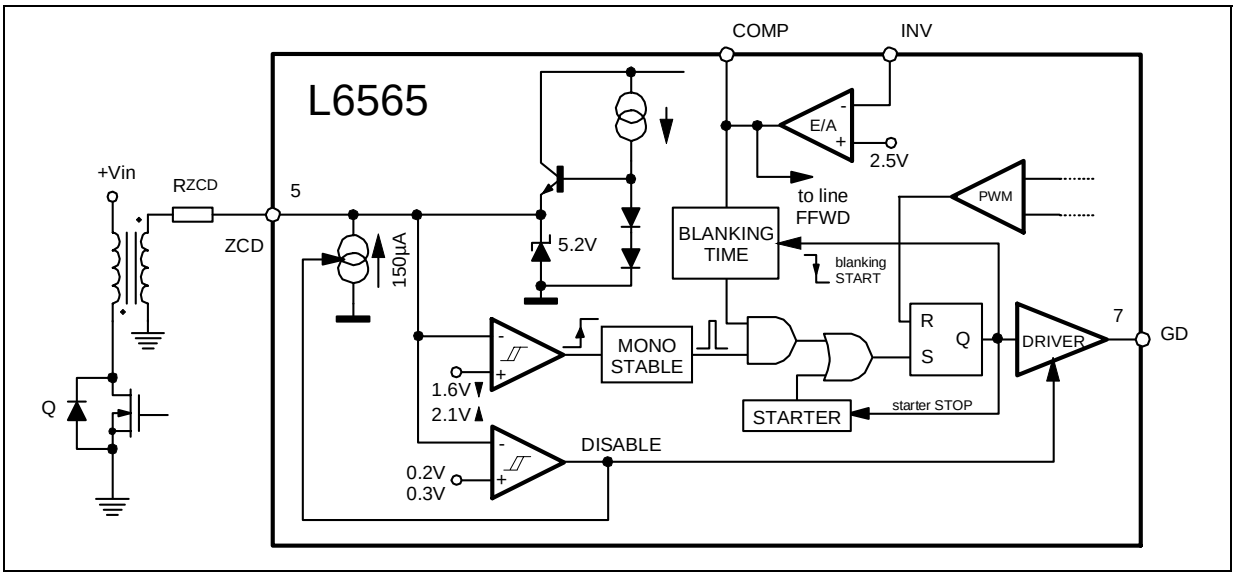
Zero Current Detection and Triggering Block (see fig. 13):

The Zero Current Detection (ZCD) block switches on the external MOSFET if a negative-going edge falling below 1.6 V is applied to the input (pin 5, ZCD). However, to ensure high noise immunity, the triggering block must be armed first: prior to falling below 1.6V, the voltage on pin 5 must experience a positive-going edge exceeding 2.1 V.

This feature is typically used to detect transformer demagnetization for QR operation, where the signal for the ZCD input is obtained from the transformer's auxiliary winding used also to supply the IC. Alternatively, this can be used to synchronize MOSFET's turn-on to the negative-going edge of an external clock signal, in case the device is not required to work in QR mode but as a standard PWM controller in a synchronized system (e.g. monitor SMPS).

The triggering block is blanked for a certain time after the MOSFET has been turned off. This has two goals: first, to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously; second, to realize the Frequency Foldback function (see the relevant description).

Figure 13. Zero Current Detection and Triggering Block; Disable and Frequency Foldback Blocks



A circuit is needed that turns on the external MOSFET at start-up since no signal is coming from the ZCD pin. This is realized with an internal starter, which forces the driver to deliver a pulse to the gate of the MOSFET.

To minimize the external interface with the synchronization source (either the auxiliary winding or an external clock), the voltage at the pin is both top and bottom limited by a double clamp, as illustrated in the internal diagram of the ZCD block of figure 13. The upper clamp is typically located at 5.2 V, while the lower clamp is at one V_{BE} above ground. The interface will then be made by just one resistor that has to limit the current sourced by and sunk from the pin within the rated capability of the internal clamps.

Disable Block (see fig. 13):

The ZCD pin is used also to activate the Disable Block. If the voltage on the pin is taken below 150 mV the device will be shut down. To do so, it is necessary to override the source capability (10 mA max.) of the internal lower clamp. While in disable, the current consumption of the IC will be reduced. To re-enable device operation, the pull-down on the pin must be released.

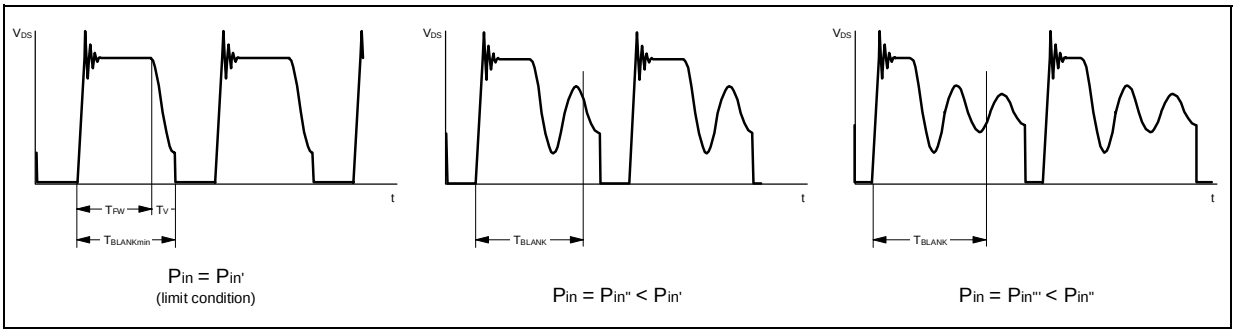
Frequency Foldback Block (see fig. 13):

To prevent the switching frequency from reaching too high values, which is a typical drawback of QR operation,

the L6565 puts a limit on the minimum OFF-time of the switch. This is done by blanking the triggering block of the ZCD circuit as mentioned before. The duration of the blanking time (3.5µs min.) is a function of the error amplifier output VCOMP, as shown in the diagram of figure 6.

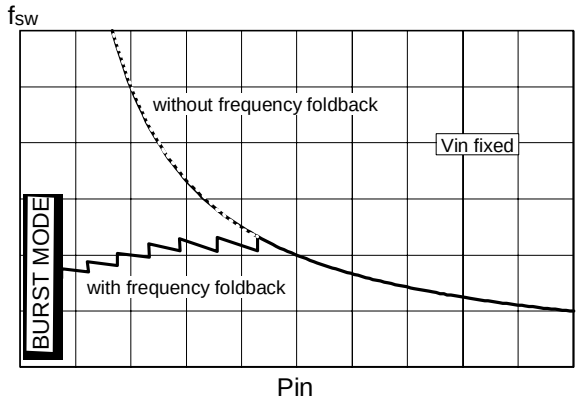
If the load current and the input voltage are such that the switch OFF-time falls below the minimum blanking time of 3.5µs, the system will enter the "Frequency Foldback" mode, a sort of "ringing cycle skipping" illustrated schematically in figure 14.

Figure 14. Frequency foldback: ringing cycle skipping as the load is progressively reduced



In this mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps (2·Tv), while the OFF-time needed for cycle-by-cycle energy balance may fall in between. Thus one or more longer switching cycles will be compensated by one or more shorter ones and vice versa. However, this mechanism is absolutely normal and there is no appreciable effect on the performance of the converter or on its output voltage.

Figure 15. Frequency Foldback: qualitative frequency dependence on power throughput

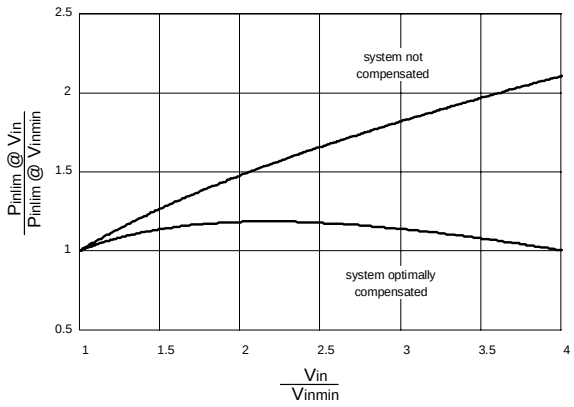


Further load reductions involve lower values for VCOMP, which increases the blanking time. Therefore, more and more ringing cycles will be skipped. When the load is low enough, so many ringing cycles need to be skipped that their amplitude becomes very small and they can no longer trigger the ZCD circuit. In that case the internal starter of the IC will be activated, resulting in burst-mode operation: a series of few switching cycles spaced out by long periods where the MOSFET is in OFF state.

Voltage Feedforward block (see fig. 17b):

The power that QR flyback converters with a fixed overcurrent setpoint (like fixed-frequency systems) are able to deliver changes with the input voltage considerably. With wide-range mains, at maximum line it can be more than twice the value at minimum line, as shown by the upper curve in the diagram of figure 16. The L6565 has the Line Feedforward function available to solve this issue.

Figure 16. Typical power capability change vs. input voltage in ZVS QR flyback converters

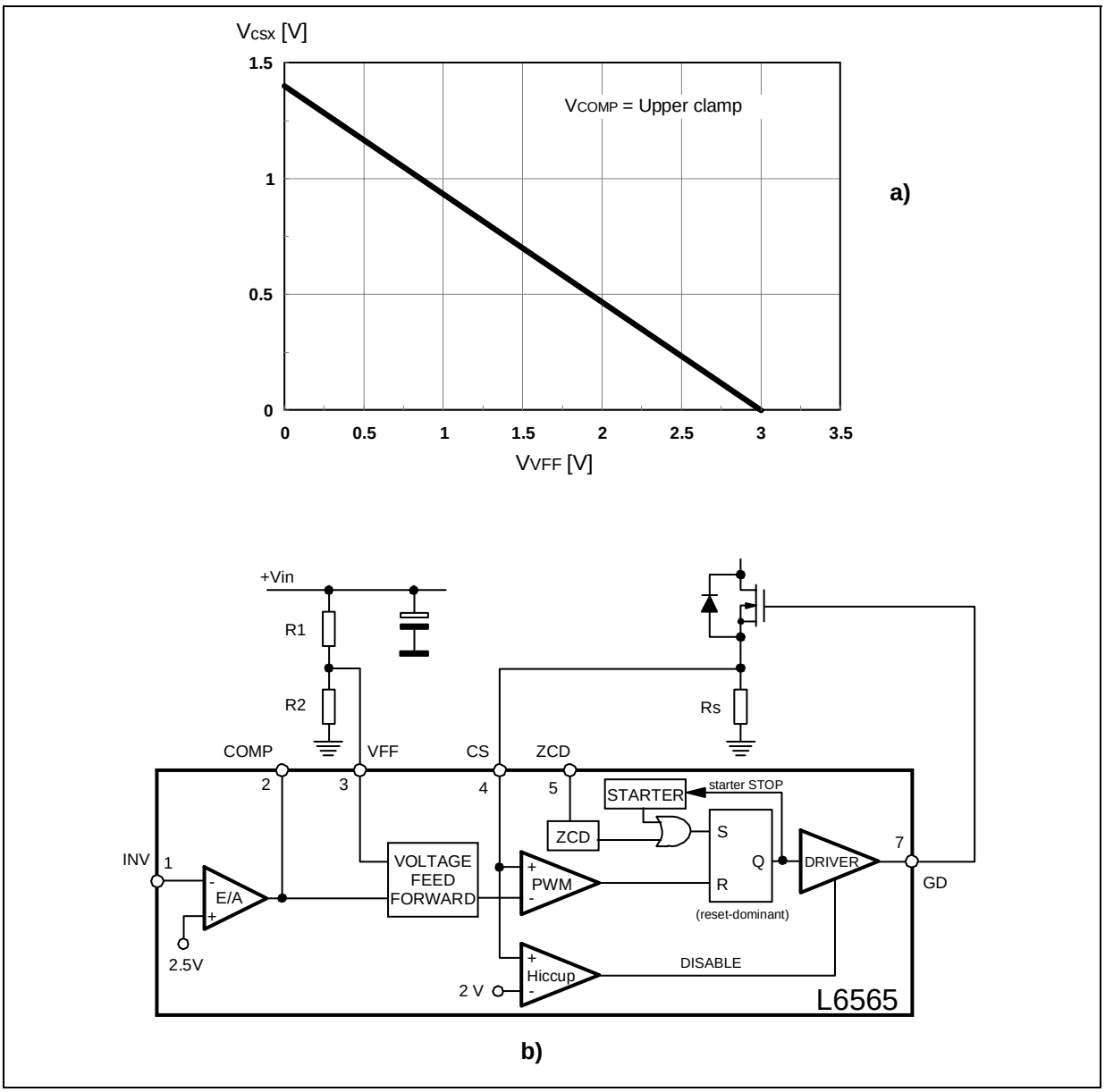


It acts on the clamp level of the control voltage V_{csx}, that is on the overcurrent setpoint, so that it is a function of the converter's input voltage sensed through a dedicated pin (#3, VFF): the higher the input voltage, the lower the setpoint. This is illustrated in the diagram of figure 17a that shows the relationship between the voltage at the pin VFF and V_{csx} (with the error amplifier saturated high in the attempt of keeping output voltage regulation). The schematic in figure 17b shows also how the function is included in the control loop. With a proper selection of the external divider R1-R2 it is possible to achieve the optimum compensation described by the lower curve in the diagram of figure 16.

In applications where this function is not wanted, e.g. because of a narrow input voltage range, the VFF pin can be simply grounded, thus saving the resistor divider. The overcurrent setpoint will be then fixed at the maximum value of about 1.4V (1.5V max.).

Line Feedforward is also beneficial to other characteristics of quasi-resonant converters: it improves their input ripple rejection ability and limits the variation of the power stage's small-signal gain versus the line voltage.

Figure 17. a) Overcurrent setpoint vs. VFF voltage; b) Line Feedforward function block



Error Amplifier Block (see fig. 17b):

The Error Amplifier (E/A) inverting input is used in primary feedback technique to compare a partition of the voltage generated by the auxiliary winding with the internal reference, to achieve converter's output voltage regulation (see "Application Ideas", fig. 24). With secondary feedback (typically using a TL431 at the secondary side and an optocoupler to transfer output voltage information to the primary side through the isolation barrier) the E/A can be used as an inverting level-shifter to achieve negative feedback and shape the loop gain (see "Application Ideas", fig. 23).

The E/A output is used typically for control loop compensation, realized with an RC network connected to the inverting input. With other secondary feedback techniques, the output is driven directly by an emitter-grounded optocoupler to modulate the duty cycle (the inverting input will be grounded in that case - see figure 23 in "Application Ideas").

Current Comparator, PWM Latch and Hiccup-mode OCP (see fig. 17b):

The current comparator senses the voltage across the current sense resistor (Rs) and, by comparing it with the programming signal delivered by the feedforward block, determines the exact time when the external MOSFET is to be switched off. The PWM latch avoids spurious switching of the MOSFET, which might result from the noise generated ("double-pulse suppression").

A comparator senses the voltage on the current sense input and disables the gate driver if the voltage at the pin exceeds 2 V. Such anomalous condition is typically generated by a short circuit on the secondary rectifier or on the secondary winding. To re-enable the driver, first the IC must be turned off and then can be restarted, that is the Vcc voltage must fall below the UVLO threshold.

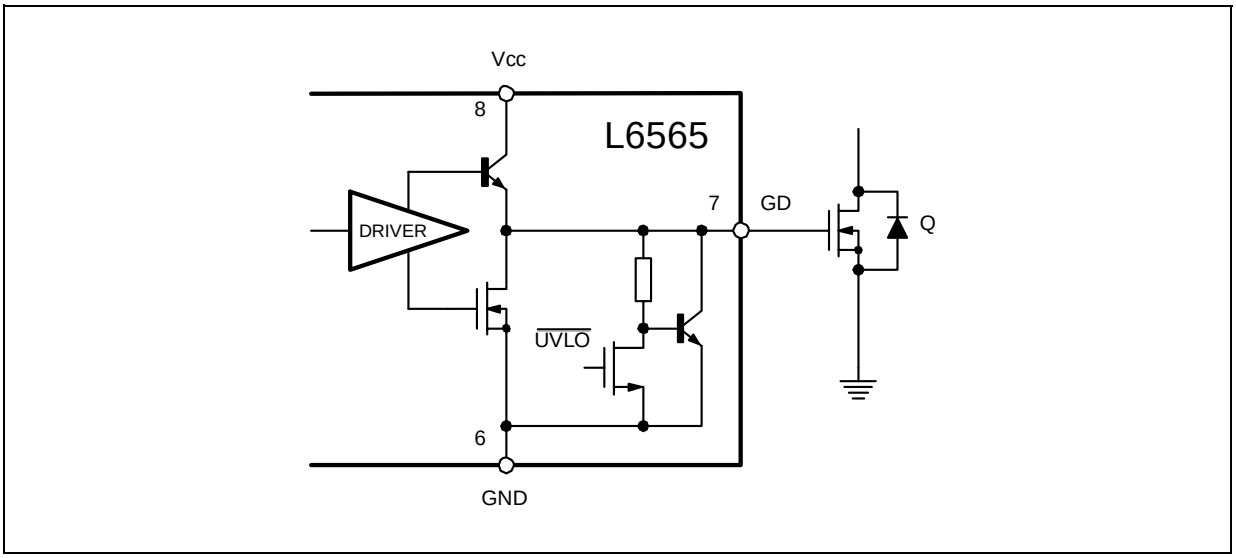
When the gate driver is disabled the quiescent current of the IC is unchanged and, since no energy is coming from the self-supply circuit, the Vcc capacitor will be discharged below the UVLO threshold after some time. Then the device will initiate a new start-up cycle. In case of failure of the secondary diode the resulting behavior will be a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit.

Gate Driver (see fig. 18):

A totem pole buffer, with 400mA source and sink capability, drives the external MOSFET. It is made up of a high-side NPN Darlington and a low-side MOSFET. In this way there is no need of an external diode clamp to prevent the voltage at the gate drive output (pin 7, GD) from being pulled too negative.

An internal pull-down circuit holds the output low when the device is in UVLO conditions, to ensure that the external MOSFET cannot be turned on accidentally (e.g. at power-on).

Figure 18. Gate driver with UVLO pull-down



TYPICAL APPLICATIONS

Figure 19. 50W Wide Range Mains SMPS for 14" TV

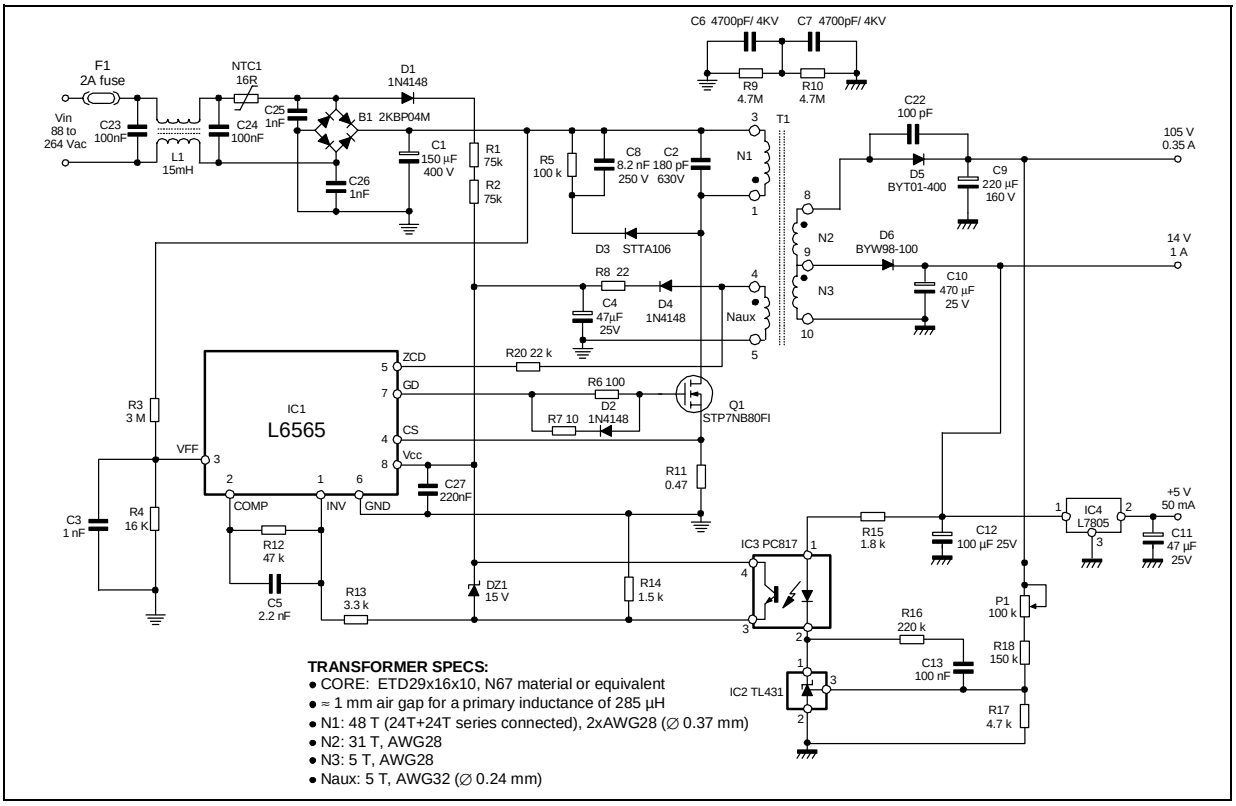
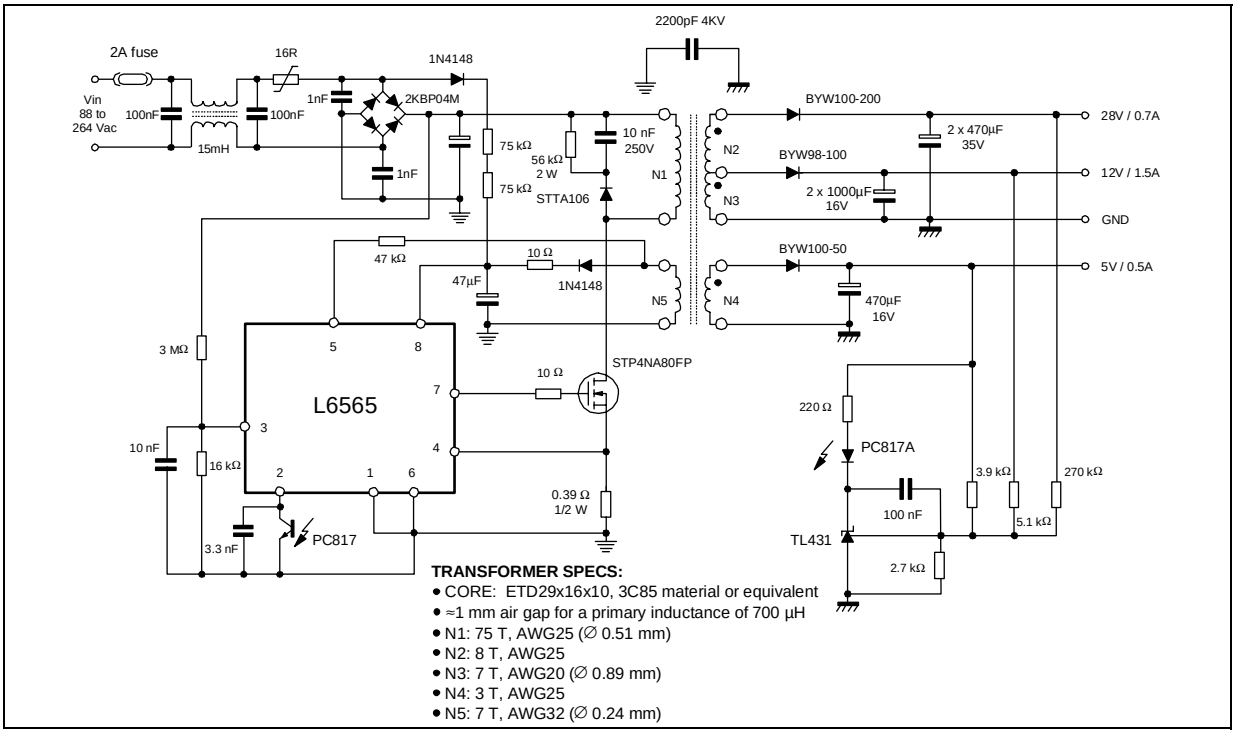


Figure 20. 40W Wide Range Mains SMPS for inkjet printer



APPLICATION IDEAS

Here follows a series of ideas/suggestions aimed at either improving performance or solving common application issues of L6565-based power supplies.

Figure 21. Enhanced turn-off for big MOSFET's drive

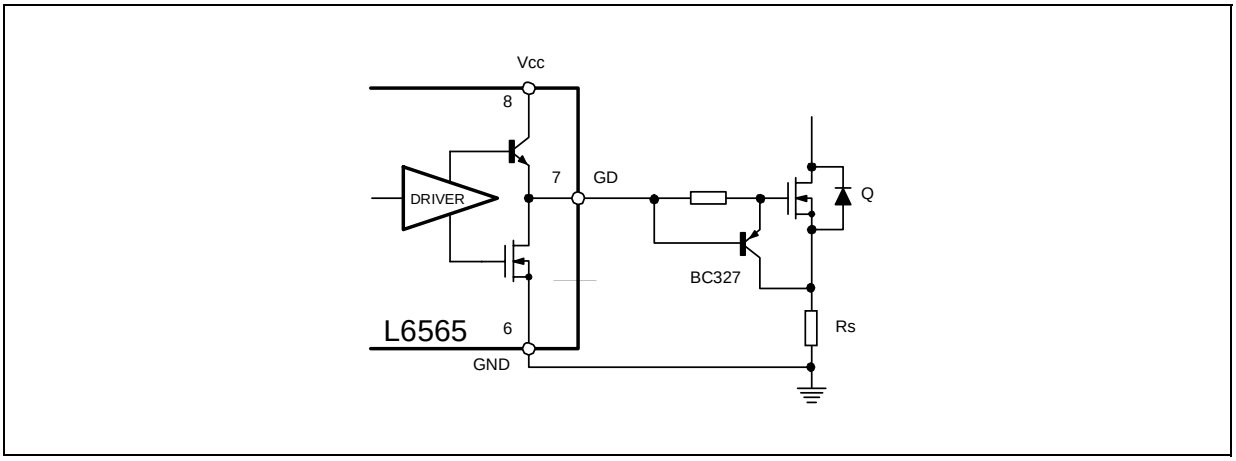


Figure 22. Latched shutdown on: a) feedback disconnection; b) overload or short circuit

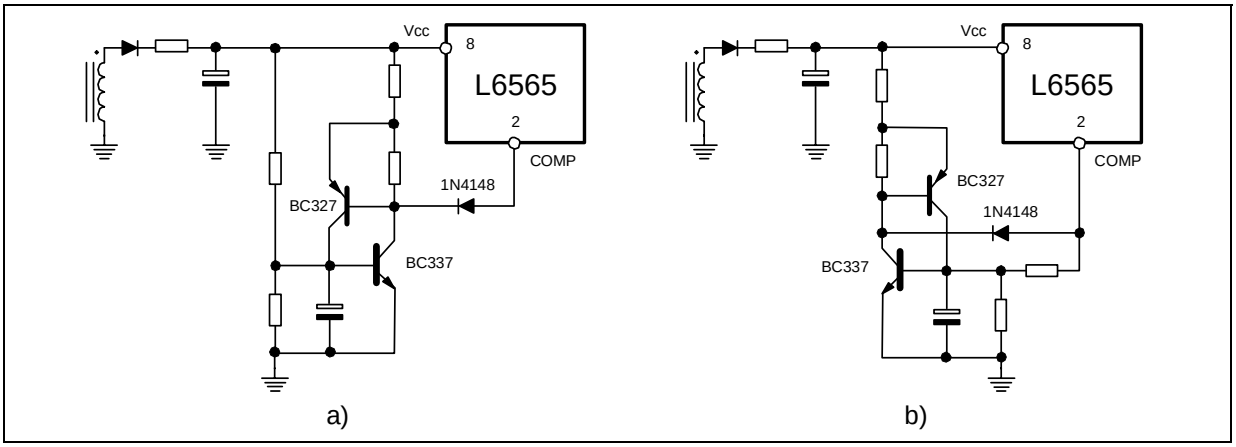


Figure 23. Secondary Feedback loop configurations

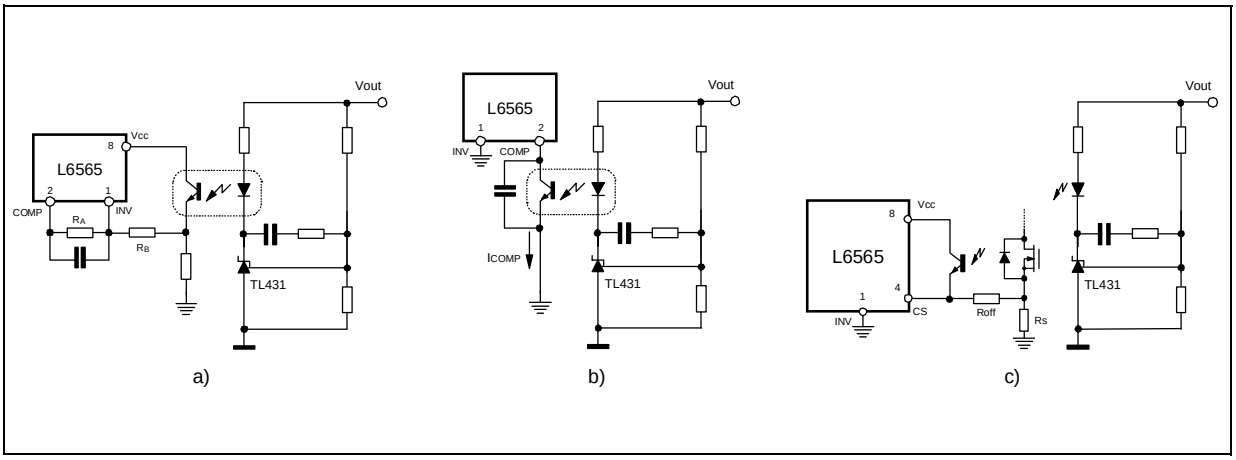


Figure 24. Primary Feedback loop configurations

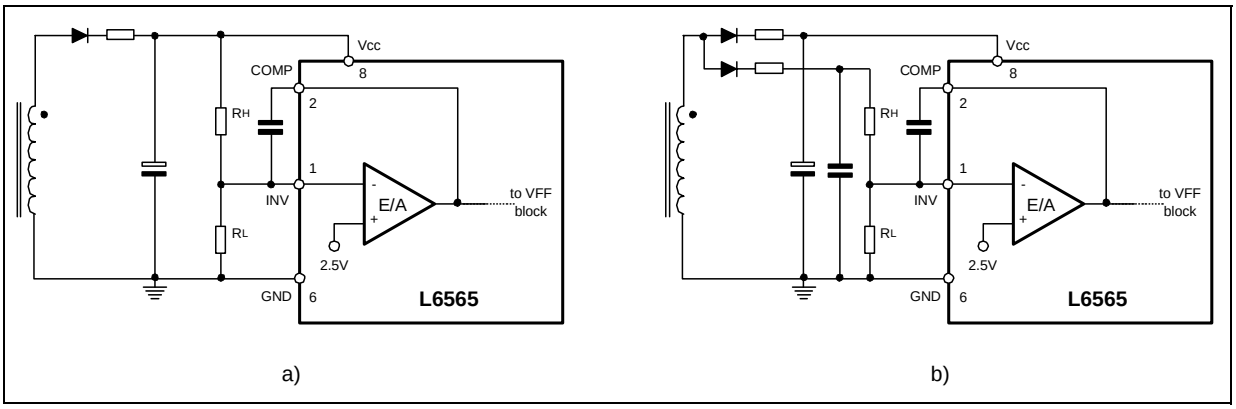


Figure 25. Protection against secondary feedback disconnection by primary regulation take-over

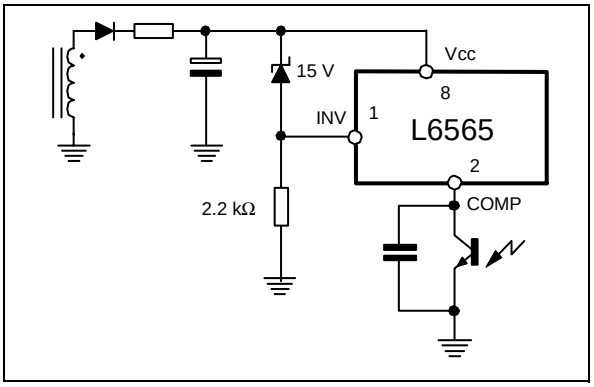


Figure 26. Leading edge blanking circuit for enhanced primary regulation

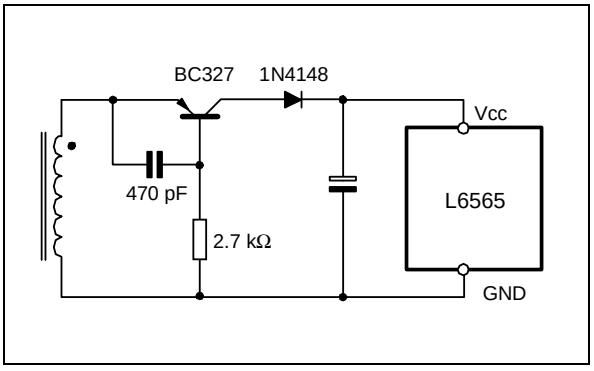


Figure 27. Remote ON/OFF control

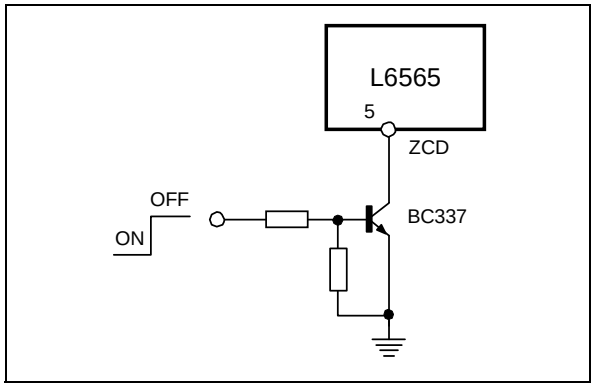
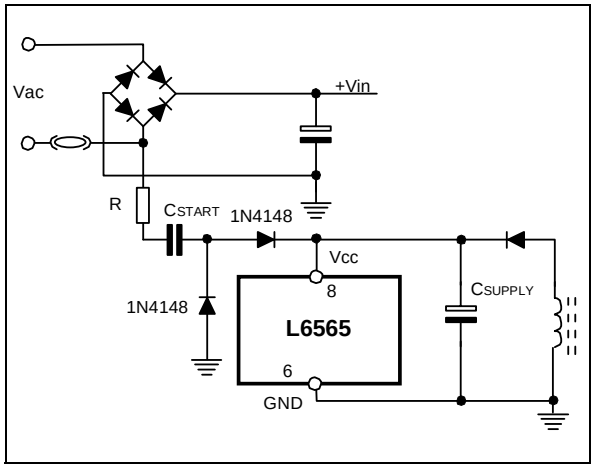


Figure 28. Low-consumption start-up circuit



RELATED DOCUMENTATION

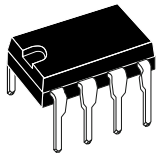
[1] "L6565, QUASI-RESONANT CONTROLLER" (AN1326)

[2] "25W QUASI-RESONANT FLYBACK CONVERTER FOR SET-TOP BOX APPLICATIONS USING THE L6565" (AN1376)

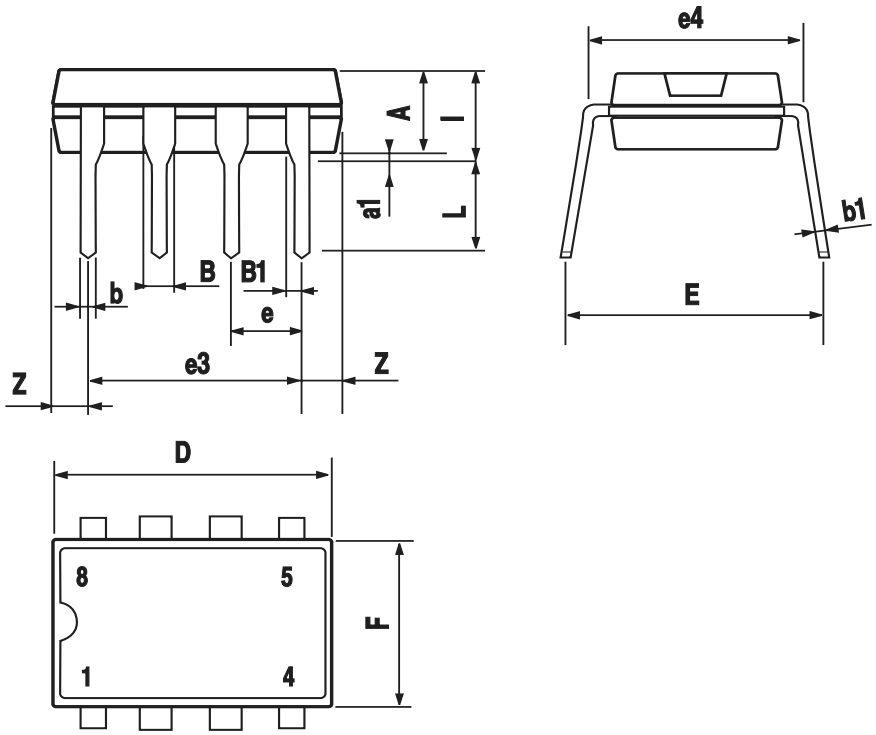
[3] "EVAL6565N, 30W AC-DC ADAPTER WITH THE L6565 QUASI-RESONANT PWM CONTROLLER" (AN1439).

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



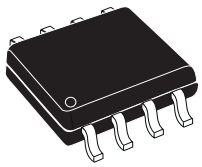
Minidip



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA



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