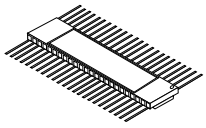
54VCXH162373

LOW VOLTAGE CMOS 16-BIT D-TYPE LATCH (3-STATE) WITH 3.6V TOLERANT INPUTS AND OUTPUTS

- 3.6V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED :
  t_{PD} = 3.3 ns (MAX.) at V_{CC} = 3.0 to 3.6V
  t_{PD} = 4.5 ns (MAX.) at V_{CC} = 2.3 to 2.7V
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 12mA (MIN) at V_{CC} = 3.0V
  $|I_{OH}| = I_{OL}$ = 8mA (MIN) at V_{CC} = 2.3V
- 26Ω SERIE RESISTOR IN OUTPUTS
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2.3V to 3.6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES H162373
- BUS HOLD PROVIDED ON DATA INPUTS
- LATCH-UP PERFORMANCE EXCEEDS 300mA (JESD 17)
- ESD PERFORMANCE:
  HBM > 2000V (MIL STD 883 method 3015);
  MM > 200V
- 100 Krad mil. 1019.6 (RHA QUAL) CONDITION A
- NO SEL, NO SEU UNDER 72 Mev/cm^2/mg LET HEAVY IONS IRRADIATION
- PRODUCT UNDER QML-V QUALIFICATION



FPC-48

DESCRIPTION

The 54VCXH162373 is a low voltage CMOS 16 BIT D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and five-layer metal wiring C^{2}MOS technology. It is ideal for low power and very high speed 2.3 to 3.6V applications; it can be interfaced to 3.6V signal environment for both inputs and outputs.

These 16 bit D-TYPE latches are bite controlled by two latch enable inputs (nLE) and two output enable inputs ($\overline{OE}$).

While the nLE input is held at a high level, the nQ outputs will follow the data input precisely.

When the nLE is taken low, the nQ outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state. Bus hold on data inputs is provided in order to eliminate the need for external pull-up or pull-down resistor. The device circuits is including 26Ω series resistance in the outputs. These resistors permit to reduce line noise in high speed applications.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION

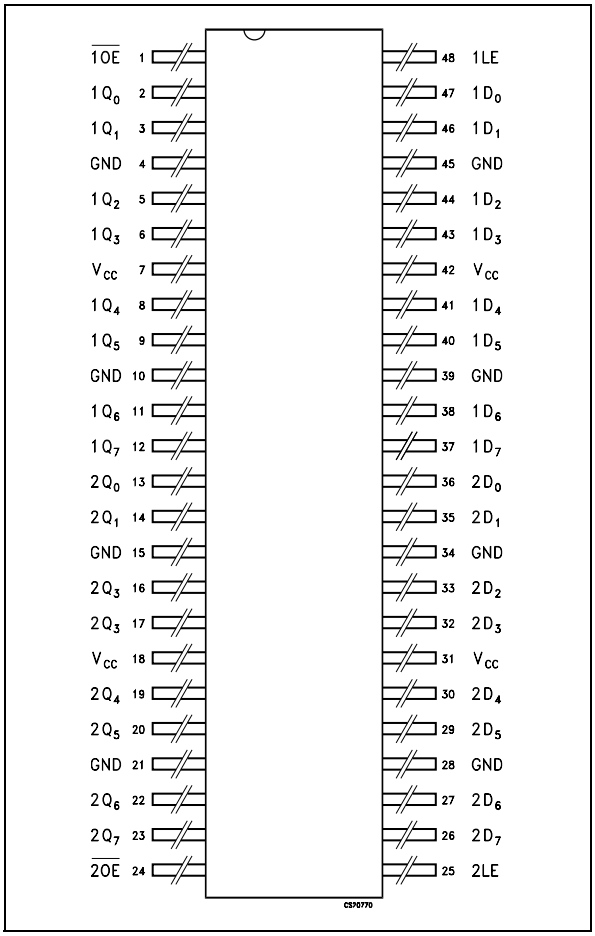


Table 1: Ordering Codes

PACKAGE	SOLDER DIPPING	FLYING MODEL		ENGINEERING MODEL
		QML-V	QML-Q	
FPC-48	GOLD	RHRXH162373K01V	RHRXH162373K01Q	RHRXH162373K1
				RHRXH162373K2 (*)
FPC-48	SOLDER	RHRXH162373K02V	RHRXH162373K02Q	

(*) EM with 48 hours Burn-In

Figure 1: Input And Output Equivalent Circuit

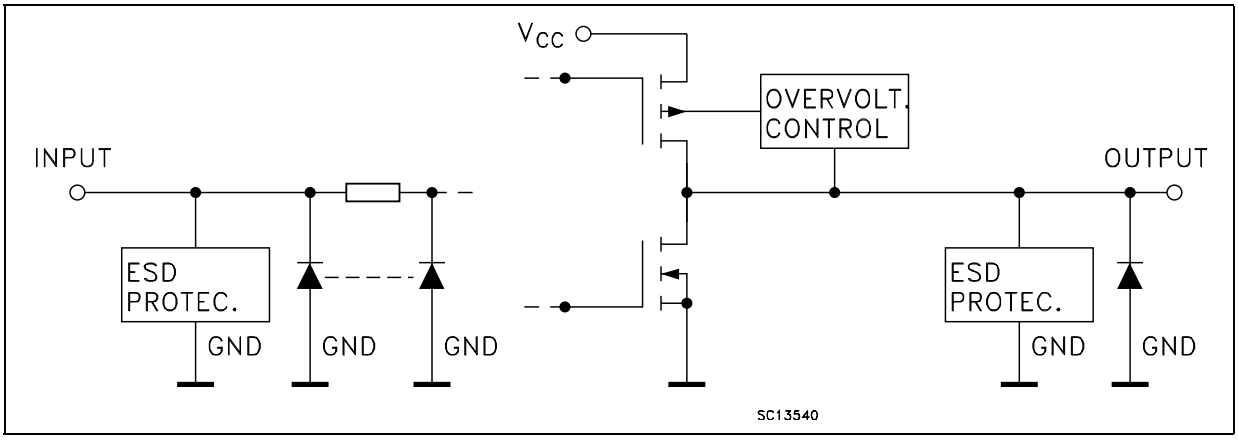


Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	$2\overline{OE}$	3 State Output Enable Input (Active LOW)
25	2LE	Latch Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1LE	Latch Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE *
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
* : Q outputs are latched at the time when the LE input is taken low logic level.

Figure 2: IEC Logic Symbols

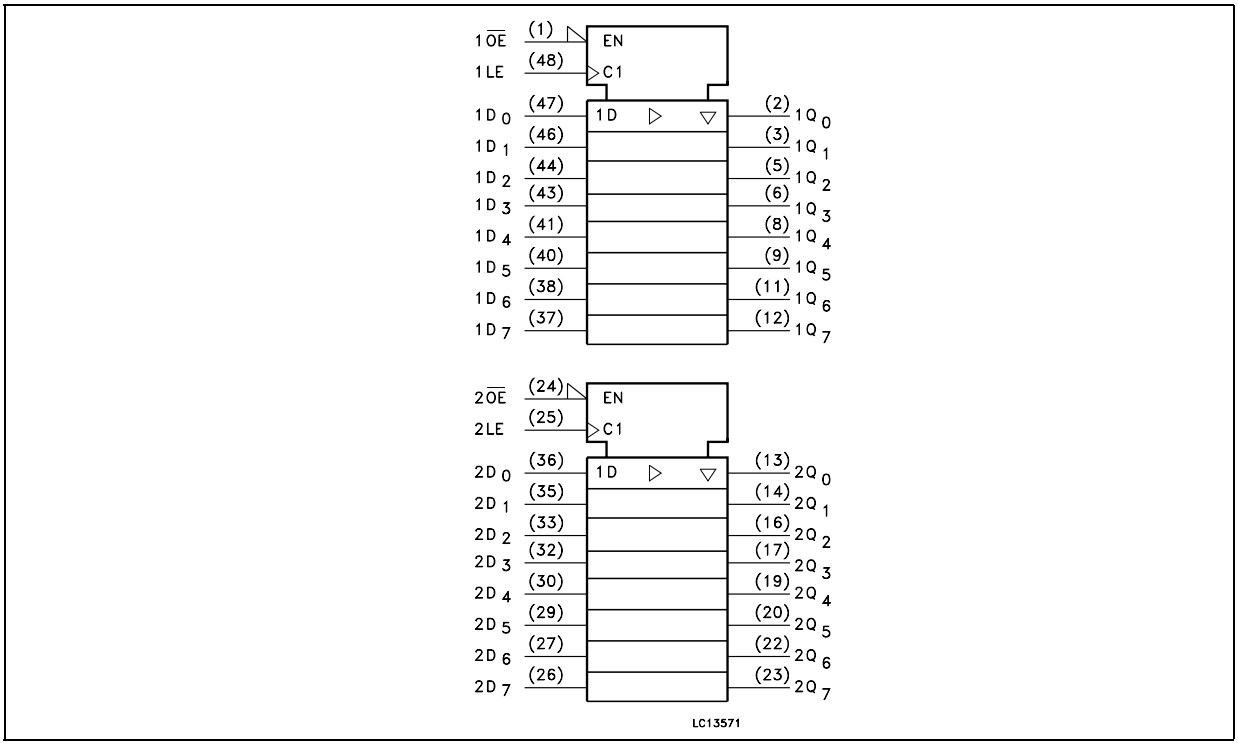
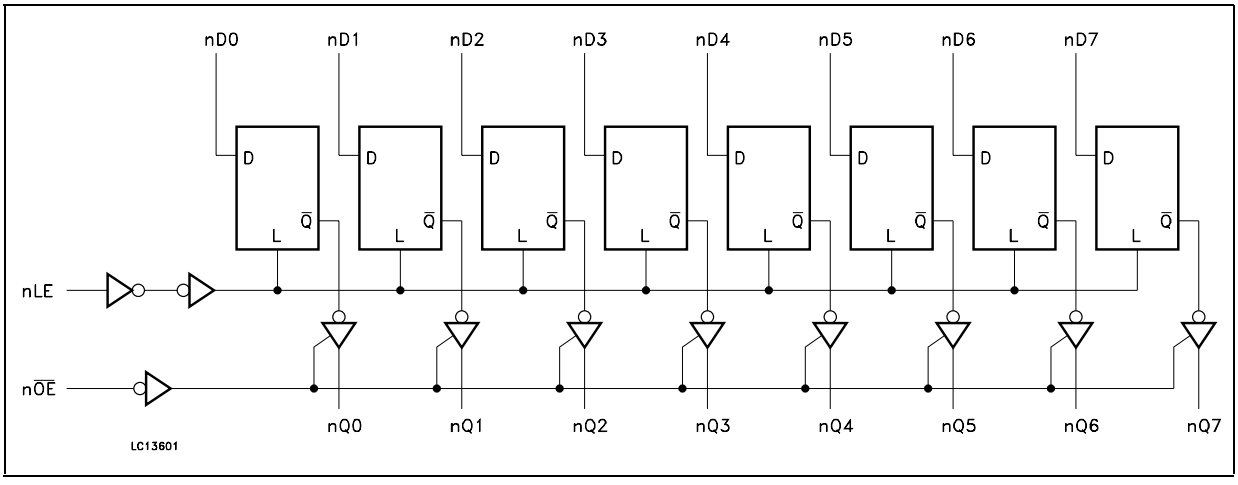


Figure 3: Logic Diagram



This logic diagram has not to be used to estimate propagation delays

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +4.6	V
V_I	DC Input Voltage	-0.5 to +4.6	V
V_O	DC Output Voltage (OFF State)	-0.5 to +4.6	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin	± 100	mA
P_D	Power Dissipation	400	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
1) I_O absolute maximum rating must be observed
2) V_O < GND, V_O > V_{CC}

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.3 to 3.6	V
V_I	Input Voltage	-0.3 to 3.6	V
V_O	Output Voltage (OFF State)	0 to 3.6	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 3.0 to 3.6V)	± 12	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 2.3 to 2.7V)	± 8	mA
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1)	0 to 10	ns/V

1) V_{IN} from 0.8V to 2V at V_{CC} = 3.0V

Table 6: DC Specifications (2.7V < V_{CC} ≤ 3.6V unless otherwise specified)

Symbol	Parameter	Test Condition		Value		Unit
		V_{CC} (V)		-55 to 125 °C		
				Min.	Max.	
V_{IH}	High Level Input Voltage	2.7 to 3.6		2.0		V
V_{IL}	Low Level Input Voltage				0.8	
V_{OH}	High Level Output Voltage	2.7 to 3.6	I_O=-100 µA	V_{CC}-0.2		V
		2.7	I_O=-6 mA	2.2		
		3.0	I_O=-8 mA	2.4		
			I_O=-12 mA	2.2		
V_{OL}	Low Level Output Voltage	2.7 to 3.6	I_O=100 µA		0.2	V
		2.7	I_O=6 mA		0.4	
		3.0	I_O=8 mA		0.55	
			I_O=12 mA		0.8	
I_I	Input Leakage Current	2.7 to 3.6	V_I = V_{CC} or GND		± 5	µA
$I_{I(HOLD)}$	Input Hold Current	3.0	V_I = 0.8V	75		µA
			V_I = 2V	-75		
		3.6	V_I = 0 to 3.6V		± 500	
I_{off}	Power Off Leakage Current	0	V_I or V_O = 0 to 3.6V		10	µA
I_{OZ}	High Impedance Output Leakage Current	2.7 to 3.6	V_I = V_{IH} or V_{IL} V_O = 0 to 3.6V		± 10	µA
I_{CC}	Quiescent Supply Current	2.7 to 3.6	V_I = V_{CC} or GND		20	µA
			V_I or V_O = V_{CC} to 3.6V		± 20	
ΔI_{CC}	I_{CC} incr. per Input	2.7 to 3.6	V_{IH} = V_{CC} - 0.6V		750	µA

Table 7: DC Specifications ($2.3V < V_{CC} \leq 2.7V$ unless otherwise specified)

Symbol	Parameter	Test Condition		Value		Unit
		V_{CC} (V)		-55 to 125 °C		
				Min.	Max.	
V_{IH}	High Level Input Voltage	2.3 to 2.7		1.6		V
V_{IL}	Low Level Input Voltage				0.7	
V_{OH}	High Level Output Voltage	2.3 to 2.7	I_O=-100 µA	V_{CC}-0.2		V
		2.3	I_O=-4 mA	2.0		
			I_O=-6 mA	1.8		
			I_O=-8 mA	1.7		
V_{OL}	Low Level Output Voltage	2.3 to 2.7	I_O=100 µA		0.2	V
		2.3	I_O=6 mA		0.4	
			I_O=8 mA		0.6	
I_I	Input Leakage Current	2.3 to 2.7	V_I = 0 to 3.6V		± 5	µA
$I_{I(HOLD)}$	Input Hold Current	2.3	V_I = 0.7V	45		µA
			V_I = 1.7V	-45		
I_{off}	Power Off Leakage Current	0	V_I or V_O = 0 to 3.6V		10	µA
I_{OZ}	High Impedance Output Leakage Current	2.3 to 2.7	$V_I = V_{IH}$ or V_{IL} V_O = 0 to 3.6V		± 10	µA
I_{CC}	Quiescent Supply Current	2.3 to 2.7	$V_I = V_{CC}$ or GND		20	µA
			V_I or $V_O = V_{CC}$ to 3.6V		± 20	

Table 8: Dynamic Switching Characteristics (T_a = 25°C, Input $t_r = t_f$ = 2.0ns, C_L = 30pF, R_L = 500Ω)

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 3)	2.5	V_{IL} = 0V $V_{IH} = V_{CC}$		0.25		V
		3.3			0.35		
V_{OLV}	Dynamic Low Voltage Quiet Output (note 1, 3)	2.5	V_{IL} = 0V $V_{IH} = V_{CC}$		-0.25		V
		3.3			-0.35		
V_{OHV}	Dynamic High Voltage Quiet Output (note 2, 3)	2.5	V_{IL} = 0V $V_{IH} = V_{CC}$		2.05		V
		3.3			2.65		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.
2) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the HIGH state.
3) Parameters guaranteed by design.

Table 4: AC Electrical Characteristics (C_L = 30pF, R_L = 500Ω, Input $t_r = t_f$ = 2.0ns)

Symbol	Parameter	Test Condition		Value		Unit
		V_{CC} (V)		-55 to 125 °C		
				Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Dn to Qn	2.3 to 2.7		1.0	5.2	ns
		3.0 to 3.6		0.8	4.0	
t_{PLH} t_{PHL}	Propagation Delay Time LE to Qn	2.3 to 2.7		1.0	5.7	ns
		3.0 to 3.6		0.8	4.2	
t_{PZL} t_{PZH}	Output Enable Time	2.3 to 2.7		1.0	6.2	ns
		3.0 to 3.6		0.8	4.7	
t_{PLZ} t_{PHZ}	Output Disable Time	2.3 to 2.7		1.0	5.1	ns
		3.0 to 3.6		0.8	4.8	
t_s	Setup TIme, HIGH or LOW level Dn to LE	2.3 to 2.7		1.0		ns
		3.0 to 3.6		1.0		
t_h	Hold Time High or LOW level Dn to LE	2.3 to 2.7		1.5		ns
		3.0 to 3.6		1.5		
t_w	LE Pulse Width, HIGH	2.3 to 2.7		1.5		ns
		3.0 to 3.6		1.5		
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note1, 2)	2.3 to 2.7			0.5	ns
		3.0 to 3.6			0.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)

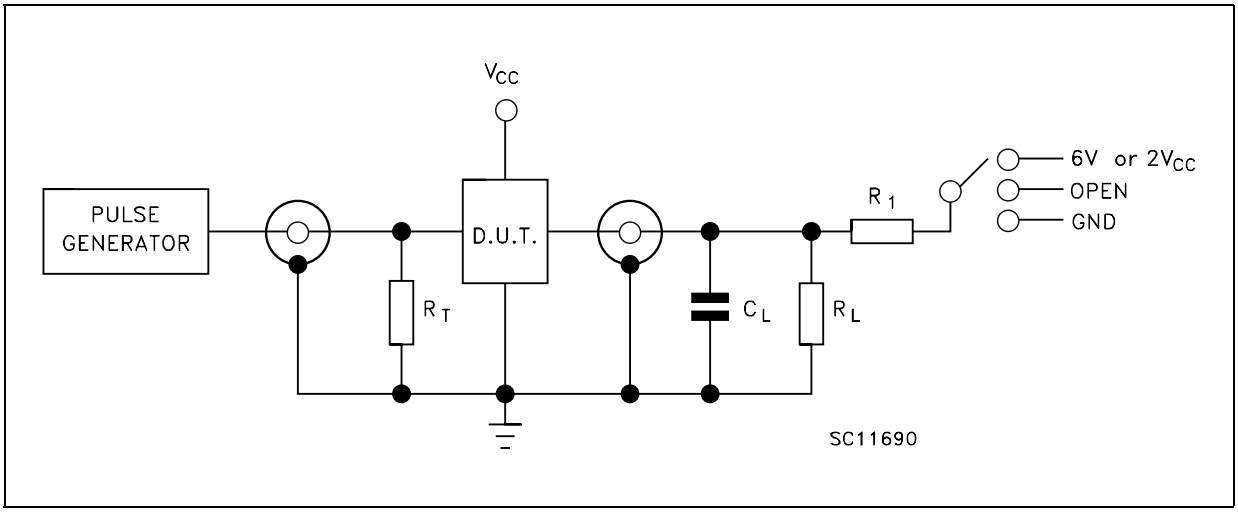
2) Parameter guaranteed by design

Table 9: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance	2.5 or 3.3	V_{IN} = 0 or V_{CC}		6		pF
C_{OUT}	Output Capacitance	2.5 or 3.3	V_{IN} = 0 or V_{CC}		7		pF
C_{PD}	Power Dissipation Capacitance (note 1)	2.5 or 3.3	f_{IN} = 10MHz V_{IN} = 0 or V_{CC}		20		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per circuit)

Figure 5: Test Circuit



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ} (V_{CC} = 3.0 to 3.6V)	6V
t_{PZL}, t_{PLZ} (V_{CC} = 2.3 to 2.7V)	$2V_{CC}$
t_{PZH}, t_{PHZ}	GND

C_L = 30 pF or equivalent (includes jig and probe capacitance)
R_L = R1 = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Table 10: Waveform Symbol Values

Symbol	V_{CC}	
	3.0 to3.6V	2.3 to 2.7V
V_{IH}	2.7V	V_{CC}
V_M	1.5V	$V_{CC}/2$
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V
V_Y	V_{OH} - 0.3V	V_{OH} - 0.15V

Figure 6: WAveform - LE TO Qn Propagation Delays, Le Minimum Pulse Width, Dn To Le Setup And Hold Times (f=1MHz; 50% duty cycle)

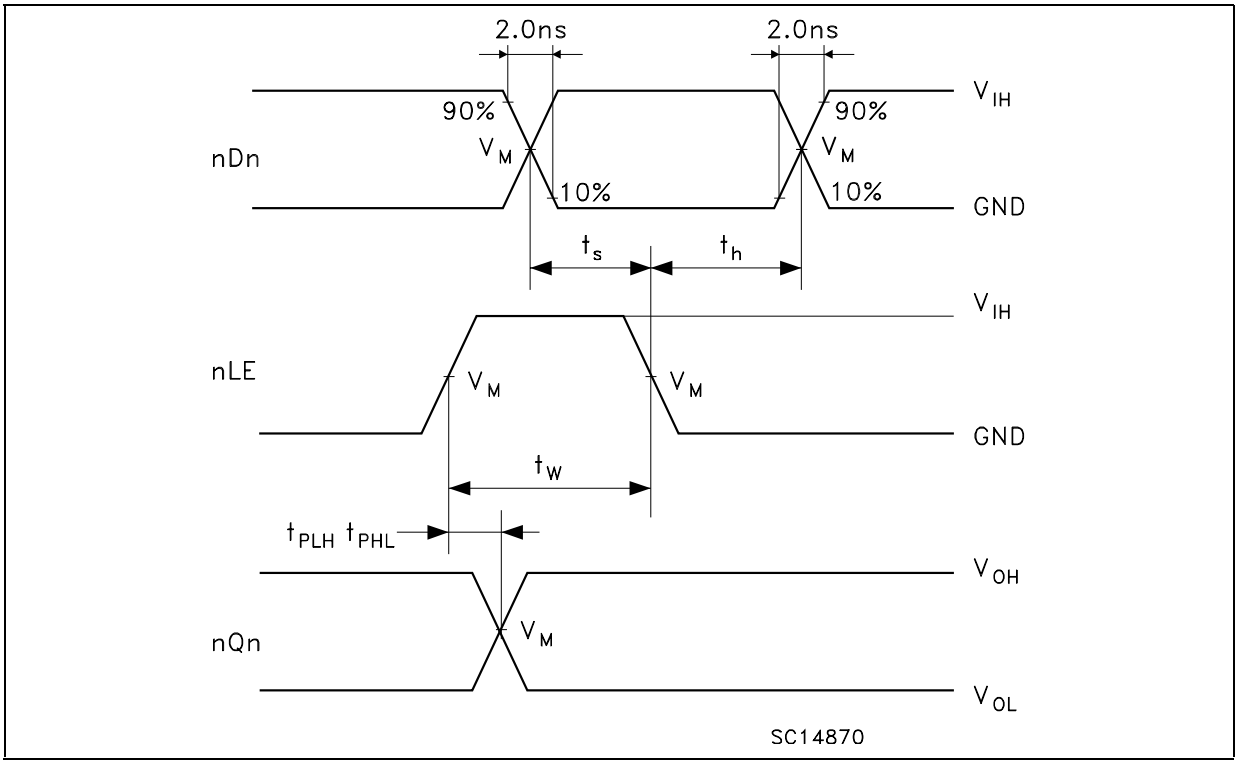


Figure 7: Waveform 2: Output Enable And Disable Time (f=1MHz; 50% duty cycle)

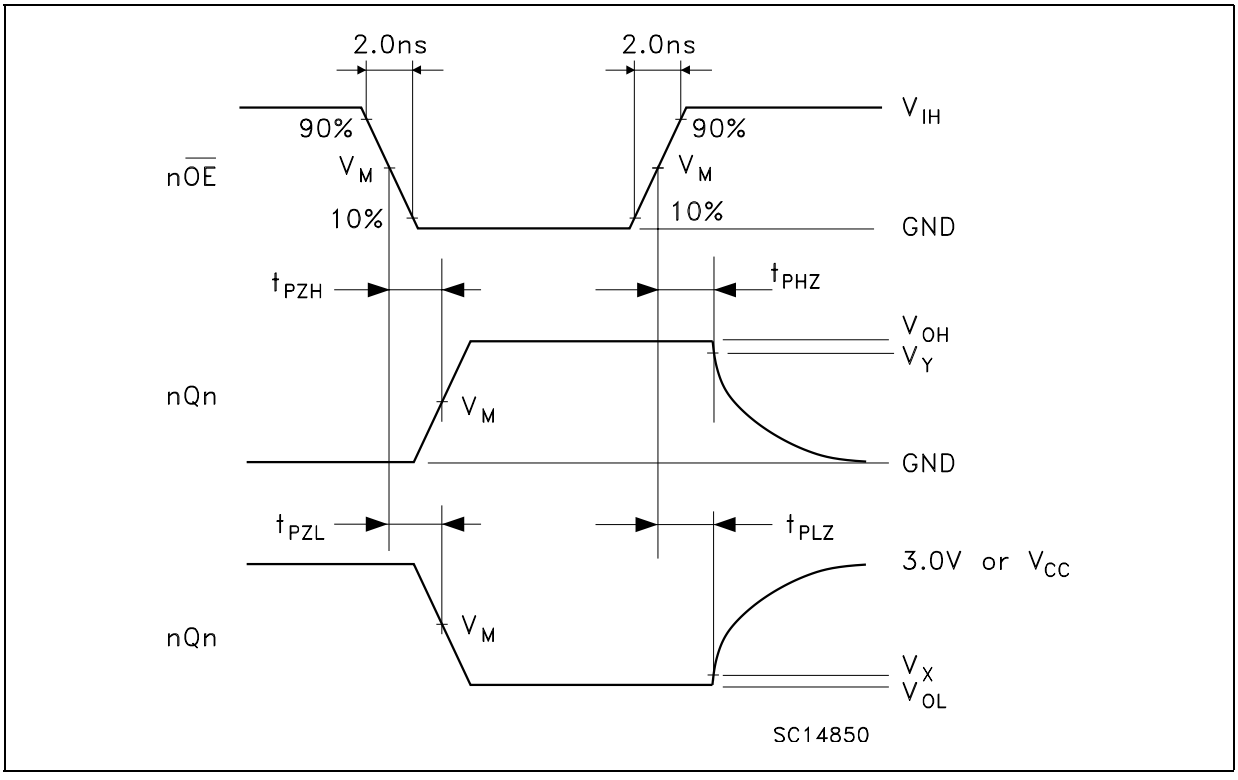
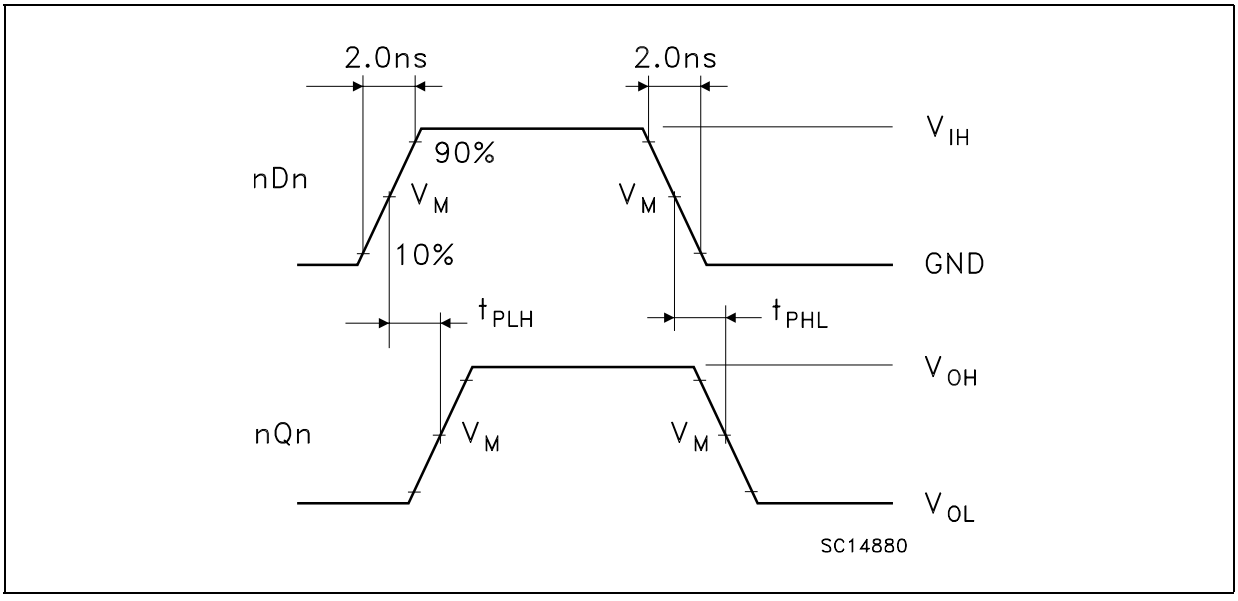


Figure 8: Waveform - Propagation Delay Time (f=1MHz; 50% duty cycle)



FPC-48 (MIL-STD-1835) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.18		2.72	0.086		0.107
b		0.254			0.010	
c		0.15			0.006	
D		15.75			0.620	
E		9.65			0.380	
E2		6.35			0.250	
e		0.635			0.025	
L		8.38			0.330	
Q	0.66		1.14	0.026		0.045
S1		0.13			0.005	

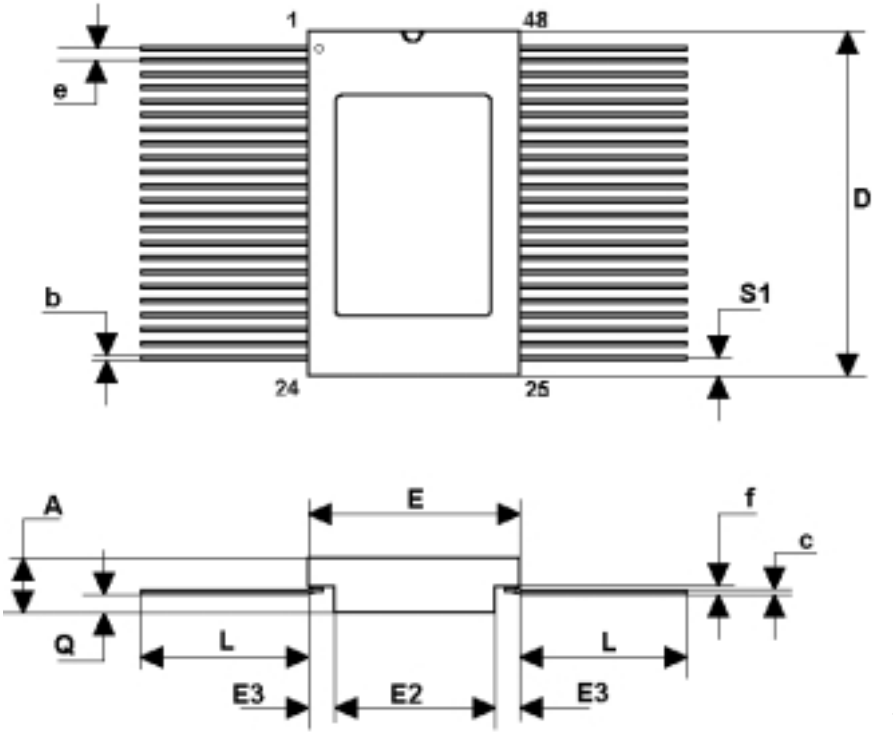


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Table 11: Revision History

Date	Revision	Description of Changes
09-Jul-2004	1	First Release