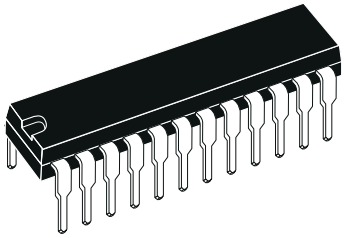
STV9212

Video Processor for CRT Monitors with PictureBooST™

Main Features

- **General**
  - I²C-Bus Controlled
  - Supports AC- and DC-coupled applications
  - 5V to 8V Power Supply
  - Matches to virtually any video amplifier
- **PictureBooST™**
  - PictureBooST™ insertion input
  - Full-screen PictureBooST™ via I²C-bus
  - Context-sensitive Picture Enhancement
- **Video Clamping**
  - Input and Output Video Clamp
  - Sync Pulse Polarity Auto-rectification
  - Clamp Pulse Generation timed either by sync or video blanking pulse
- **Video Processing**
  - Contrast Adjustment with excellent channel matching
  - Gain stages for control of white
  - Two DC-mode cut-off ranges
  - Output DC offset control
  - Automatic Beam Limiter (ABL)
  - Video Insertion Pulse (VIP), 2 levels
  - Amplifier Control (Blanking and Stand-by)
- **OSD Insertion with Contrast Control**
- **Control Output**
  - Amplifier Standby and Blanking Control
  - 3 DAC for control of DC Restore Amplifier or Brightness in DC-coupled system



DIP24S:(Plastic Package)

ORDER CODE: STV9212

General Description

The STV9212 is an I²C-bus controlled color video processor designed for standard CRT monitor applications. It can drive systems where cathodes are either AC- or DC-coupled to the amplifier outputs. The three video channels provide contrast and white balance separate gain adjustments as well as one-per-channel DC cut-off control and common DC offset control functions. On top of these usual controls, it features context-sensitive picture enhancement circuitry to support the PictureBooST™ function that enhances the appearance of still pictures and moving video.

In AC coupling applications, the device can pilot three cathode DC restore channels dedicated to set CRT cut-off bias voltages and to control brightness through cathodes.

The RGB video outputs have a class A architecture and directly drive the amplifier channels without unnecessarily consuming current. Bandwidth limitation I²C-bus adjustments can contribute to keeping the application EMI under control.

OSD (On-Screen Display) graphics are inserted by means of a Fast Blanking signal. Independent OSD contrast control facilitates adaptation to various OSD generators and provides system flexibility.

The STV9212 is perfectly compatible with other ST components for CRT video boards, such as video amplifiers and OSD generators.

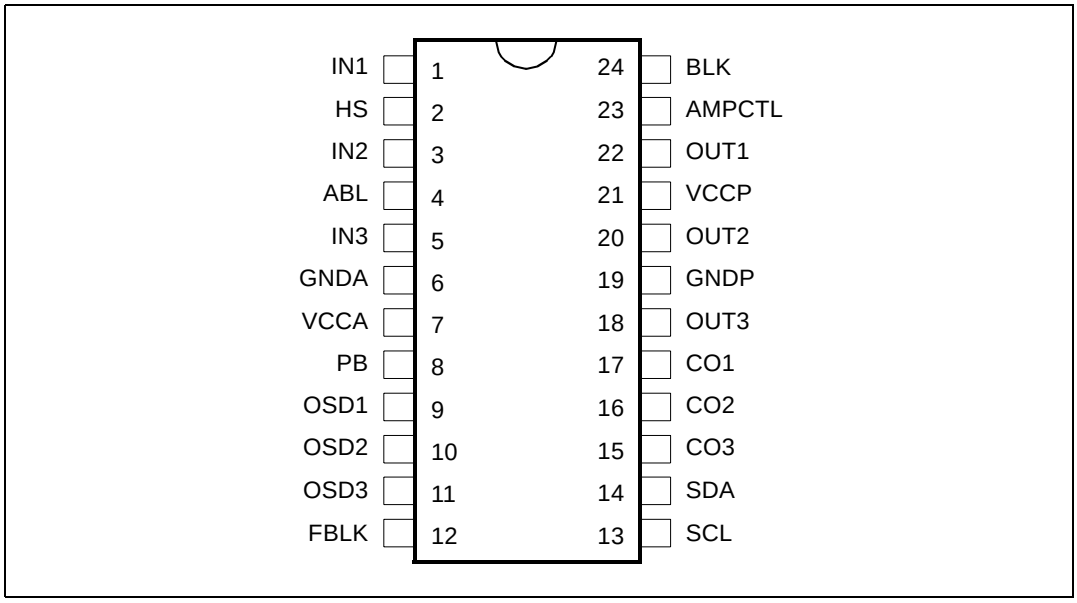
This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Table of Contents

1 STV9212 Pin Allocation and Description

1.1 Pinout

Figure 1: STV9212 Pinout



1.2 Pin Descriptions

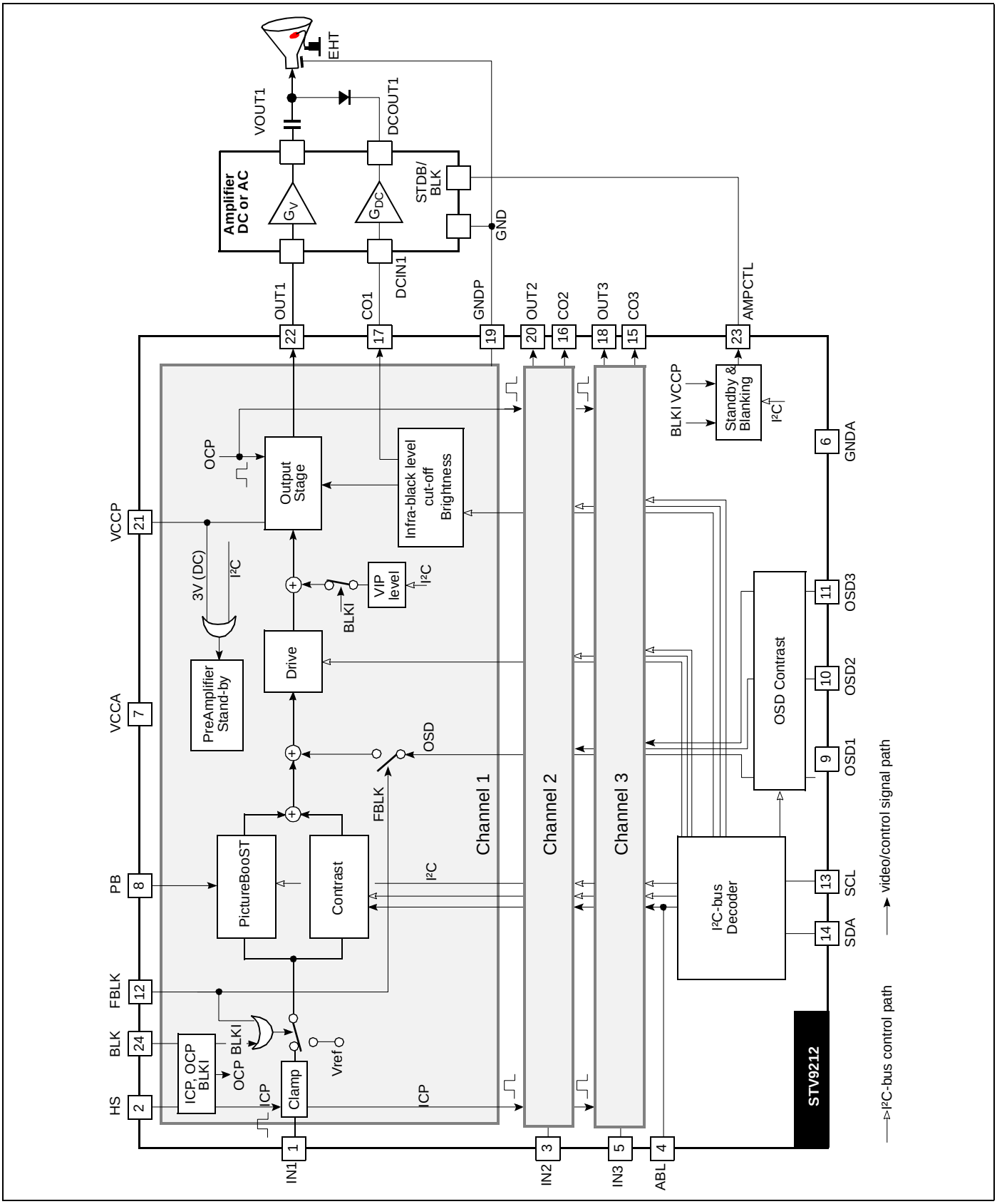
Table 1: STV9212 Pin Descriptions

Pin	Name	Function	Pin	Name	Function
1	IN1	Video Input, Channel 1	13	SCL	I²C-bus Clock Input
2	HS	Video Clamp Sync Input	14	SDA	I²C-bus Data Input/Output
3	IN2	Video Input, Channel 2	15	CO3	Cut-off / Brightness DAC 3 Output
4	ABL	Automatic Beam Limiter Input	16	CO2	Cut-off DAC 2 Output
5	IN3	Video Input, Channel 3	17	CO1	Cut-off DAC 1 Output
6	GNDA	Analog Ground	18	OUT3	Video Output, Channel 3
7	VCCA	Analog Supply	19	GNDP	Output Stage Ground
8	PB	Picture Boost Input	20	OUT2	Video Output, Channel 2
9	OSD1	OSD Input, Channel 1	21	VCCP	Output Stage Supply
10	OSD2	OSD Input, Channel 2	22	OUT1	Video Output, Channel 1
11	OSD3	OSD Input, Channel 3	23	AMPCTL	Output for Amplifier Control
12	FBLK	OSD Insertion Control Input	24	BLK	Blanking and Video Clamp Sync Input

2 Functional Description

The functional blocks are described in the order they act on the signal.

Figure 2: STV9212 Block Diagram



2.1 Video RGB Input Clamp

The three RGB inputs have to be supplied with a video signal through coupling capacitors playing the role of analog memories for internal video clamps. The input clamping level is approximately 0V. The clamp is gated by the Input Clamp Pulse (ICP) that is internally generated from a signal on either the HS or BLK pin. The selection is done via register 8 of the I²C-bus. For more information, refer to Figure 3: ICP, OCP and BLKI Generation and Table 2: ICP Timing.

Provided with an automatic polarity rectification function, the HS input accepts horizontal synchronization signals of either polarity. The device can select either the leading or trailing edge of this signal to trigger the ICP generator.

The BLK input is followed by an inverter stage that can be enabled or by-passed via the I²C-bus. This allows the use of a signal of either polarity, the control software taking care of the inverter position according to the signal applied. The BLKI signal found behind this inverter stage also drives the video blanking circuitry which requires a positive BLKI polarity for correct operation. Once bit *BLKPOL* has correctly been uploaded to ensure a positive BLKI polarity, the ICP triggering edge can be selected via control bit *BCEDGE*. A horizontal flyback pulse is generally expected to be applied on the BLK input. As the edges of horizontal flyback pulse can fall into the active video content (outside the video signal line blanking portion), the application must ensure that such an edge is never selected for triggering the ICP.

The width of the internally generated ICP is controlled via the I²C-bus. The HS input can be used to pass a clamping pulse, if available in the application, directly to clamping stages, without any additional processing. In this case, the appropriate polarity (positive) is required. See Table 2: ICP Timing. The ICP timings triggered by the trailing edge of the BLK signal are not presented.

The Output Clamp Pulse (OCP) is described in Section 2.8: Output Stage.

Figure 3: ICP, OCP and BLKI Generation

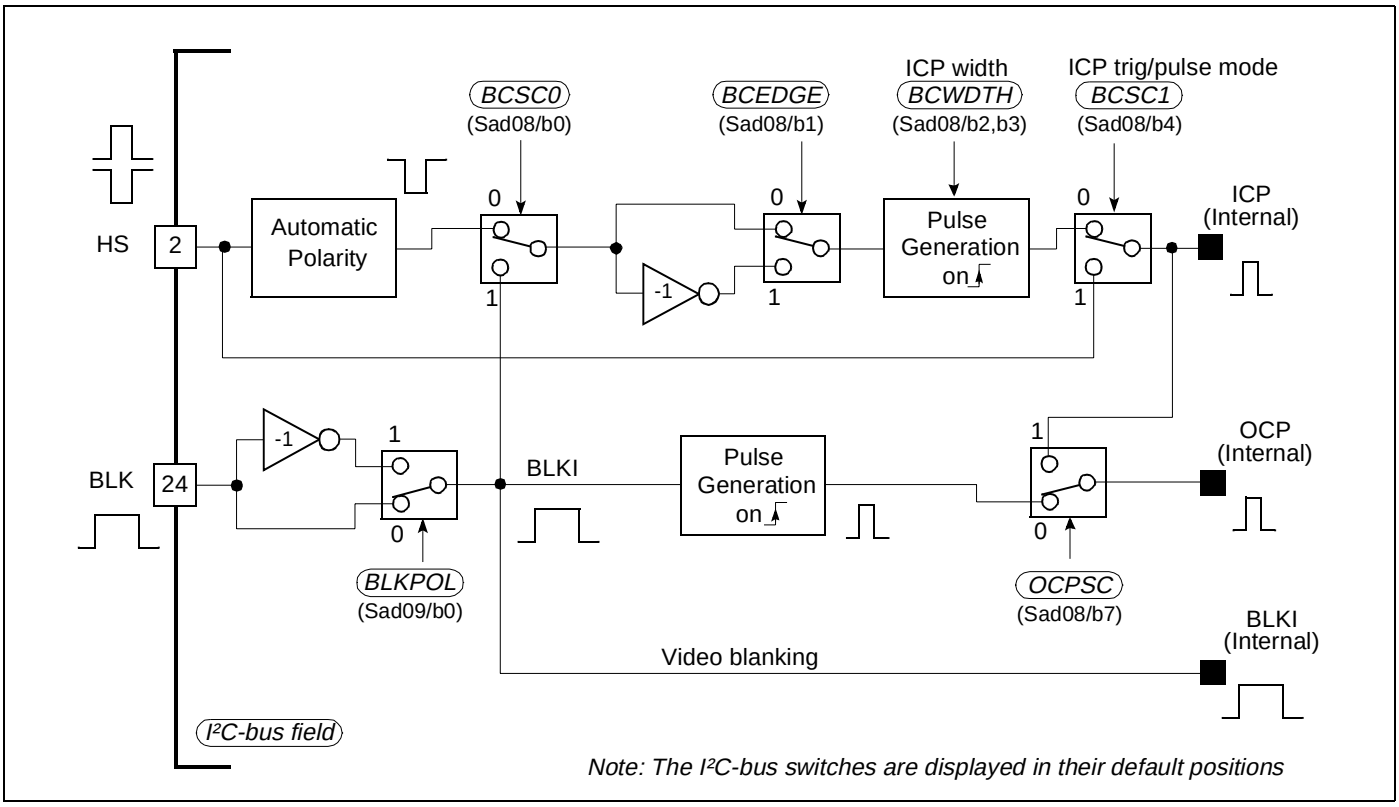


Table 2: ICP Timing

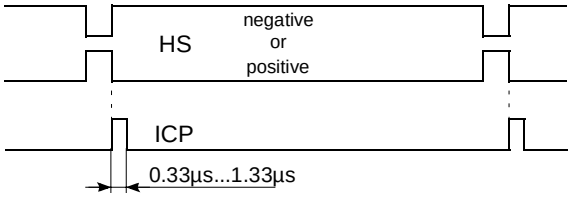
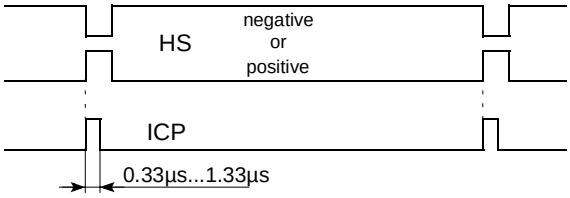
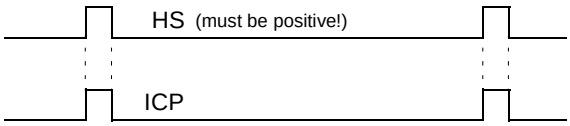
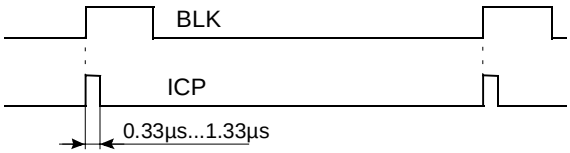
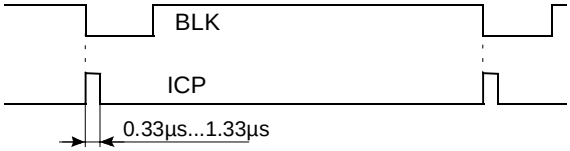
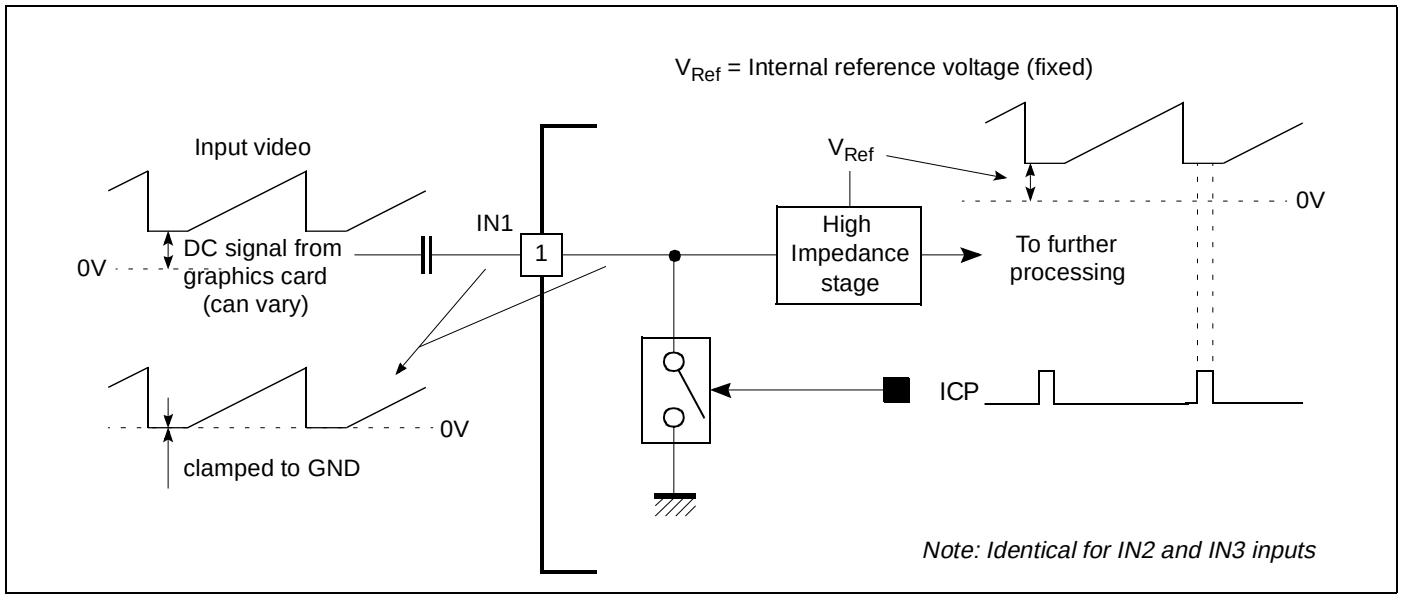
Trigger Source	Trigger Event	*BCSC1*	*BCSC0*	*BCEDGE*	*BLKPOL*	Timing Diagram
HS pin	Trailing edge	0	0	0	Don't care	
	Leading edge	0	0	1	Don't care	
	Pulse	1	Don't care	Don't care	Don't care	
BLK	Rising edge	0	1	0	0	
				1	1	
	Falling edge	0	1	0	1	
				1	0	

Figure 4: Video Input Clamp



2.2 Video Blanking

The three video channels are simultaneously blanked with the high level of either BLKI or FBLK signals. BLKI is an internal signal drawn from the signal applied on the BLK pin (H-flyback) as shown in Figure 3. The blanking consists in forcing a “black” level to the internal clamped video signal.

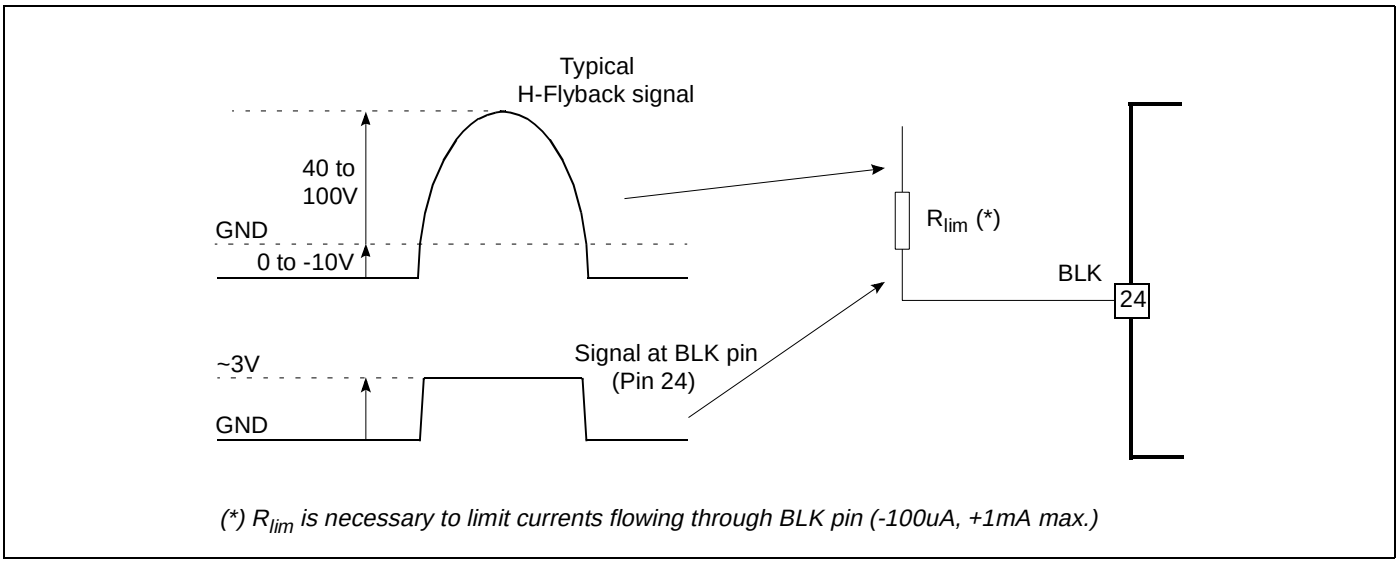
BLK Input

The BLK input receives an H-flyback pulse that drives:

- the video blanking circuitry during scan line retrace,
- the output clamping stage.

A clipping circuit at the input allows the direct use of a high-voltage H-flyback pulse applied through a serial resistor as shown in Figure 5. A logic-level signal is also accepted but the serial resistor remains mandatory. In all cases, the value of this resistor must be such that the sinking and sourcing currents are limited to 1mA and 100µA, respectively.

Figure 5: BLK Input Pin

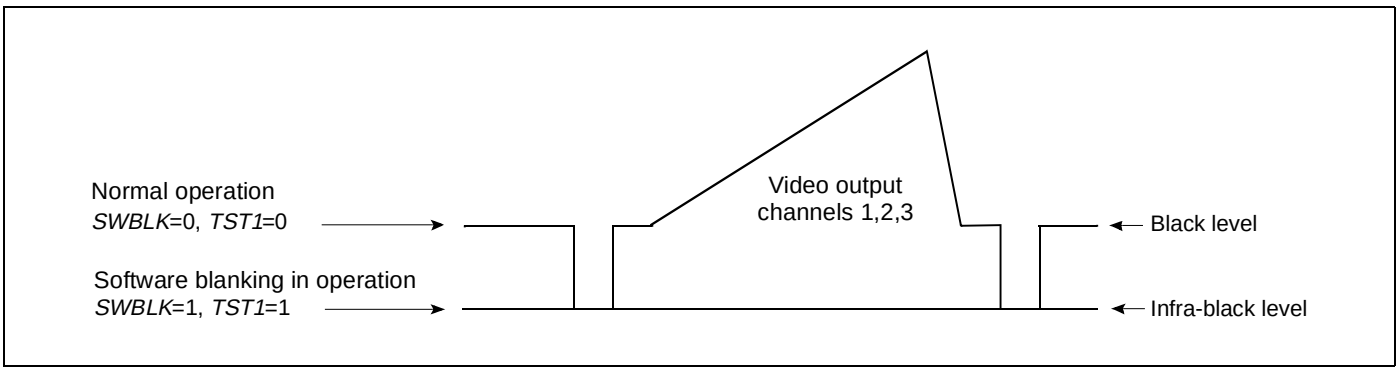


(*) R_{lim} is necessary to limit currents flowing through BLK pin (-100uA, +1mA max.)

Permanent Blanking

The entire TV screen can be blanked for an unlimited amount of time using the software blanking feature. Both bits *SWBLK* and *TST1* must be set to 1. The three video outputs are forced to their infra-black levels as shown in Figure 6. Infra-black levels are defined in Section 2.9.

Figure 6: Software Blanking

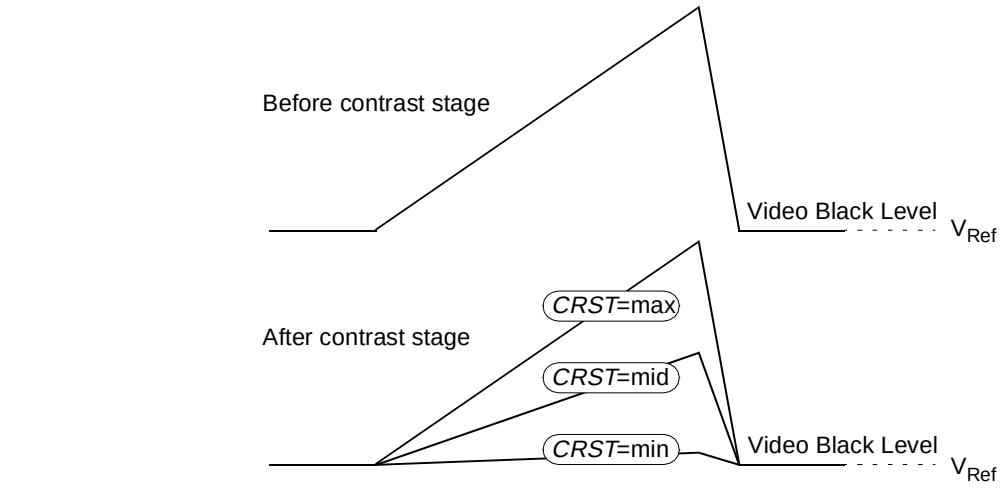


The screen can also be blanked by permanently keeping the On-Screen Display FBLK input signal at high level. In this case, only the video contents of the three video channels are replaced by “black level” OSD content insertion (signals on pins OSD1 through OSD3 permanently at low level). Refer to Section 2.5: OSD Insertion on page 11.

2.3 Contrast Control Stage and Automatic Beam Limiter

The contrast stages are simultaneously controlled on all three RGB channels with high attenuation matching precision. Refer to electrical specifications for values. See Figure 7: Contrast Control and Table 4: I²C-Bus Register Map.

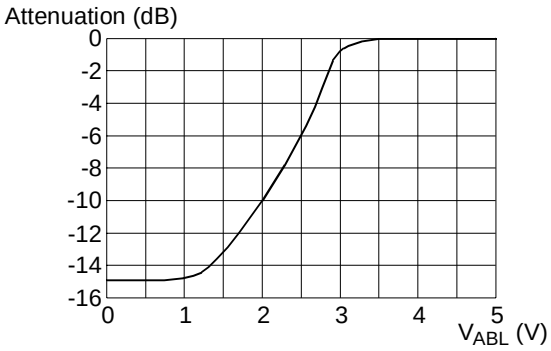
Figure 7: Contrast Control



Note: CRST I²C-bus field acts equally on all 3 video channels

The Automatic Beam Limiter (ABL) is an attenuator controlled through the ABL input, independent of contrast stage attenuation. The operating range is about 2 V (from 3 V to 1 V). A typical characteristic is shown in Figure 8. Refer to Section 4: Electrical Specifications for specific values. When not used, the ABL pin is to be connected to VCCA.

Figure 8: ABL Characteristics



2.4 PictureBooST

The PictureBooST™ function provides a picture enhancement effect for images with photographic or moving video contents.

The function is activated whenever the level on pin PB is high (TTL) or the bit *PBINS* is at 1, if the general PictureBooST™ enable bit *PBGEN* is at 1. By means of PB input signal toggling, the function can take effect in a part of the screen, e.g. a window, or on the whole screen.

The picture enhancement is achieved through combination of three actions, as shown in Figure 9:

- a content-sensitive peaking with slow restore (vivacity),
- a contrast addition,
- a brightness addition.

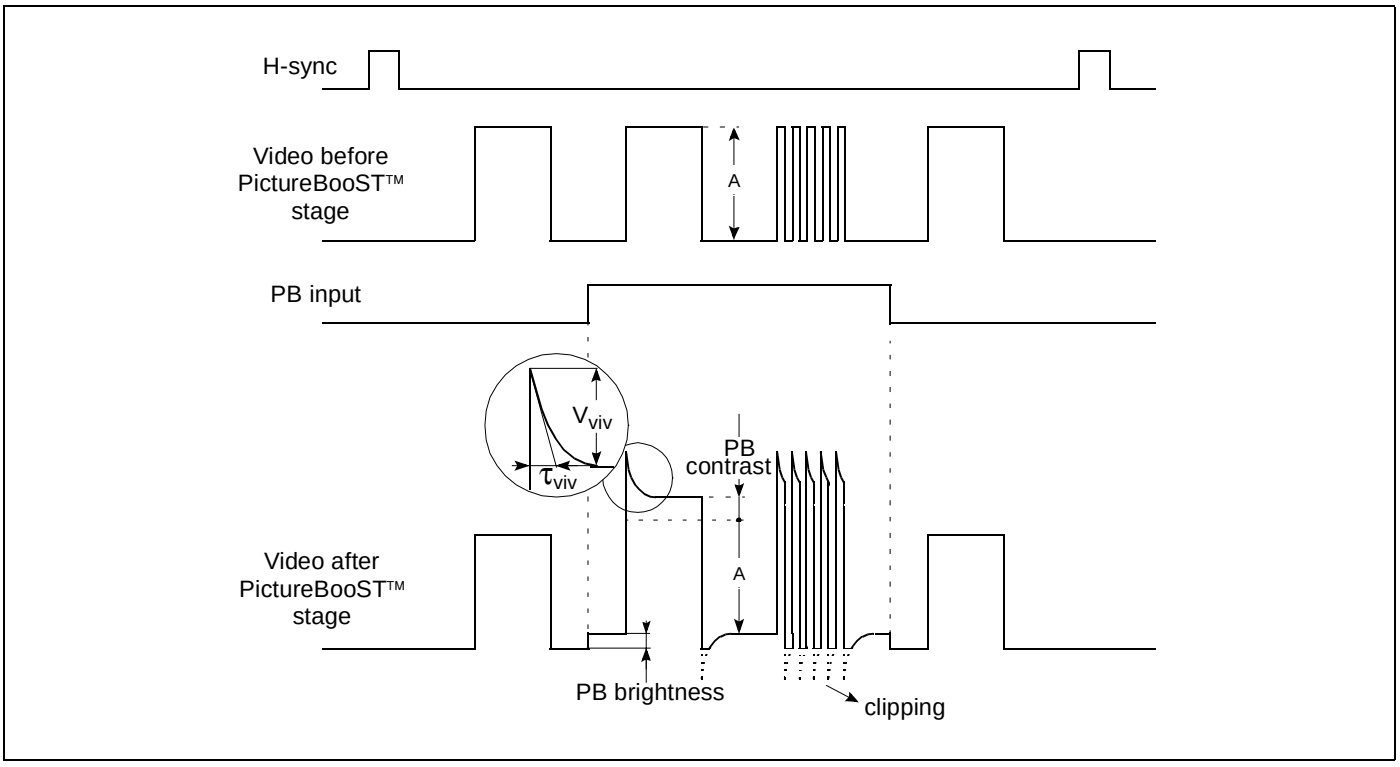
The vivacity amplitude depends on the slope height and steepness and on the status of bits *PBVIVAM[1:0]*. The return to stabilized state is exponential with a time constant adjustable via bits *PBVIVTC[2:0]*. Any undershoot below the video black level is clipped to a level close to black.

The PictureBooST™ brightness is a DC offset superimposed on the video signal in the boosted zone. Its value is selected by bits *PBBRIG[1:0]*. The vivacity and PictureBooST™ brightness are both enabled by bit *PBVIVEN*.

The PictureBooST™ contrast component evenly increases the video amplitude in the boosted zone. Its value is controlled by bits *PBCRST[1:0]*.

Refer to Section 4: Electrical Specifications for values.

Figure 9: PictureBooST Action



2.5 OSD Insertion

The On-Screen Display (OSD) is inserted with a high level on the FBLK input (TTL). The device acts as follows:

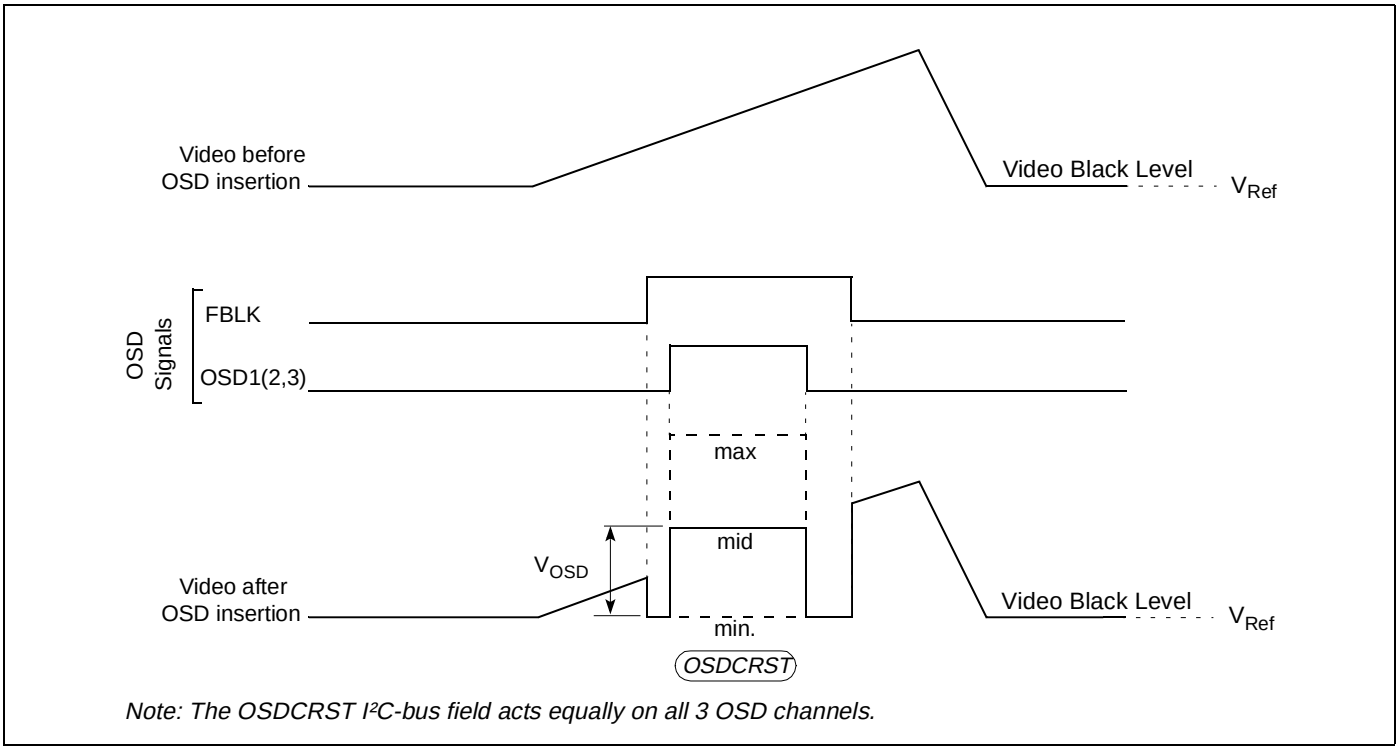
- The three RGB video input signals (IN1, IN2, IN3) are internally blanked, i.e. put at the black level.
- Binary levels (TTL) on inputs OSD1, OSD2 and OSD3, after processing in the OSD contrast stage, are added to the corresponding blanked video channels.

In this way, the OSD contents replace the video contents where the FBLK input is high. See Figure 2 and Figure 10.

The OSD is inserted after the PictureBooST™ block and before the Drive block. As a consequence, OSD insertion overlaps all video contents, including the PictureBooST™-ed zones. Color temperature adjustments by means of the I²C-bus Drive registers act in the OSD insets.

The OSD contrast stage allows the adjustment of the level of OSD insets simultaneously on the three OSD channels and independently of the video contrast adjustment. Refer to Section 4: Electrical Specifications for values.

Figure 10: OSD Insertion

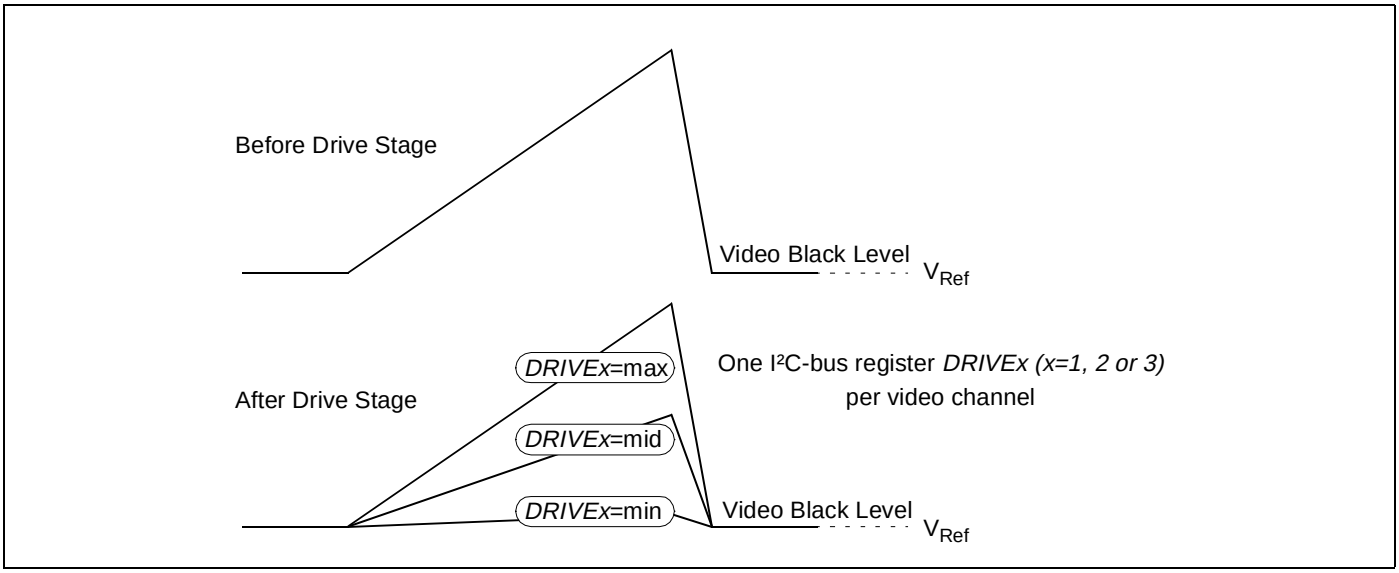


Note: The OSDCRST I²C-bus field acts equally on all 3 OSD channels.

2.6 Drive Stage

The Drive stage is a set of three attenuators separately controlled via three I²C-bus registers, DRIVE1, DRIVE2 and DRIVE3. It affects all signals, ordinary video, PictureBooST™ processed video and OSD insets. It is designed to compensate for differences in gain of the three CRT cathodes. See Figure 11 and for values, refer to Section 4: Electrical Specifications.

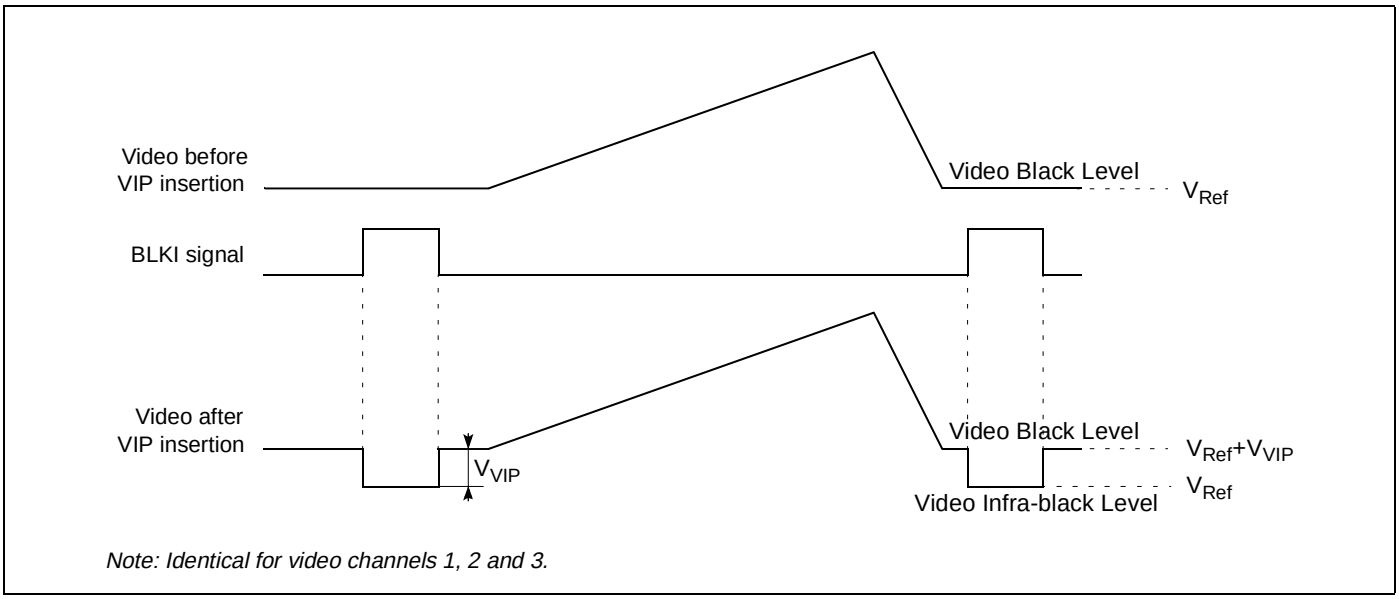
Figure 11: Drive Control



2.7 Video Insertion Pulse

The Video Insertion Pulse (VIP) creates an indent on the three video signals, timed with the positive part of the BLKI signal. (See Section 2.2: Video Blanking on page 8). As its level is below the video black level, it introduces a video “infra-black” level. The video infra-black level position versus ground is then controlled in subsequent stages. In the absence of the blanking pulse on pin BLK, the VIP is not inserted and the subsequent stages control the position of video black level. Figure 12 shows the signal before and after insertion of the VIP. Two different VIP values are programmable by bit *VIP*. Refer to Section 4: Electrical Specifications for values.

Figure 12: VIP Insertion



Note: Identical for video channels 1, 2 and 3.

2.8 Output Stage

The output stage consists of an output clamp and a buffer. If a reduced output video amplitude and/or a reduced infra-black level range is sufficient in the application, the V_{CCP} can be lowered to 5V.

Even at 8V of V_{CCP}, care must be taken at device application level to ensure operation without signal top limitation.

2.8.1 Output Clamp

The DC position of video infra-black and video black levels at the video outputs must be fixed regardless of video or OSD inset contents, especially in applications where the device's output infra-black level determines directly the infra-black level on the CRT cathodes (DC-coupled applications). This fixing is achieved by means of a fully-integrated output clamp that brings the output video infra-black level (video black level, in absence of the BLK pulse) to the level of a variable reference (V_{ib}) as shown in Figure 13. The V_{ib} is described in detail in Section 2.9 on page 15. The clamp circuit is driven by the Output Clamp Pulse (OCP). For correct operation, this pulse must entirely fall into the VIP pulse if this is present (clamp of infra-black level) or onto the video black part (clamp of black level). In the former case, the OCP generator is to be triggered with the leading edge of the BLK pulse, in the latter case it must copy the ICP pulse. Refer to Figure 3 for the OCP generation block diagram. Table 3 shows possible OCP timings. Although possible, the OCP timings, triggered by the BLK trailing edge, are not shown as they have no practical use.

2.8.2 Bandwidth Control

Controlled via bits *BW[3:0]*, the output stage can limit the rise and fall time of the output signal. The optimum choice for this adjustment is highly application dependent. Refer to Section 4: Electrical Specifications for values and to Section 6: Application Hints for practical advice.

2.8.3 Output Buffer

The output buffer provides enough current so that external buffers are not required and the power amplifier can interface directly to the device's outputs.

Figure 13: Output Stage

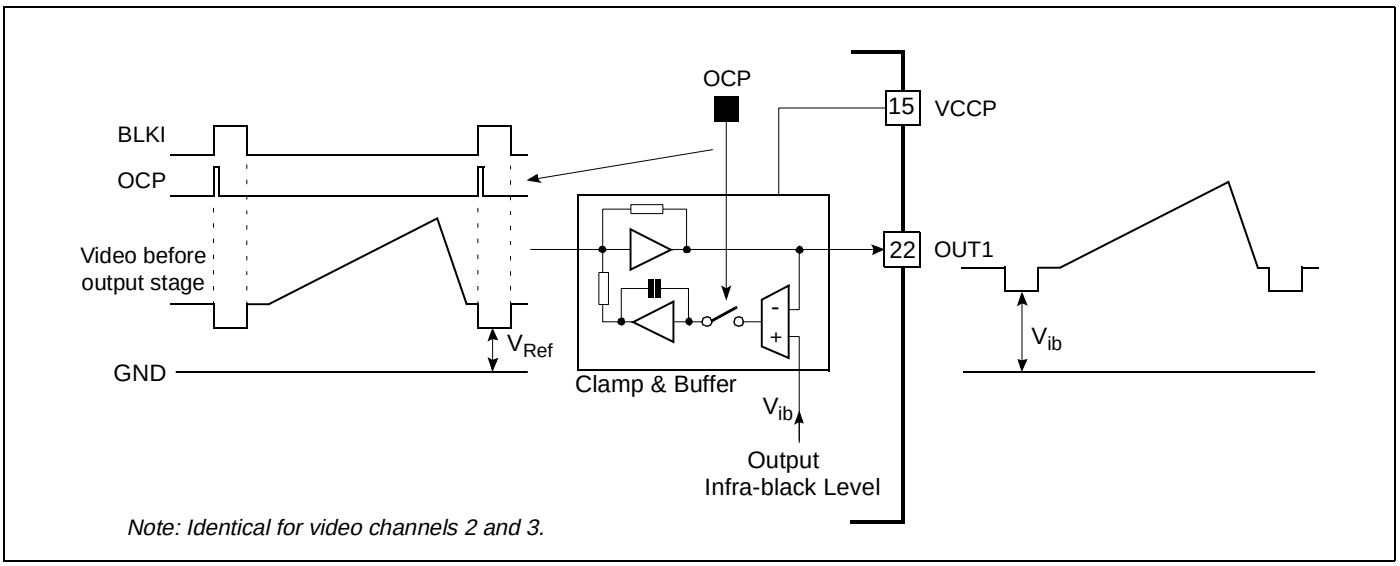
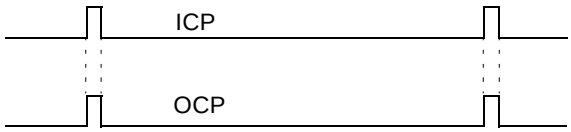
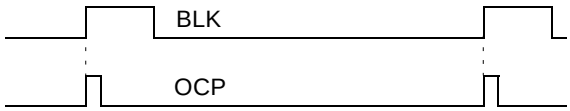


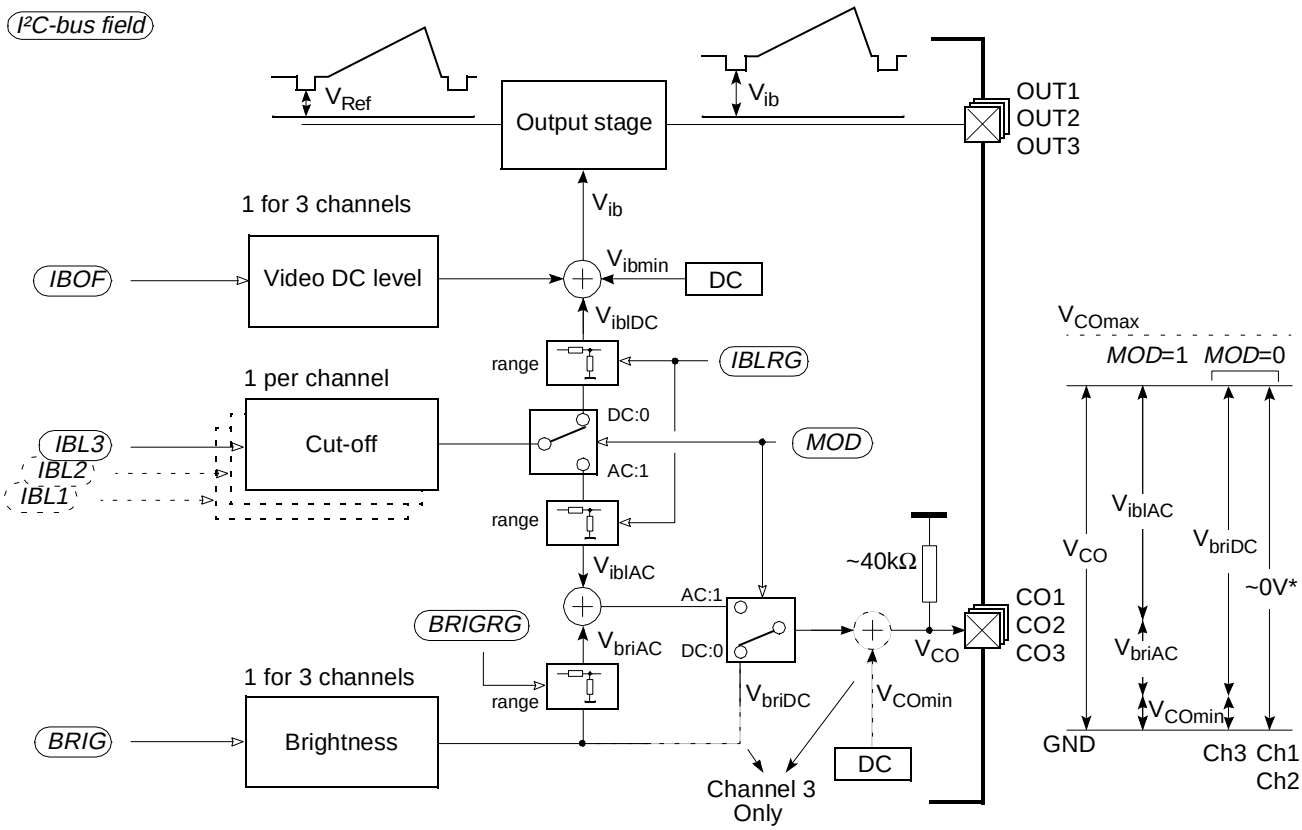
Table 3: OCP Timing

Source	Trigger Event	*OCPSC*	*BLKPOL*	Timing Diagram
ICP	Pulse	1	Don't care	
BLK	Rising edge	0	0	
	Falling edge		1	

2.9 Output Infra-black Level, Cut-off and Brightness

The schematic diagram of these functions is shown in Figure 14.

Figure 14: Cut-off and Brightness Control Block Diagram

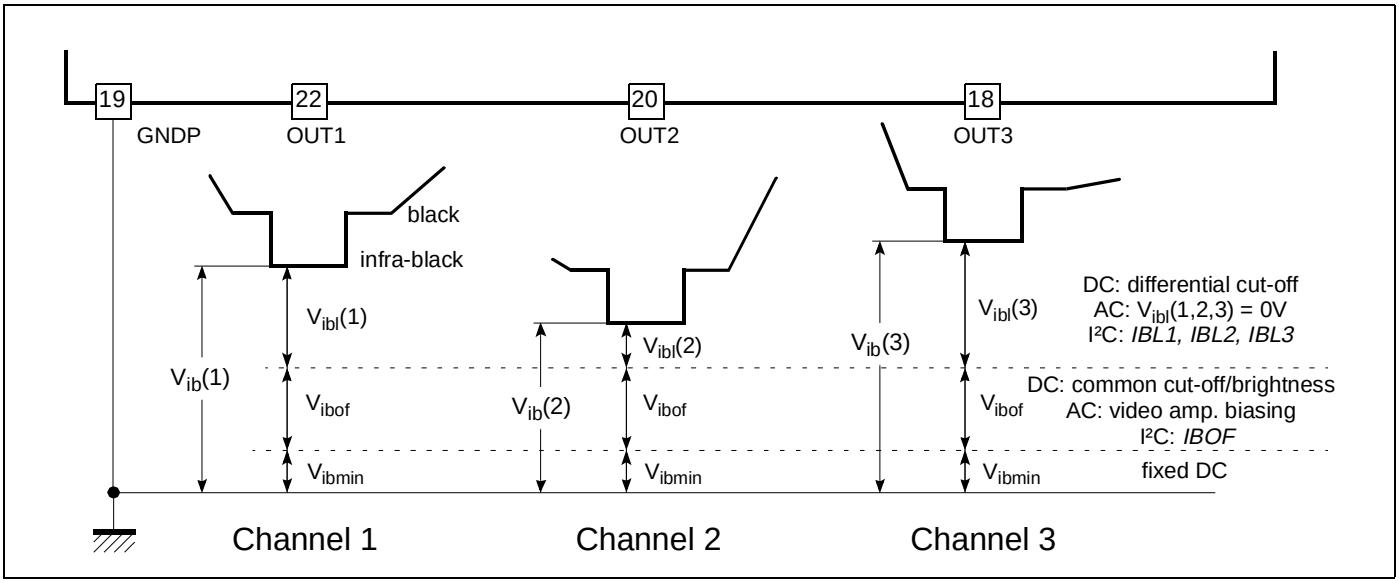


Note: Identical for CO1, CO2 and CO3 outputs except for "brightness" (V_{briDC}) that is only output at CO3 while MOD=0.
The switches are drawn in their default positions.
** ~0V when the output is left open*

2.9.1 Output Infra-black Level

The infra-black level of the video signal at the video outputs OUT1, OUT2 and OUT3 is positioned to the V_{ib} reference by the output clamp circuit, thus defining the Output infra-black level. If the output clamp circuit is furnished with a correctly timed OCP (see corresponding sections), the output infra-black level equals V_{ib}. V_{ib} is composed of a fixed DC voltage (V_{ibmin}), a variable DC voltage (V_{ibof}) applied on all three channels and a per-channel variable DC voltage (V_{ibl} (1,2,3)) as shown in Figure 15. In AC-coupling mode (bit *MOD* = 1), the V_{ibl} part is suppressed and the V_{ib} is therefore equal on all three channels, only varying with bits *IBOF[5:0]* acting on V_{ibof}. This can be used to match the device's outputs to the input of the video amplifier used (biasing). In DC-coupling mode (bit *MOD* = 0), V_{ibl} (1,2,3) are separately set via bits *IBL1[7:0]*, *IBL2[7:0]* and *IBL3[7:0]*, respectively. This serves to adjust the cut-off points of the three CRT cathodes. In this case, V_{ibof} can serve to pre-position the cut-off ranges in the factory adjustment procedure or/and to provide a rough brightness control.

Figure 15: Output Infra-black Level

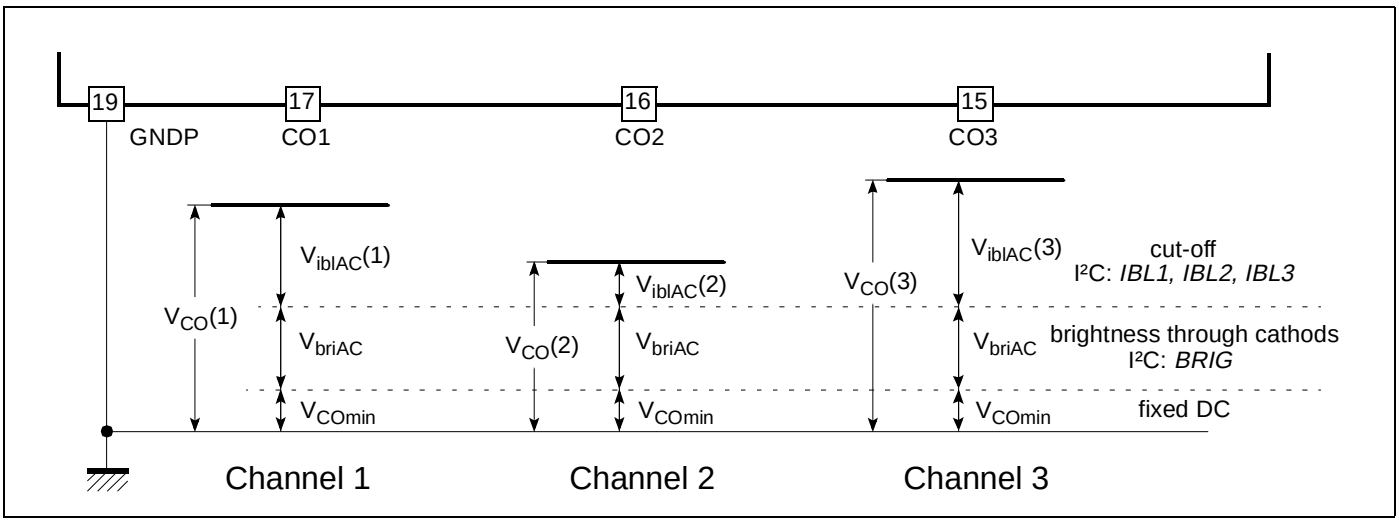


2.9.2 Cut-off and Brightness Control Outputs

Outputs CO1, CO2 and CO3 provide a DC voltage controlled via bits *BRIG[7:0]*, *IBLx[7:0]*, *IBLRG[7:0]*, *BRIGRG[1:0]* and *MOD[7:0]*. The principal of operation is shown in Figure 14.

When bit *MOD* is in position AC (= 1), the output voltage is a sum of the “brightness” V_{briAC}, “cut-off” V_{iblAC} and a fixed V_{COmin} providing a bottom limitation. The brightness adjustment is equally applied to all three CO1, CO2 and CO3 outputs. It varies depending on bits *BRIG[7:0]* and *BRIGRG[1:0]*, with bits *BRIGRG[1:0]* controlling the range of BRIG adjustment. The cut-off adjustment is separate for each channel, having one I²C-bus field per channel: *IBL1*, *IBL2* and *IBL3*. The ratio between the brightness and cut-off ranges depends on the brightness range selection. See Figure 16.

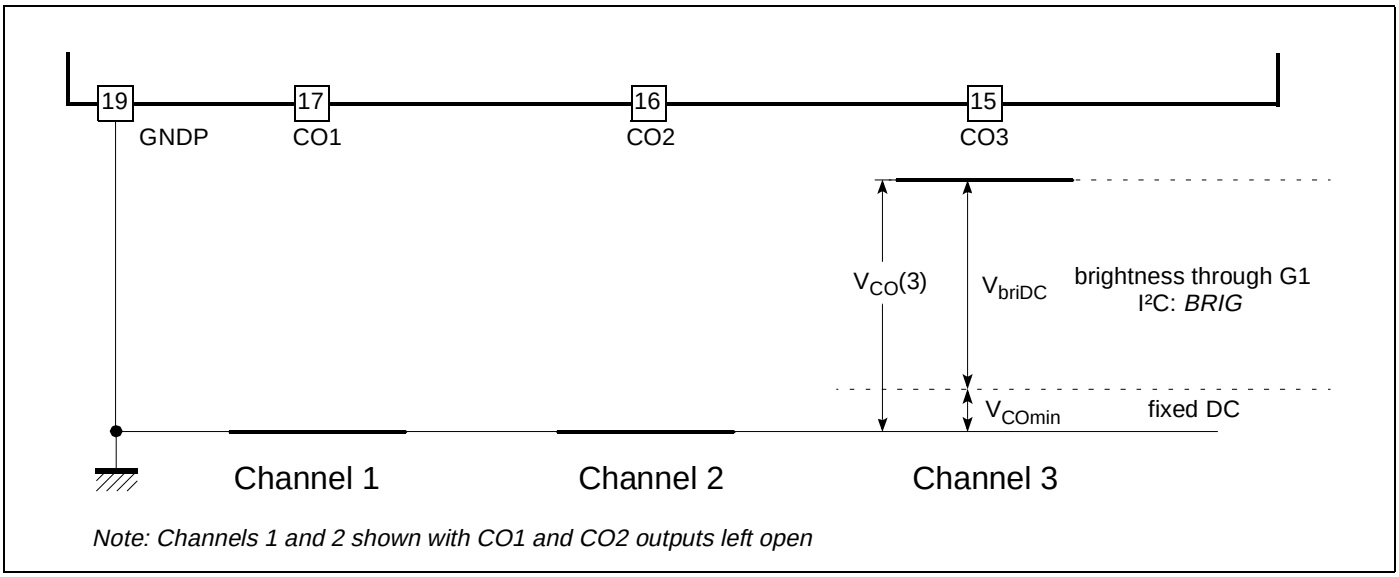
Figure 16: CO1, CO2 and CO3 Outputs while MOD = 1



When bit *MOD* is in position DC (= 0), the output voltage on CO3 output is a sum of the “brightness” V_{briDC} and a fixed V_{COmin} providing a pedestal. Outputs CO1 and CO2 are floating with internal

resistors of approximately 40 kΩ to ground. The V_{briDC} varies with bits *BRIG[7:0]* and does not depend on bits *BRIGRG[1:0]*. See Figure 17.

Figure 17: CO1, CO2 and CO3 Outputs while MOD = 0

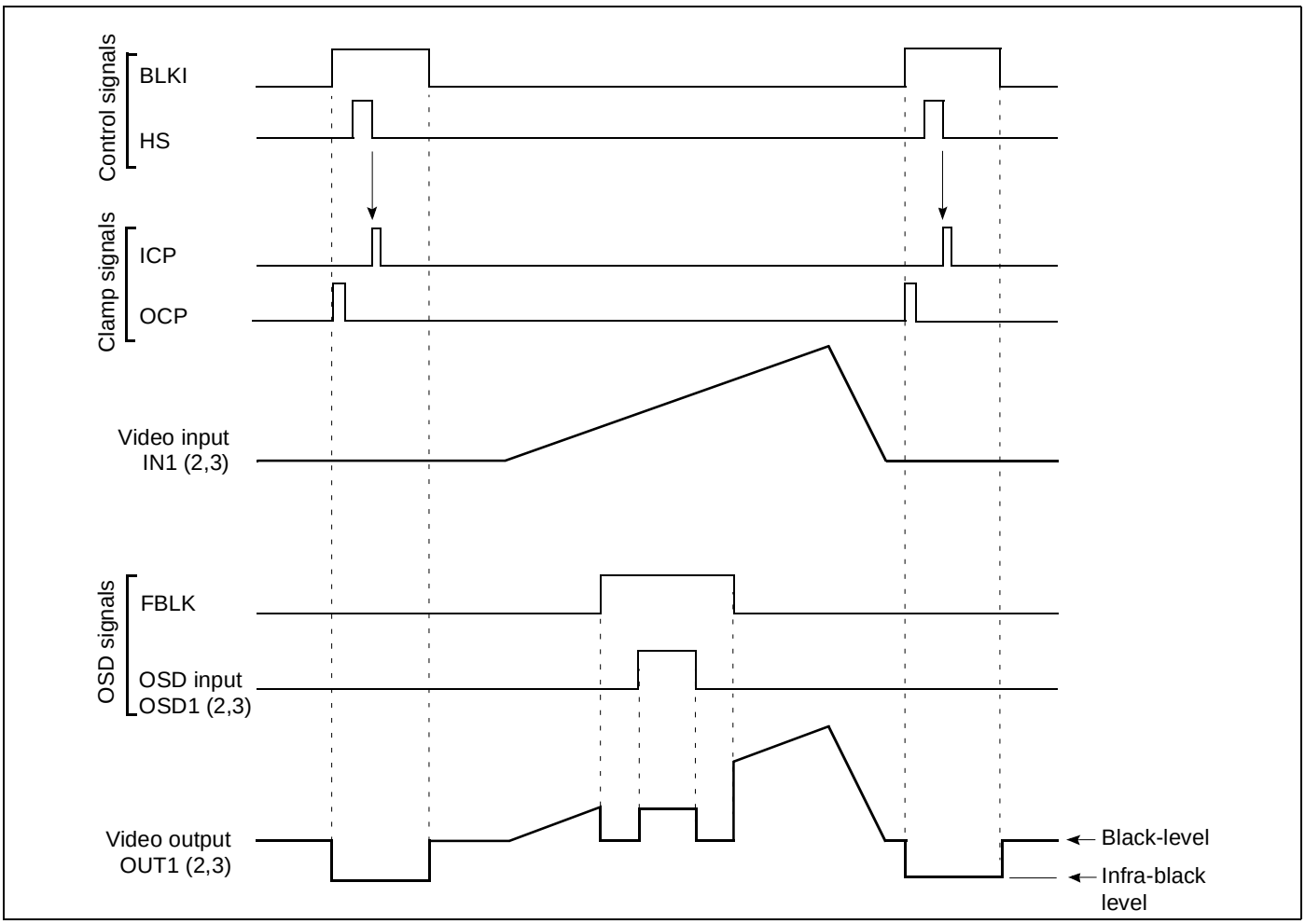


Note: Channels 1 and 2 shown with CO1 and CO2 outputs left open

2.10 Signal Waveforms

Figure 18 gives a summary of main signals waveforms.

Figure 18: Signal Waveforms



2.11 Miscellaneous

2.11.1 Stand-by Mode

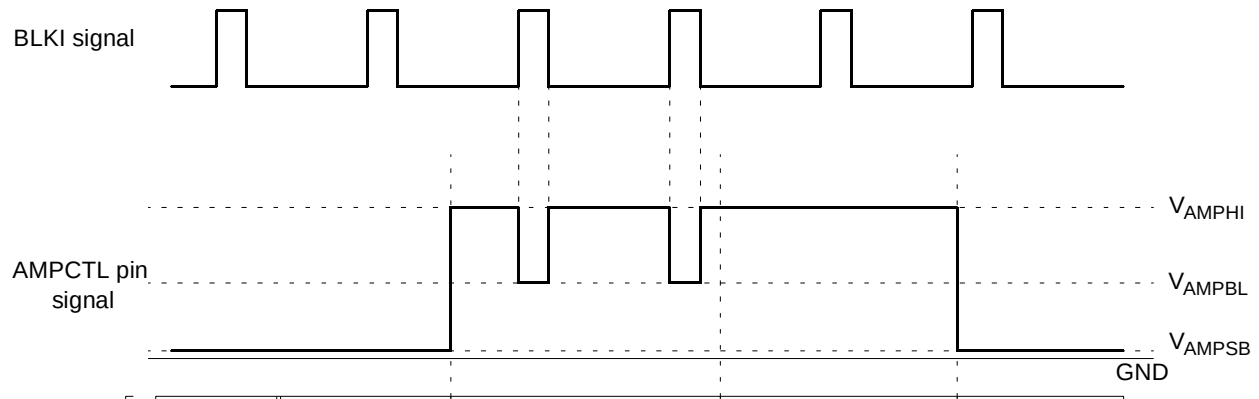
The device is set in Stand-by mode either by means of bit *PASTBY* or by lowering the V_{CCP} supply voltage below the V_{CCPS} threshold. Once in Stand-by mode, the device does not process the video signal and its power consumption is significantly reduced. The I²C-bus interface remains operational. A low level is forced on the AMPCTL output. Refer to Section 4: Electrical Specifications for values.

2.11.2 AMPCTL Output

The AMPCTL is designed to control a video power amplifier. It provides a three-level logical signal that depends on bits *ASTBY* and *ABLEN*, as well as on the operating mode (stand-by / normal) of the device. Figure 19 gives all possible states of the AMPCTL output. Refer to Section 4: Electrical Specifications for electrical parameter values. Pin AMPCTL is of push-pull type. It must not directly

be grounded in the application and it can be left floating. Only video amplifiers provided with an appropriate control input can take advantage of the signal on the AMPCTL output.

Figure 19: AMPCTL Output States



I²C-bus bits					
ASTBY	X	1	0	0	X
PASTBY	1	X	0	0	X
ABLEN	X	X	1	0	X
V_{CCP}	$>V_{STBTH}$		$>V_{STBTH}$	$>V_{STBTH}$	$<V_{STBTH}$

Note: X stands for "don't care" value

3 I²C-Bus Interface Specifications

The device is compatible to general I²C-bus specification. Its slave write address is DCh. Subaddress (Sad) auto-incrementing is not available. Only Write mode is supported. The control register map is given in Table 4.

Bold weight denotes default values assumed at power-on reset. The power-on reset is effected every time that the supply voltage on VCCA pin drops below V_{PORTH} threshold (Refer to electrical specifications).

In order to ensure compatibility with future devices, all “Reserved” bits are to be set to 0 once uploaded by the control software.

Table 4: I²C-Bus Register Map

Sad	b7	b6	b5	b4	b3	b2	b1	b0
01	*CRST*							Reserved
	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**
02	*BRIG*							
	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**
03	*DRIVE1*							Reserved
	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**
04	*DRIVE2*							Reserved
	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**
05	*DRIVE3*							Reserved
	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**
06	Reserved						*BRIGRG*	
	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**
07	Reserved				*OSDCRST*			
	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**
08	*OCPTG*	*TST1*	*TST0*	*BCSC1*	*BCWDTH*		*BCEDGE*	*BCSC0*
	0:BLK 1:ICP	**0**:Normal 1:Test	**0**:Normal 1:Test	**0**:Trig mode 1:HS pulse	**0**	**1**	**0**:Rising 1:Falling	**0**:HS trig 1:BLK trig
09	*ASTBY*	*ABLEN*	Reserved	*TST2*	Reserved	*MOD*	*SWBLK*	*BLKPOL*
	0:Normal 1:Standby	**0**:Bl. disable 1:Bl. enable	**0**	0:Test **1**:Normal	**0**	**0**:DC 1:AC	**0**:Disable 1:Enable	**0**:Non-inv. 1:Inverted
0A	*IBL1*							
	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0B	*IBL2*							
	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0C	*IBL3*							
	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0D	*PASTBY*	Reserved	*TST4*	*TST3*	*BW*			
	0:Normal 1:Standby	**0**	**0**:Normal 1:Test	**0**:Normal 1:Test	**1**	**0**	**0**	**0**
0E	*VIP*	*IBOF*						*IBLRG*
	0:0.2V **1**:0.4V	**1**	**0**	**0**	**0**	**0**	**0**	0:Wide **1**:Narrow
0F	*PBGEN*	*PBINS*	Reserved	*PBCRST*		Reserved	*PBBRIG*	
	0:Disable 1:Enable	**0**:PB Pin 1:Perman.	**0**	**0**	**1**	**0**	**0**	**1**
10	*PBVIVEN*	*PBVIVAM*		Reserved	*PBVIVTC*			Reserved
	0:Disable 1:Enable	**0**	**1**	**0**	**1**	**0**	**0**	**0**

3.1 I²C-bus Register Descriptions

Sad01

Read/Write
Reset Value: 1000 0000 (80h)

7							0
CRST[6:0]							

Values 00 and 7Fh in field *CRST[6:0]* are prohibited.
Bits[7:1] = Contrast Adjustment (*CRST*)
Bit 0 = Reserved

Sad02

Read/Write
Reset Value: 1000 0000 (80h)

7							0
BRIG[7:0]							

Bits[7:0] = Brightness Adjustment *(BRIG)*
In AC mode, this value is added to infra-black levels and output on pins CO1, CO2 and CO3.
In DC mode, it is output all alone on pin CO3.

Sad03

Read/Write
Reset Value: 1000 0000 (80h)

7							0
DRIVE1[6:0]							

Values 00 and 7Fh in field *DRIVE1[6:0]* are prohibited.
Bits[7:1] = Gain Adjustment on Channel 1 (*DRIVE1)*
Bit 0 = Reserved

Sad04

Read/Write
Reset Value: 1000 0000 (80h)

7							0
DRIVE2[6:0]							

Values 00 and 7Fh in field *DRIVE2[6:0]* are prohibited.
Bits[7:1] = Gain Adjustment on Channel 2 (*DRIVE2*)
Bit 0 = Reserved

Sad05

Read/Write
Reset Value: 1000 0000 (80h)

7							0
DRIVE3[6:0]							

Values 00 and 7Fh in field *DRIVE3[6:0]* are prohibited.
Bits[7:1] = Gain Adjustment on Channel 3 (*DRIVE3)*
Bit 0 = Reserved.

Sad06

Read/Write
Reset Value: 0000 0001 (01h)

7							0
						BRIGRG [1:0]	

Bits[7:2] = Reserved.
Bits[1:0]= Brightness Adjustment Range *(BRIGRG)*
Four positions. See Section 4.4: Dynamic Electrical Characteristics.

Sad07

Read/Write
Reset Value: 0000 1001 (09h)

7							0
				OSDCRST[3:0]			

Bits[7:4] = Reserved.
Bits[3:0]= OSD Contrast Adjustment

Sad08

Read/Write
Reset Value: 0000 0100 (04h)

7							0
OCPTG	*TST[1:0]*		*BCSC1*	*BCWDTH[1:0]*		*BCEDGE*	*BCSC0*

Bit 7 = Output clamping pulse selection
0: Pulse triggered by BLK input (default)
1: Internal ICP pulse

Bits[6:5] = Test mode activation for device testing in fabrication. When performing software blanking through *SWBLK* bit, *TST1* bit must be set to 1.
0: Normal operation mode (Default)
1: Test mode

Bits[4,0] = Blanking and clamping pulse source.

BCSC1	*BCSC0*	Selected Source
0	0	HS pin trigger (Default)
0	1	BLK pin trigger
1	Don't care	HS pin pulse

Bits[3:2] = Width of ICP pulse when bit *BCSC1* is 0.

BCWDTH		BCPC Width
0	0	0.33 µs
0	1	0.66 µs (Default)
1	0	1 µs
1	1	1.33 µs

Bit 1 = When HS pin is selected to trigger the ICP pulse generator.
0: Trailing edge of HS pulse (Default)
1: Leading edge of HS pulse

When BLK pin is selected to trigger the ICP pulse generator:

BCEDGE	*BLKPOL*	Trigger on BLK
0	0	Rising edge (default)
0	1	Falling edge
1	0	Falling edge
1	1	Rising edge

Refer to *BLKPOL* bit description.

Sad09

Read/Write
Reset Value: 0001 0000 (10h)

7							0
ASTBY	*ABLEN*		*TST2*		*MOD*	*SWBLK*	*BLKPOL*

Bit 7 = Amplifier standby selection.
0: Normal (default)
1: Standby

Bit 6 = Amplifier blanking enable. The bit is "don't care" whenever bit *ASTBY* is in Standby position.
0: Blanking pulse not generated (default)
1: Blanking pulse generated

Bit 5 = Reserved.

Bit 4 = Test mode activation for device testing in fabrication.
0: Test mode
1: Normal operation mode (Default)

Bit 3 = Reserved.

Bit 2 = Application mode selection.
0: Application with DC-coupled cathodes. (Default)
1: Application with AC-coupled cathodes.

Bit 1 = Permanent blanking of video channels through software.
0: Disable, blanking gated with signal on BLK pin. (Default)
1: Permanent blanking. Bit *TST1* must also be set to 1.

Bit 0 = Blanking signal (H-fly back) polarity inversion. For correct operation, the internal BLKI pulse after this controlled inversion must be positive.
0: Non Inverted, good for positive blanking pulse (Default)
1: Inverted, good for negative blanking pulse

Sad0A, Sad0B and Sad0C

Read/Write
Reset Value: 1000 0000 (80h)

7	0
IBL1[7:0] *IBL2[7:0]* *IBL3[7:0]*	

Bits[7:0] = Infra-black (Cut-off) Level Control, Channels 1 to 3 *(IBLx)*
In DC-coupling mode, the register controls the pedestal of corresponding video channel signal.
In AC-coupling mode, the register controls the level on outputs CO1, CO2 or CO3, respectively.

Sad0D

Read/Write
Reset Value: 0000 1000 (08h)

7			0
PASTBY		*TST[4:3]*	*BW[3:0]*

Bit 7 = Preamplifier and Amplifier STandBY selection
0: Normal (default)
1: Standby

Bit 6 = Reserved.

Bits[5:4] = Test mode activation bits for device testing in fabrication.
0: Normal operation mode (Default)
1: Test mode
Bits[3:0] = Internal band width limitation control. Refer to electrical characteristics.

Sad0E

Read/Write
Reset Value: 1100 0001 (C1h)

7							0
VIP	*IBOF[5:0]*						*IBLRG*

Bit 7 = Video Insertion Pulse depth.
0: 0.2V
1: 0.4V (default)
Bits[6:1] = Infra-black level offset control simultaneously on all three video channels.
Bit 0 = Control range of infra-black level adjustments via *IBL1*, *IBL2* and *IBL3* registers. Acts either on video signal channels or CO1, CO2, CO3 outputs. Refer to electrical characteristics.
0: Wide
1: Narrow (default)

Sad0F

Read/Write
Reset Value: 0000 1001 (09h)

7							0
PBGEN	*PBINS*		*PBCRST[1:0]*			*PBBRIG[1:0]*	

Bit 7 = PictureBooST General Enable. *(PBGEN)*
0: Disable, function inhibited (Default)
1: Enable, function active
Bit 6 = PictureBooST Insertion Control. *(PBINS)*
0: PB pin insertion (Default)
1: Permanent insertion regardless of signal on PB pin
Bit 5 = Reserved.
Bits[4:3] = PictureBooST Contrast Control *(PBCRST)*
Bit 2 = Reserved.
Bits[1:0] = PictureBooST Brightness Control *(PBBRIG)*

Sad10

Read/Write
Reset Value: 0010 1000 (28h)

7							0
PBVIVEN	*PBVIVAM[1:0]*			*PBVIVTC[2:0]*			

Bit 7 = PictureBooST vivacity and brightness enable.
0: Disable (default)
1: Enable
Bits[6:5] = PictureBooST Vivacity Amplitude Control.
Bit 4 = Reserved.
Bits[3:1] = PictureBooST Vivacity Time Constant Control.
Bit 0 = Reserved.

4 Electrical Specifications

4.1 Absolute Maximum Ratings

All voltages refer to the GNDA pin.

Symbol	Parameter	Min.	Max.	Units
V_{CCA}	Supply voltage on VCCA (Pin 7)	TBD	5.5	V
V_{CCP}	Supply voltage on VCCP (Pin 21)	TBD	8.8	V
V_{IN}	Voltage at any pin except video inputs and supply pins	TBD	5.5	V
V_I	Voltage at video inputs (Pins 1,3 and 5)	TBD	1.4	V
V_{ESD}	ESD susceptibility Human Body Model (100 pF discharge through 1.5 kΩ)	TBD	±2	kV
T_{STG}	Storage Temperature	-40	+150	°C
T_{OPER}	Operating Junction Temperature	-40	+150	°C

4.2 Thermal Data

Symbol	Parameter	Min.	Typ.	Max.	Units
R_{thJA}	Junction-to-Ambient Thermal Resistance		60		°C/W
T_{AMB}	Operating Ambient Temperature	0		70	°C/W

4.3 Static Electrical Characteristics

T_{AMB} = 25°C, V_{CCA} = 5V, and V_{CCP} = 8V, unless otherwise specified. All voltages refer to the GNDA pin.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Supply						
V_{CCA}	Supply Voltage	Pin 7	4.5	5	5.5	V
V_{CCP}	Power Stage Supply Voltage	Pin 21	4.5	8	8.8	V
V_{CCPS}	Power Supply Voltage Stand-by Threshold	Pin 21	2.5	3.0	3.5	V
I_{CCA}	VCCA Supply Current	V_{CCA} = 5V (*PBGEN* Disable) V_{CCA} = 5V (*PBGEN* Enable)		65 85		mA mA
I_{CCP}	VCCP Supply Current	V_{CCP} = 8V		50		mA
I_S	Total Supply Current in Stand-by Mode	Pin 21 and pin 7			6	mA
Inputs and Outputs						
V_I	Video Input voltage amplitude			0.7	1	V
V_O	Output voltage swing		0.5(1)		V_{CCP} -0.5V	V
V_{IL}	Low level input voltage (TTL)	OSD, FBLK, PB, HS,BLK			0.8	V
V_{IH}	High level input voltage (TTL)	OSD, FBLK, PB, HS,BLK	2.4			V
I_{IL}	BLK input current	BLK	-0.1		+1.0	mA
I_{IN}	Input current	OSD, FBLK, PB	-1		1	µA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
R_{HS}	Input resistance	HS		40		kΩ
V_{AMPSB}	Output voltage at AMPCTL pin, standby (Figure 18)	I²C-bus bit *ASTBY* = 1 or/and $V_{CCP} < V_{CCPS}$ Sink current 200µA		80	200	mV
V_{AMPBL}	Output voltage at AMPCTL pin, blanking (Figure 18)	I²C-bus bit *ASTBY* = 1 I²C-bus bit *ABLEN* = 1 Sink current 0µA BLKI at high level	TBD	1.6	TBD	V
V_{AMPHI}	Output voltage at AMPCTL pin, no standby, no blanking (Figure 18)	I²C-bus bit *ASTBY* = 0 and $V_{CCP} > V_{CCPS}$ Sink current 0µA		3.1		V

4.4 Dynamic Electrical Characteristics

T_{AMB} = 25°C, V_{CCA} = 5 V, V_{CCP} = 8 V, V_i = 0.7 V_{PP}, C_{LOAD} = 5 pF, R_S = 100 Ω serial resistor between output pin and C_{LOAD}, unless otherwise specified. “x” denotes channel number and can assume values of 1, 2 and/or 3. All voltages refer to the GNDA pin.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Video Output Signal (Pins 18, 20 and 22) - Contrast and Drive						
G	Maximum total gain for video path with PictureBooST off	I²C-bus fields *CRST* = 7Eh, *DRIVEx* = 7Eh *PBGEN = 0*		12		dB
V_{OM}	Maximum video output voltage(2)	I²C-bus fields *CRST* = 7Eh, *DRIVEx* = 7Eh *PBGEN* = 0 *PBGEN* = 1		2.8 4.0		V V
V_{ON}	Nominal video output voltage	I²C-bus fields *CRST* = 40h, *DRIVEx* = 40h (POR state)		TBD		V
CAR	Contrast control range	Max. to min. contrast (*CRST* = 7Eh to *CRST* = 01h)		28		dB
DAR	Drive control range	Max. to min. drive (*DRIVEx* = 7Eh to *DRIVEx* = 01h)		13		dB
GM	Gain matching (3)	I²C-bus fields *CRST* = 40h, *DRIVEx* = 40h (POR state)		±0.1		dB
Video Output Signal - OSD						
V_{OSD}	OSD insertion output level	referenced to output black level *DRIVEx* = 7Eh *OSDCRST* = 0Fh *OSDCRST* = 0h		4.9 0		V V
Video Output Signal - VIP						
V_{VIP}	Video Insertion Pulse level	From Infrablack level to black level *VIP* = 1 *VIP* = 0 (4)		0.4 0.2		Vpp Vpp
Video Output Signal - Infra Black Level (Figure 15)						
V_{ibmin}	Infra black level pedestal			0.4		V
V_{ibof}	Infra black offset component	*IBOF* = 3Fh *IBOF* = 0h		2.1 0		V V
$V_{ibl}[x]$	Infra black level component	*IBLx* = 0h or *MOD* = 1 (AC mode) *IBLx* = FFh, *MOD* = 0 (DC mode) *IBLRG* = 1 *IBLRG* = 0		0 1.3 1.8		V V V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Cut-off Output (Pins CO1, CO2 and CO3)						
V_{COmin}	Pedestal level on COx outputs			0.5		V
V_{COmax}	Upper limitation on COx outputs	Sum of V_{briAC}+V_{iblAC} or V_{briDC} exceeding the limit		V_{CCA} -0.5V		V
V_{briAC}	Brightness component in AC mode (Figure 16)	*MOD* = 1 (AC mode) *BRIG* = 0h *BRIG* = FFh: *BRIGRG* = 00b *BRIGRG* = 01b *BRIGRG* = 10b *BRIGRG* = 11b		 0 0.4 0.8 1.25 1.9		 V V V V V
V_{briDC}	Brightness component in DC mode on CO3 pin(6) (Figure 17)	*MOD* = 0 (DC mode) *BRIG* = 0h *BRIG* = FFh		 0 4		 V V
$V_{iblAC}(x)$	Cut-off component	*MOD* = 0 (DC mode) *MOD* = 1 (AC mode) *IBLx* = 0h *IBLx* = FFh: *IBLRG* = 0 *IBLRG* = 1		0 0 3.7 1.85		V V V V
PictureBooST™ Block (Figure 9)						
G_{PB}	Maximum gain	*PBGEN* = 1 *PBCRST* = 00b *PBCRST* = 01b *PBCRST* = 10b *PBCRST* = 11b		 0.8 1.6 2.3 3		 dB dB dB dB
V_{BriPB}	PictureBooST brightness expressed in equivalent input level	*PBGEN* = 1 and *PBVIVEN* = 1 *PBBRIG* = 00b *PBBRIG* = 01b *PBBRIG* = 10b *PBBRIG* = 11b		 64 48 32 16		 mV mV mV mV
V_{viv}/A	Vivacity amplitude as percentage of its host square pulse level before PictureBooST("A" in Figure 9)	*PBGEN* = 1 and *PBVIVEN* = 1 *PBVIVAM* = 00b *PBVIVAM* = 01b *PBVIVAM* = 10b *PBVIVAM* = 11b		 12.5 25 37.5 50		 % % % %
τ_{viv}	Vivacity time constant	*PBGEN* = 1 and *PBVIVEN* = 1 *PBVIVTC* = 000b *PBVIVTC* = 001b *PBVIVTC* = 111b		 0 35 245		 ns ns ns
ABL (Figure 9)						
G_{ABL}	ABL gain	V_{ABL}>3.2 V V_{ABL} = 1 V		0 -15		dB dB
V_{ThABL}	ABL threshold voltage			3		V
I_{ABL}	ABL input current	V_{ABL} = 3.2V V_{ABL} = 1V		0 -2		µA µA
Video Output Signal - Dynamic Performances (Figure 15)						
t_r, t_f	Rise Time, Fall Time (5)	V_{OUT} = 2V_{PP} (VIP exclusive) *BW* = 0Fh *BW* = 00h		 3.5 7		 ns ns
BW	Large signal bandwidth	V_{OUT} = 2V_{PP}, sinus wave, -3dB *BW* = 0Fh *BW* = 00h		 TBD TBD		 MHz MHz

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
CT	Crosstalk between Video Outputs	$V_{OUT} = 2V_{PP}$ f = 10 MHz f = 50 MHz		 TBD TBD		 dB dB

4.5 I²C-Bus Electrical Characteristics

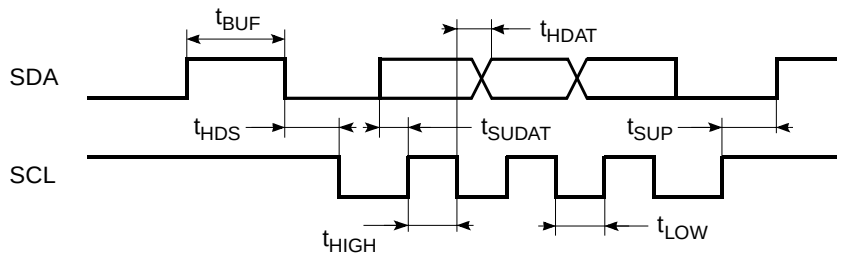
T_{amb} = 25° C, V_{CCA} = 5 V, V_{CCP} = 8 V, V_i = 0.7 V_{PP}, C_{LOAD} = 5 pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Low Level Input Voltage	On Pins SDA, SCL			1.5	V
V_{IH}	High Level Input Voltage		3			V
I_{IN}	Input Current (Pins SDA, SCL)	0.4 V < V_{IN} < 4.5 V	-10		+10	µA
$f_{SCL(Max.)}$	SCL Maximum Clock Frequency			200		kHz
V_{OL}	Low Level Output Voltage	SDA pin when ACK Sink Current = 6 mA			0.6	V

4.6 I²C-Bus Interface Timing Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{BUF}	Time the bus must be free between two accesses	1300			ns
t_{HDS}	Hold Time for Start Condition	600			ns
t_{SUP}	Set-up Time for Stop Condition	600			ns
t_{LOW}	The Low Period of Clock	1300			ns
t_{HIGH}	The High Period of Clock	600			ns
t_{HDAT}	Hold Time Data	300			ns
t_{SUDAT}	Set-up Time Data	250			ns
t_r	Rise Time of both SDA and SCL			1	µs
t_f	Fall Time of both SDA and SCL			300	ns

Figure 20: I²C-Bus Timing Diagram



Notes on Electrical Characteristics

Note 1. The video on the preamplifier output must remain above 0.5V even for high frequency signals.

2. Assuming that the video output signal remains inside the linear area of the preamplifier output (between 0.5V and V_{CCP} - 0.5V).

3. *Matching measured between the different outputs.*
4. *When the Blanking signal is present on the BLK input, the VIP insertion pulse is always generated. Only its amplitude changes (see Figure 12).*
5. *t_R, t_F are simulated values, assuming an ideal input signal with rise/fall time = 0.1 ns. Measured between 10% and 90% of the pulse height.*
6. *When MOD = 0, the CO1 and CO2 are internally grounded through resistors.*

5 Soldering Information

The device can be soldered by wave, dipping or manually. Wave soldering is the preferred method for mounting through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature (T_{STG}[max]). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may last up to 5 seconds.

6 Package Mechanical Data

Figure 21: 24-Pin Plastic Dual In-Line Package, Shrink 300-mil Width

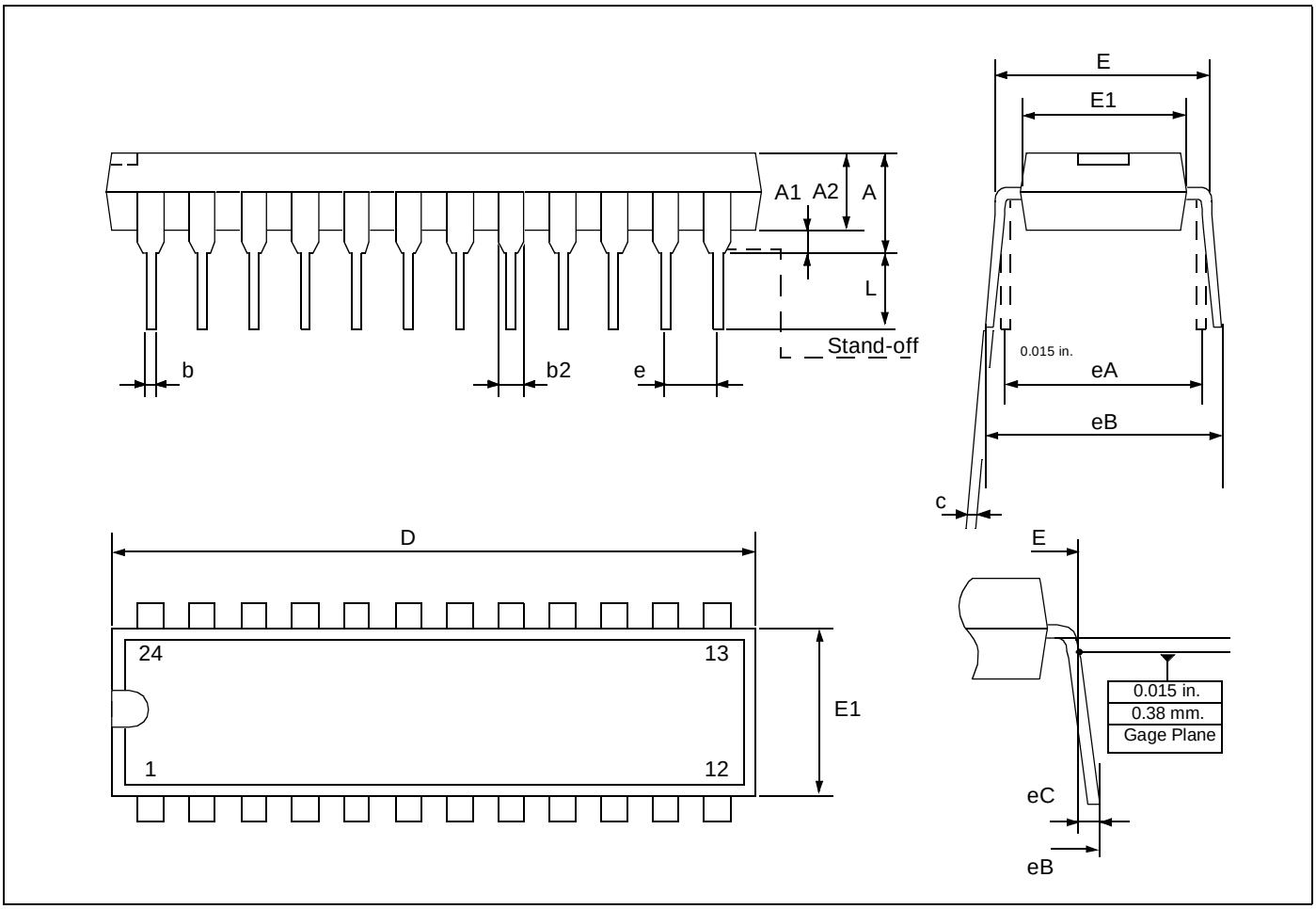
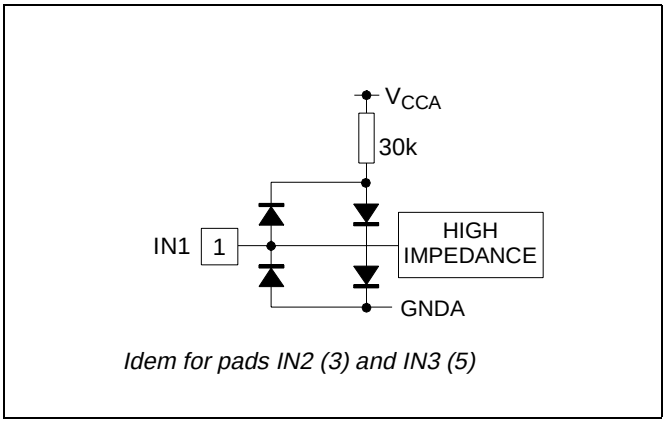


Table 5: Package Dimensions

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.30	4.57	0.120	0.130	0.180
b	0.38	0.46	0.56	0.015	0.018	0.022
b2	0.89	1.02	1.14	0.035	0.040	0.045
c	0.23	0.25	0.38	0.009	0.010	0.015
D	22.35	22.61	22.86	0.880	0.890	0.900
E	7.62		8.64	0.300		0.340
E1	6.10	6.40	6.86	0.240	0.252	0.270
e		1.78			0.070	
eA		7.62			0.300	
eB			10.92			0.430
eC	0.00		1.52	0.000		0.060
L	2.54	3.30	3.81	0.100	0.130	0.150
	Number of Pins					
N	24					

7 Input/Output Diagrams

Figure 22: Video Inputs



Idem for pads IN2 (3) and IN3 (5)

Figure 23: ABL Input

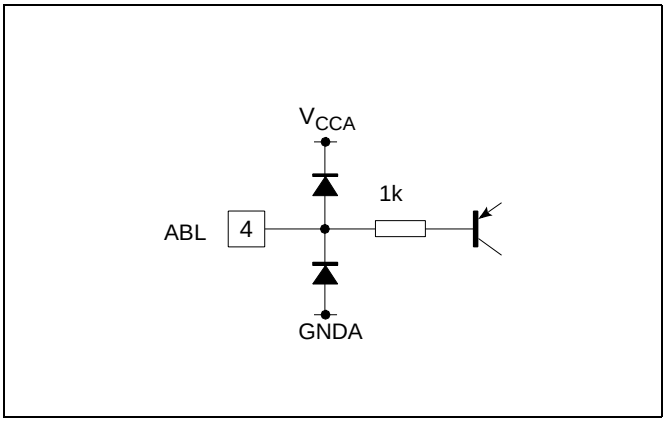


Figure 24: Amplifier Control Output

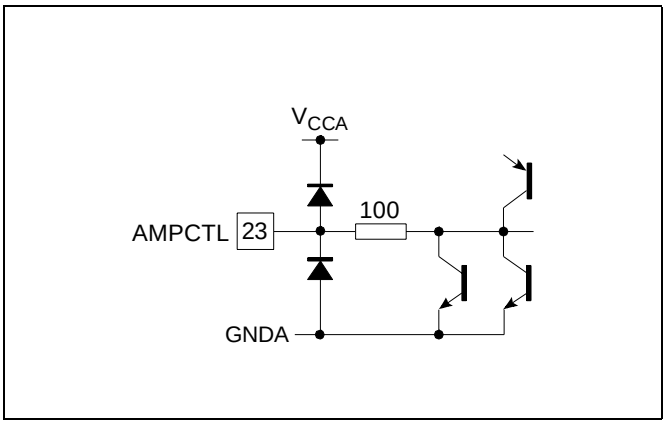


Figure 25: Hsync Input

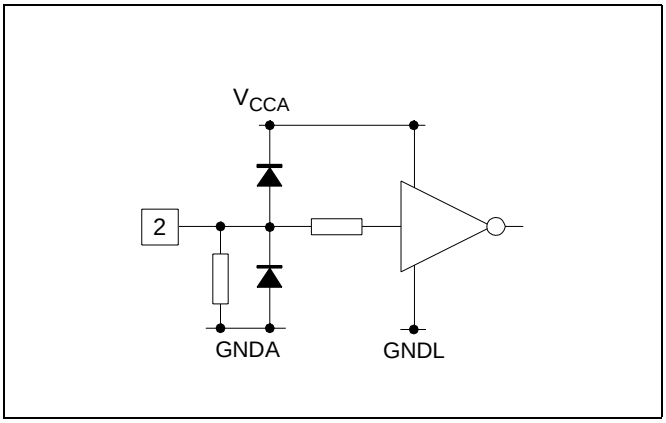
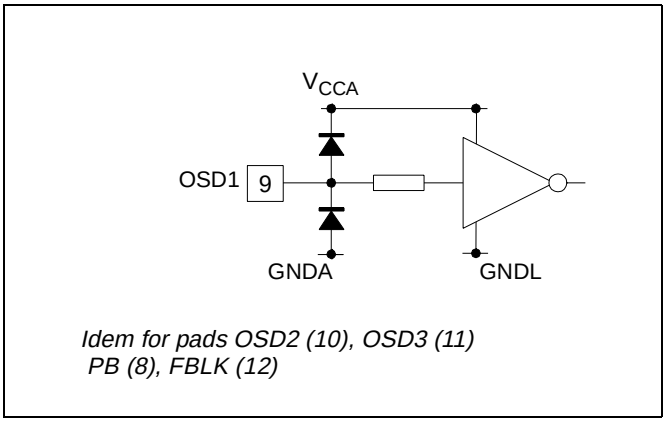


Figure 26: PictureBooST and OSD Inputs



Idem for pads OSD2 (10), OSD3 (11)
PB (8), FBLK (12)

Figure 27: Analog Supplies

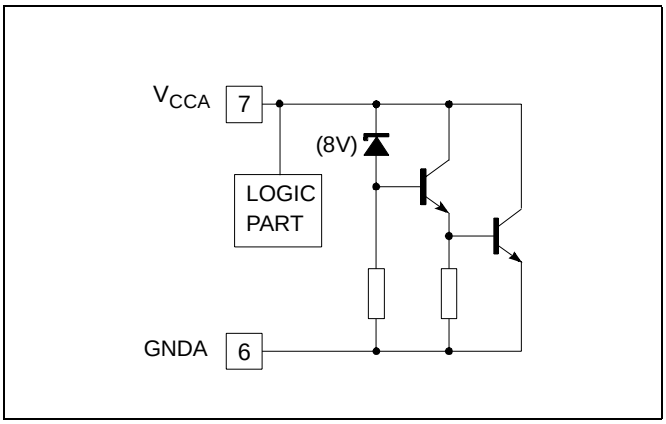


Figure 28: I²C-Bus

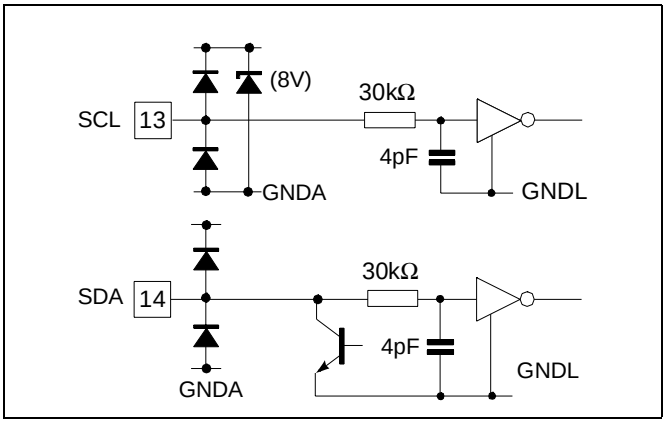
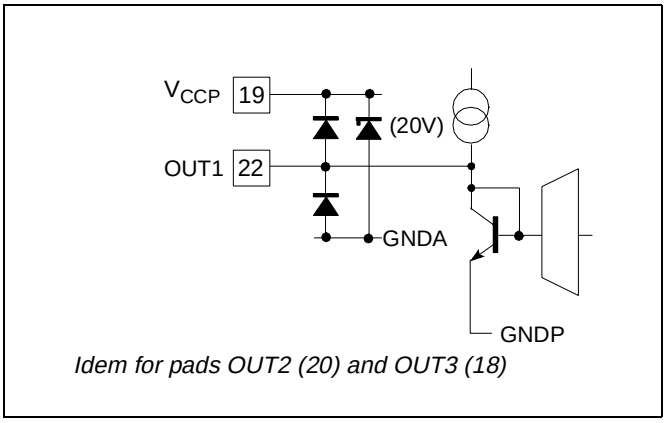


Figure 29: Output Stage Supply and Video Outputs



Idem for pads OUT2 (20) and OUT3 (18)

Figure 30: Blanking / Video Clamping Sync Inputs

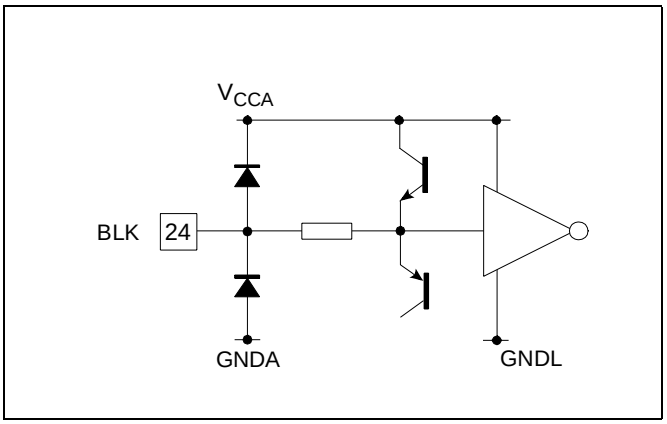


Figure 31: Output Stage Ground

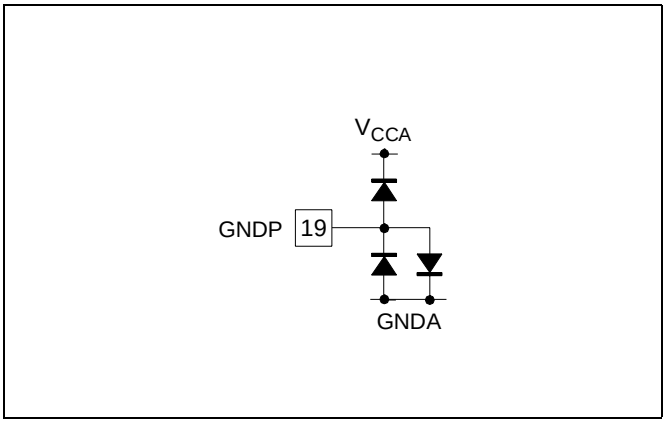
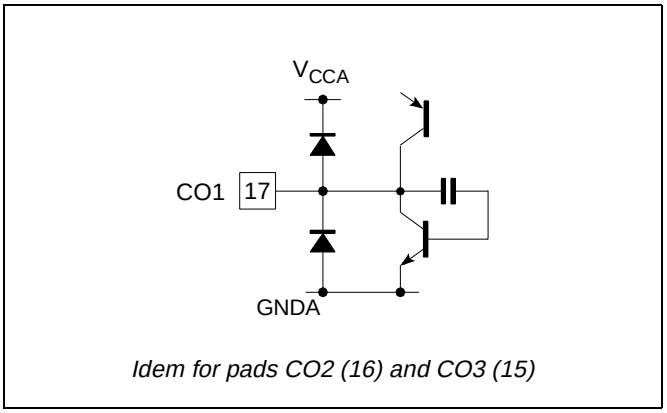


Figure 32: Cut-off DAC Output Pins



Idem for pads CO2 (16) and CO3 (15)

8 Revision History

Table 6: Summary of Modifications

Version	Date	Description
1.0	14 Nov 2002	First Issue
1.1	03 Jul 2003	Minor modifications.

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