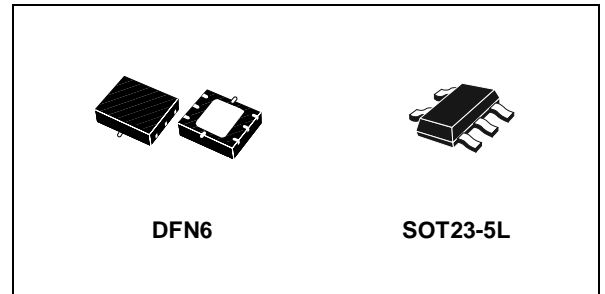


ULTRA LOW DROP-LOW NOISE BICMOS 300mA V.REG. FOR USE WITH VERY LOW ESR OUTPUT CAPACITOR

- INPUT VOLTAGE FROM 2.5V TO 6V
- STABLE WITH LOW ESR CERAMIC CAPACITORS
- ULTRA LOW DROPOUT VOLTAGE (150mV TYP. AT 300mA LOAD, 0.4mV TYP. AT 1mA LOAD)
- VERY LOW QUIESCENT CURRENT (85µA TYP. AT NO LOAD, 200µA TYP. AT 300mA LOAD; MAX 1.5µA IN OFF MODE)
- GUARANTEED OUTPUT CURRENT UP TO 300mA
- WIDE RANGE OF OUTPUT VOLTAGE: 1.25V; 1.35; 1.5V; 1.8V; 2V; 2.1V; 2.2V; 2.5V; 2.6V; 2.7V; 2.8V; 2.85V; 2.9V; 3V; 3.1V; 3.2V; 3.3V; 4.7V
- FAST TURN-ON TIME: TYP. 240µs [$C_O=2.2\mu F$, $C_{BYP}=33nF$ AND $I_O=1mA$]
- LOGIC-CONTROLLED ELECTRONIC SHUTDOWN
- INTERNAL CURRENT AND THERMAL LIMIT
- OUTPUT LOW NOISE VOLTAGE 30µV_{RMS} OVER 10Hz to 100KHz
- S.V.R. OF 55dB AT 1KHz, 50dB AT 10KHz
- TEMPERATURE RANGE: -40°C TO 125°C



It is stable with ceramic and high quality tantalum capacitor. The ultra low drop-voltage, low quiescent current and low noise makes it suitable for low power applications and in battery powered systems. Regulator ground current increases only slightly in dropout, further prolonging the battery life. Shutdown Logic Control function is available, this means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. Typical applications are in mobile phone and similar battery powered wireless systems, portable information appliances.

DESCRIPTION

The LDS3985 provides up to 300mA, from 2.5V to 6V input voltage.

Figure 1: Schematic Diagram

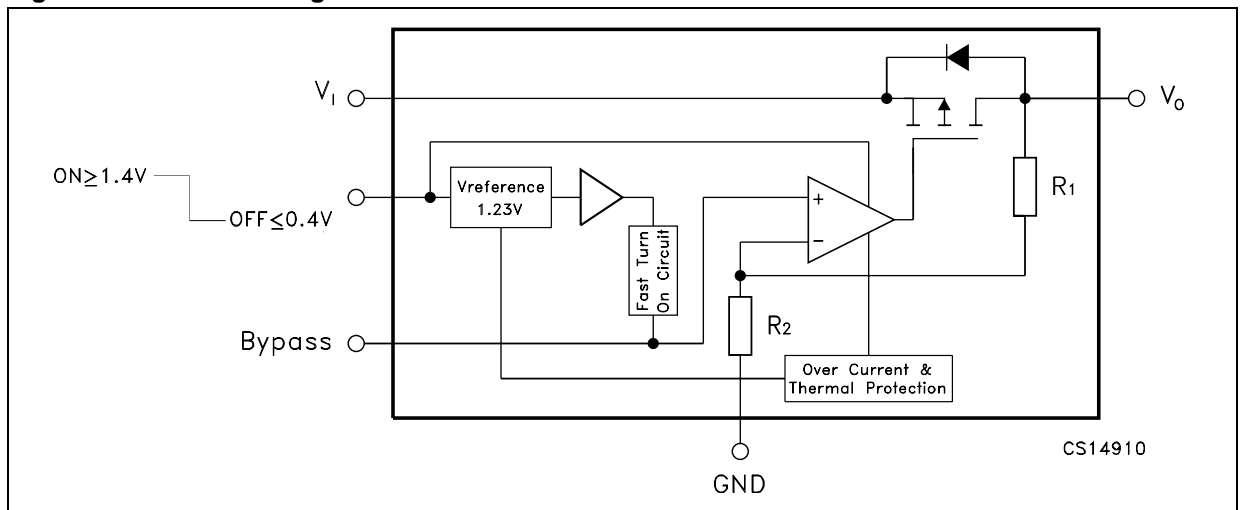


Table 1: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	-0.3 to 6 (*)	V
V_O	DC Output Voltage	-0.3 to $V_I+0.3$	V
V_{INH}	INHIBIT Input Voltage	-0.3 to $V_I+0.3$	V
I_O	Output Current	Internally limited	
P_D	Power Dissipation	Internally limited	
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{OP}	Operating Junction Temperature Range	-40 to 125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) The input pin is able to withstand non repetitive spike of 6.5V for 200ms.

Table 2: Thermal Data

Symbol	Parameter	SOT23-5L	DFN6	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	81	10	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	255	55	°C/W

Table 3: Order Codes

SOT23-5L	DFN6	OUTPUT VOLTAGES
LDS3985M125R (*)	LDS3985PM12R (*)	1.25 V
LDS3985M135R (*)	LDS3985PM13R (*)	1.35 V
LDS3985M15R (*)	LDS3985PM15R (*)	1.5 V
LDS3985M18R	LDS3985PM18R	1.8 V
LDS3985M20R (*)	LDS3985PM20R (*)	2.0 V
LDS3985M21R (*)	LDS3985PM21R (*)	2.1 V
LDS3985M22R (*)	LDS3985PM22R (*)	2.2 V
LDS3985M25R	LDS3985PM25R	2.5 V
LDS3985M26R (*)	LDS3985PM26R (*)	2.6 V
LDS3985M27R (*)	LDS3985PM27R (*)	2.7 V
LDS3985M28R	LDS3985PM28R	2.8 V
LDS3985M285R (*)	LDS3985PM285R (*)	2.85 V
LDS3985M29R	LDS3985PM29R (*)	2.9 V
LDS3985M30R (*)	LDS3985PM30R (*)	3.0 V
LDS3985M31R (*)	LDS3985PM31R (*)	3.1 V
LDS3985M32R (*)	LDS3985PM32R (*)	3.2 V
LDS3985M33R	LDS3985PM33R	3.3 V
LDS3985M47R (*)	LDS3985PM47R (*)	4.7 V
LDS3985M48R (*)	LDS3985PM48R (*)	4.8 V
LDS3985M49R (*)	LDS3985PM49R (*)	4.9 V
LDS3985M50R (*)	LDS3985PM50R (*)	5.0 V

(*) Available on request.

Figure 2: Connection Diagram (top view for SOT, top through view for DFN6)

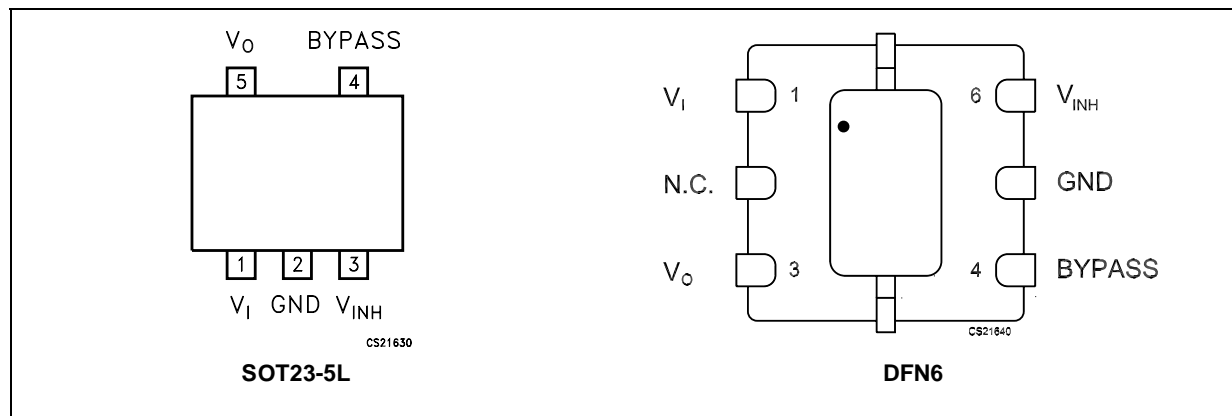


Table 4: Pin Description

Pin N° SOT23-5L	Pin N° DFN6	Symbol	Name and Function
1	1	V_I	Input Voltage of the LDO
2	5	GND	Common Ground
3	6	V_{INH}	Inhibit Input Voltage: ON MODE when $V_{INH} \geq 1.2V$, OFF MODE when $V_{INH} \leq 0.4V$ (Do not leave floating, not internally pulled down/up)
4	4	BYPASS	Bypass Pin: Connect an external capacitor (usually 10nF) to minimize noise voltage
5	3	V_O	Output Voltage of the LDO
-	2	N.C.	Not Connect.

Figure 3: Typical Application Circuit

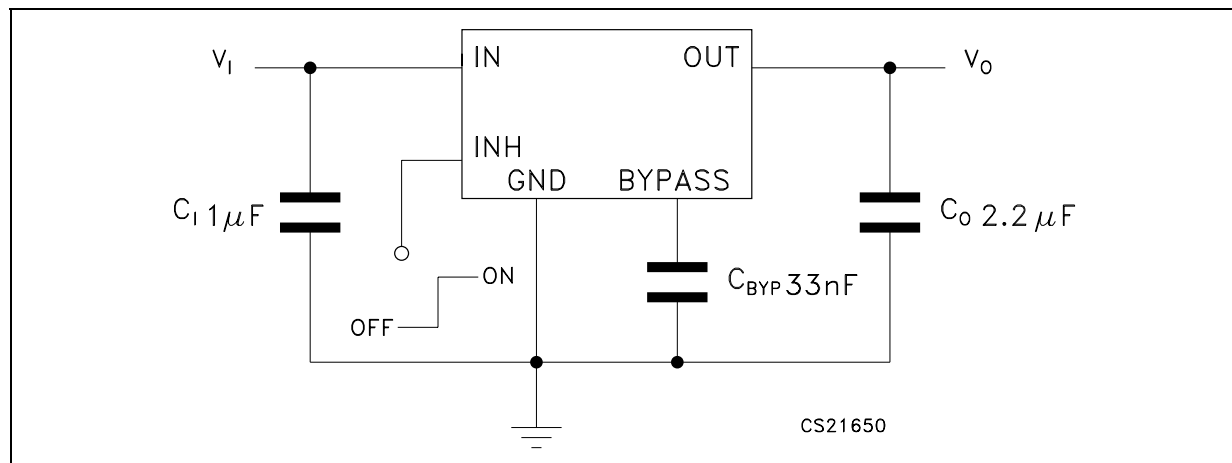


Table 5: Electrical Characteristics For LDS3985 ($T_J = 25^\circ\text{C}$, $V_I = V_{O(NOM)} + 0.5\text{V}$, $C_I = 1\mu\text{F}$, $C_O = 2.2\mu\text{F}$, $C_{BYP} = 33\text{nF}$, $I_O = 1\text{mA}$, $V_{INH} = 1.4\text{V}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_I	Operating Input Voltage		2.5		6	V
V_O	Output Voltage < 2.5V	$I_O = 1\text{mA}$	-50		50	mV
		$T_J = -40\text{ to }125^\circ\text{C}$	-75		75	
V_O	Output Voltage $\geq 2.5\text{V}$	$I_O = 1\text{mA}$	-2		2	% of $V_{O(NOM)}$
		$T_J = -40\text{ to }125^\circ\text{C}$	-3		3	
ΔV_O	Line Regulation (Note 1)	$V_I = V_{O(NOM)} + 0.5\text{ to }6\text{V}$, $T_J = -40\text{ to }125^\circ\text{C}$	-0.1		0.1	% / V
		$V_O = 4.7\text{ to }5\text{V}$	-0.19		0.19	
ΔV_O	Load Regulation	$I_O = 1\text{mA to }300\text{mA}$, $V_O \leq 2.5\text{V}$ $T_J = -40\text{ to }125^\circ\text{C}$		0.005	0.01	% / mA
ΔV_O	Load Regulation	$I_O = 1\text{mA to }300\text{mA}$, $V_O \geq 2.5\text{V}$ $T_J = -40\text{ to }125^\circ\text{C}$		0.0008	0.004	% / mA
ΔV_O	Output AC Line Regulation (Note 2)	$V_I = V_{O(NOM)} + 1\text{V}$, $I_O = 300\text{mA}$, $t_R = t_F = 30\mu\text{s}$		5		mV _{PP}
I_Q	Quiescent Current ON MODE: $V_{INH} = 1.24\text{V}$	$I_O = 0$		85		μA
		$I_O = 0$	$T_J = -40\text{ to }125^\circ\text{C}$		150	
		$I_O = 0\text{ to }300\text{mA}$		200		
		$I_O = 0\text{ to }300\text{mA}$	$T_J = -40\text{ to }125^\circ\text{C}$		300	
	OFF MODE: $V_{INH} = 0.4\text{V}$			0.003		
		$T_J = -40\text{ to }125^\circ\text{C}$			1.5	
V_{DROP}	Dropout Voltage (Note 3)	$I_O = 1\text{mA}$		0.4		mV
		$I_O = 1\text{mA}$	$T_J = -40\text{ to }125^\circ\text{C}$		2	
		$I_O = 150\text{mA}$		60		
		$I_O = 150\text{mA}$	$T_J = -40\text{ to }125^\circ\text{C}$		100	
		$I_O = 300\text{mA}$		150		
		$I_O = 300\text{mA}$	$T_J = -40\text{ to }125^\circ\text{C}$		250	
I_{SC}	Short Circuit Current	$R_L = 0$		600		mA
SVR	Supply Voltage Rejection	$V_I = V_{O(NOM)} + 0.25\text{V} \pm$ $V_{RIPPLE} = 0.1\text{V}$, $I_O = 50\text{mA}$ For $V_{O(NOM)} < 2.5\text{V}$, $V_I = 2.55\text{V}$	$f = 1\text{KHz}$	55		dB
			$f = 10\text{KHz}$	50		
$I_{O(PK)}$	Peak Output Current	$V_O \geq V_{O(NOM)} - 5\%$	300	550		mA
V_{INH}	Inhibit Input Logic Low	$V_I = 2.5\text{V to }6\text{V}$, $T_J = -40\text{ to }125^\circ\text{C}$			0.4	V
	Inhibit Input Logic High		1.4			
I_{INH}	Inhibit Input Current	$V_{INH} = 0.4\text{V}$, $V_I = 6\text{V}$		± 1		nA
eN	Output Noise Voltage	$B_W = 10\text{ Hz to }100\text{ KHz}$, $C_O = 2.2\mu\text{F}$		30		μV_{RMS}
t_{ON}	Turn On Time (Note 4)	$C_{BYP} = 33\text{ nF}$		240		μs
T_{SHDN}	Thermal Shutdown	Note 5		160		$^\circ\text{C}$
C_O	Output Capacitor	Capacitance (Note 6)	2.2		22	μF
		ESR	5		5000	m Ω

Note 1: For $V_{O(NOM)} < 2\text{V}$ $V_I = 2.5\text{V}$

Note 2: For $V_{O(NOM)} = 1.25\text{V}$ $V_I = 2.5\text{V}$

Note 3: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.

Note 4: Turn -on time is time measured between the enable input just exceeding V_{INH} High Value and the output voltage just reaching 95% of its nominal value

Note 5: Typical thermal protection hysteresis is 20°C

TYPICAL PERFORMANCE CHARACTERISTICS ($T_j = 25^\circ\text{C}$, $V_I = V_{O(\text{NOM})} + 0.5\text{V}$, $C_1 = 1\mu\text{F}$, $C_O = 2,2\mu\text{F}$, $C_{\text{BYP}} = 33\text{nF}$, $I_O = 1\text{mA}$, $V_{\text{INH}} = 1.4\text{V}$, unless otherwise specified)

Figure 4: Output Voltage vs Temperature

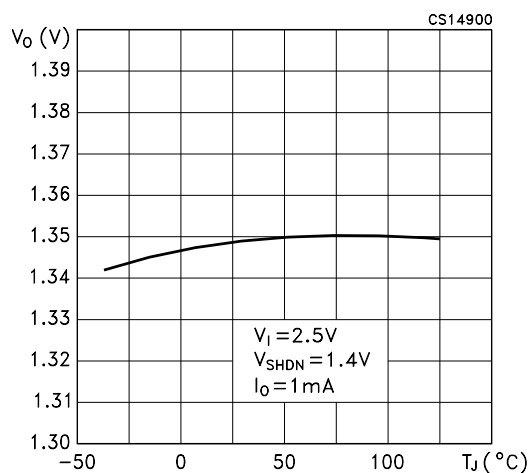


Figure 7: Shutdown Voltage vs Temperature

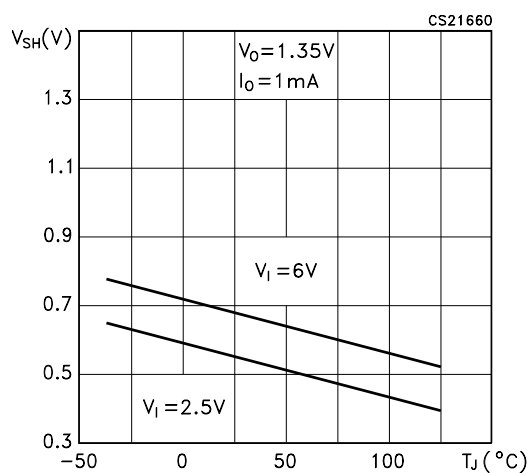


Figure 5: Output Voltage vs Temperature

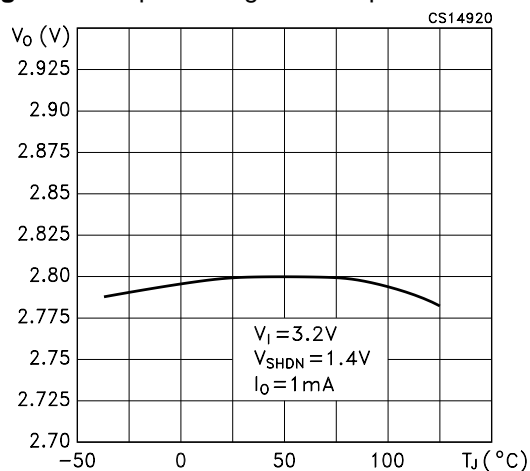


Figure 8: Shutdown Voltage vs Temperature

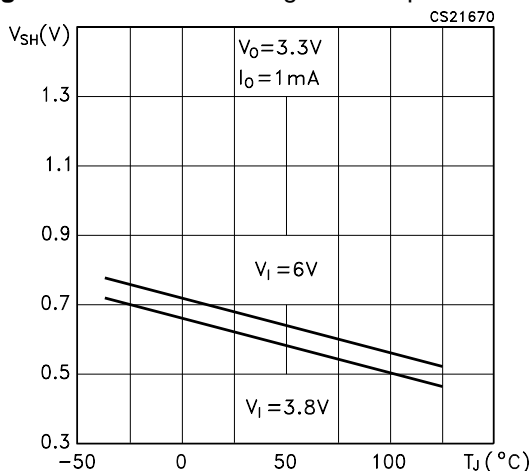


Figure 6: Output Voltage vs Temperature

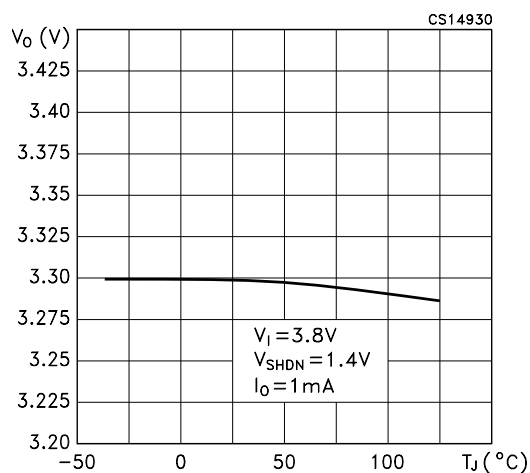


Figure 9: Line Regulation vs Temperature

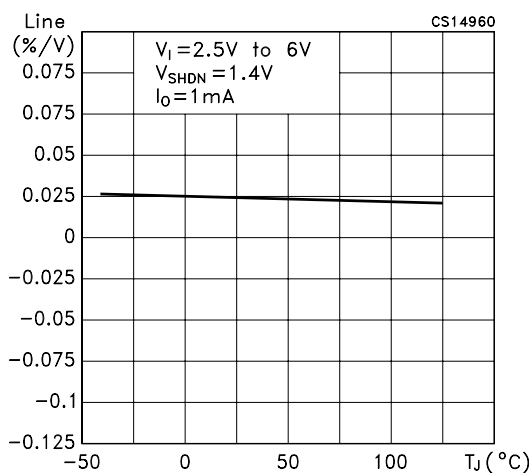


Figure 10: Line Regulation vs Temperature

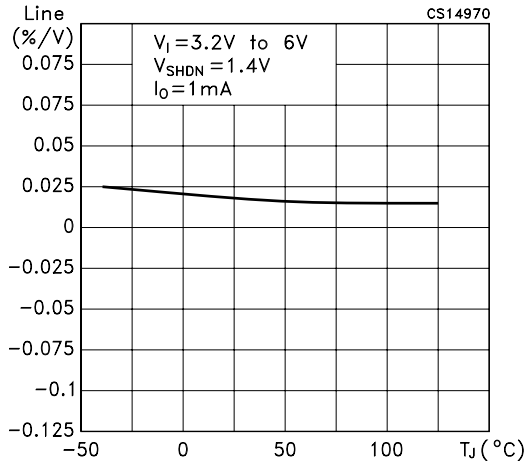


Figure 11: Line Regulation vs Temperature

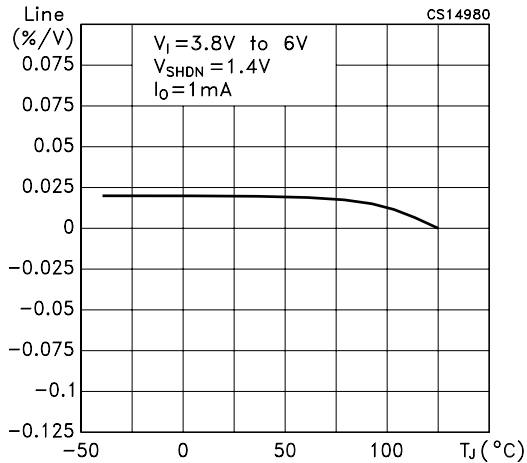


Figure 12: Quiescent Current vs Temperature

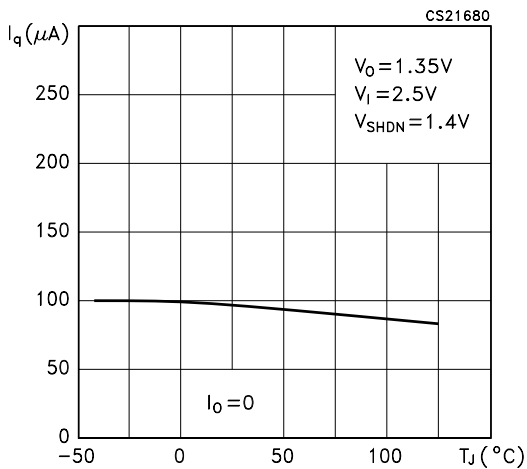


Figure 13: Quiescent Current vs Temperature

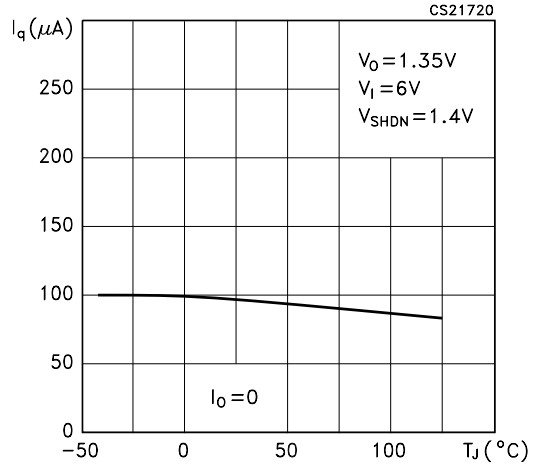


Figure 14: Quiescent Current vs Temperature

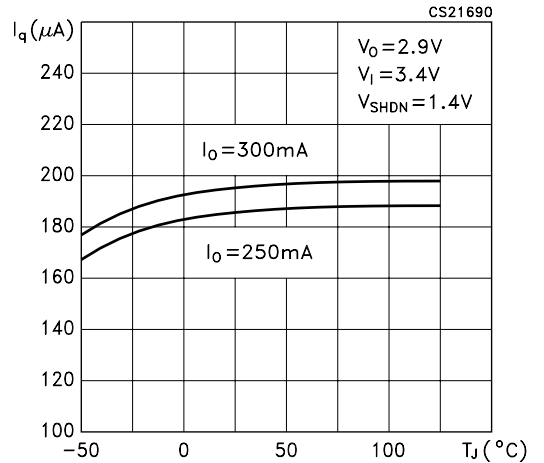


Figure 15: Supply Voltage Rejection vs Frequency

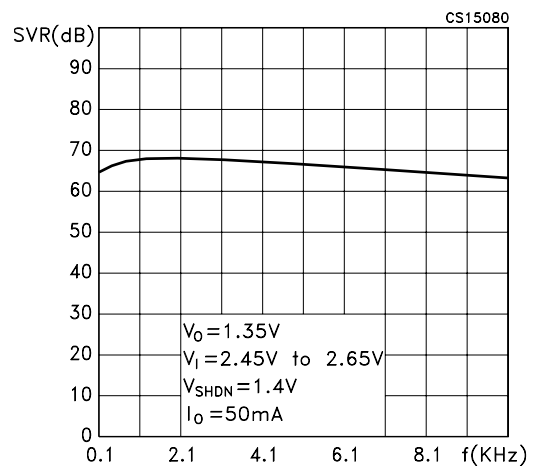


Figure 16: Dropout Voltage vs Temperature

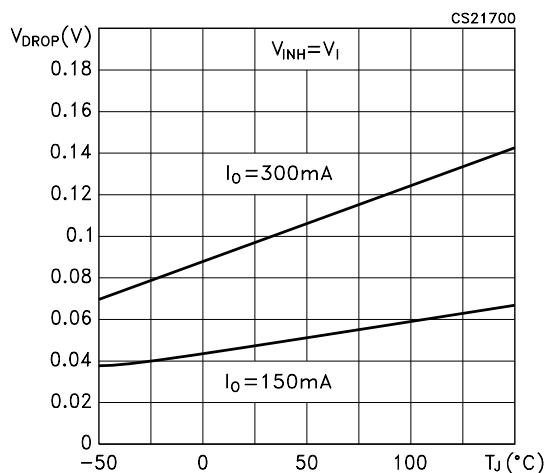


Figure 17: Dropout Voltage vs Output Current

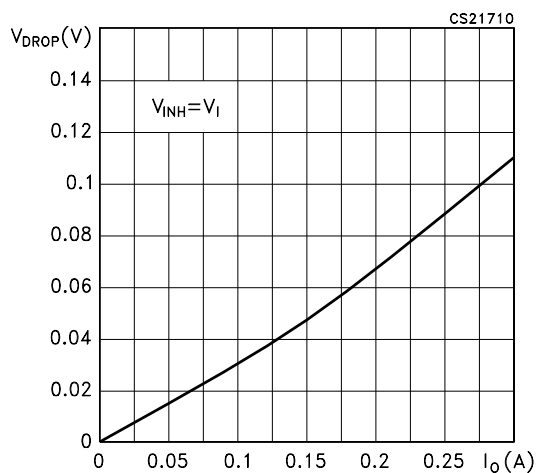
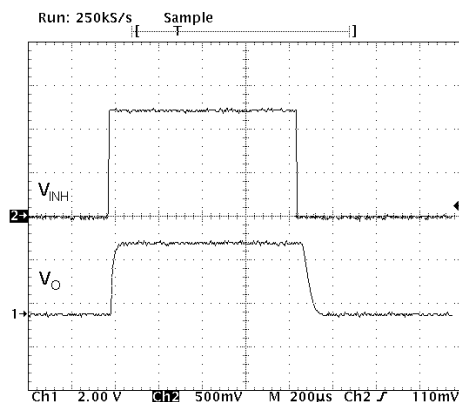


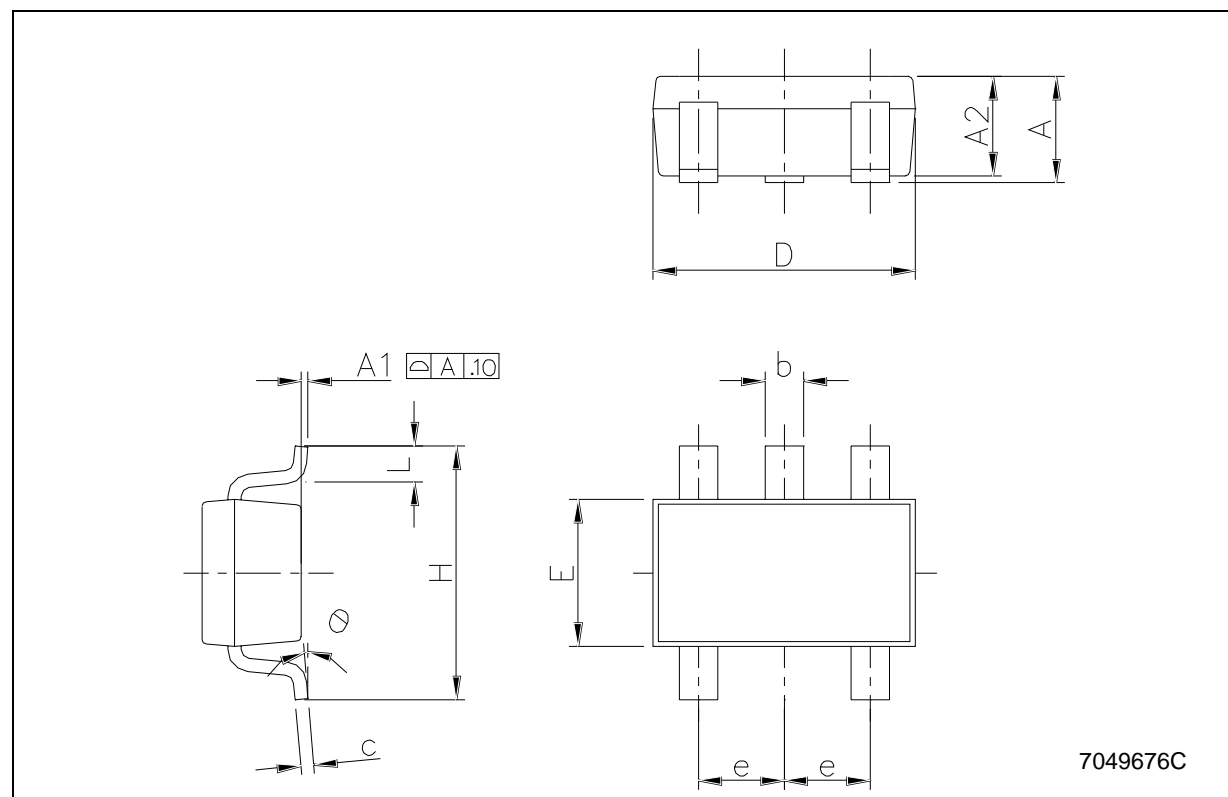
Figure 18: Inhibit Transient



$V_{\text{I}} = 5\text{V}$, $I_{\text{O}} = 1\text{mA}$, $V_{\text{INH}} = 0$ to 1.2V , $C_{\text{I}} = C_{\text{O}} = 1\mu\text{F}$ (cer),
 $C_{\text{BYP}} = 10\text{nF}$, $T_{\text{R}} = T_{\text{F}} = 1\mu\text{s}$

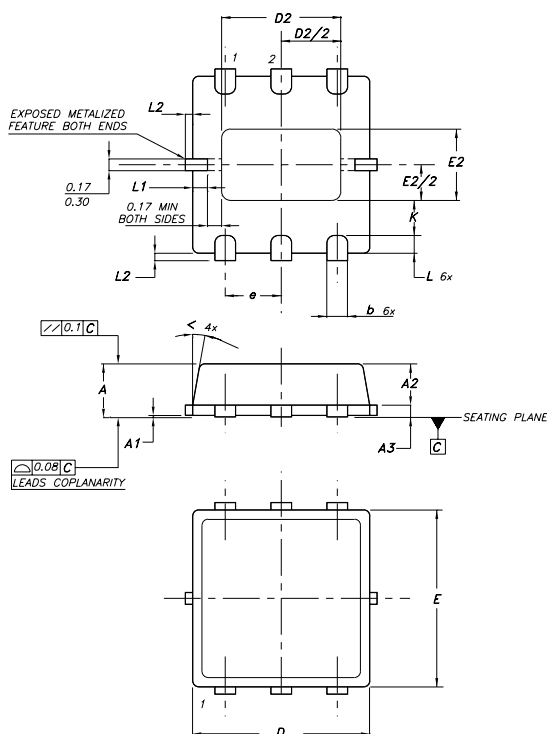
SOT23-5L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



DFN6 (3x3) MECHANICAL DATA

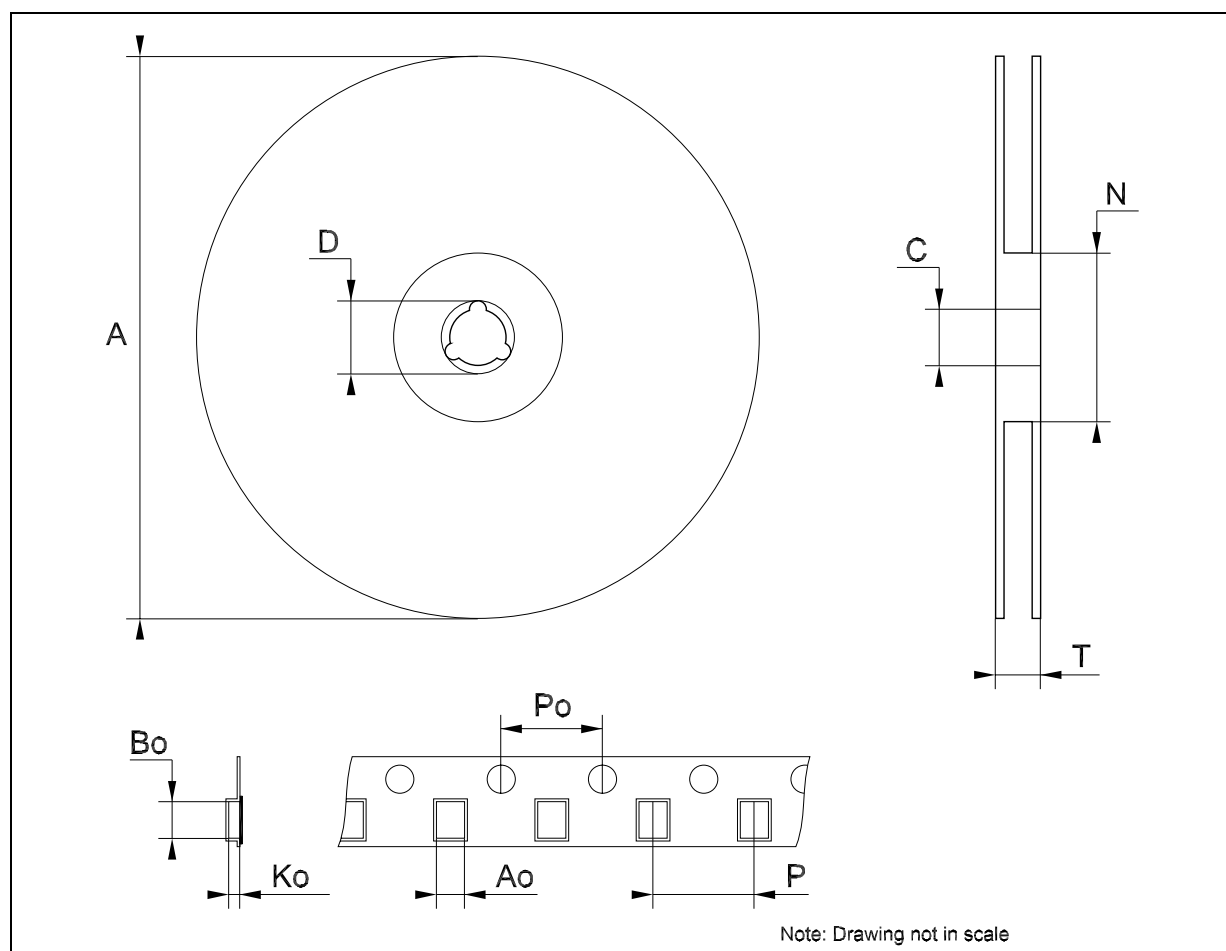
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80		1.00	31.5		39.4
A1	0		0.05	0.0		2.0
A2	0.65		0.75	25.6		29.5
A3		0.20			7.9	
b	0.33		0.43	13.0		16.9
D	2.90	3.00	3.10	114.2	118.1	122.0
D2	1.92		2.12	75.6		83.5
E	2.90	3.00	3.10	114.2	118.1	122.0
E2	1.11		1.31	43.7		51.6
e		0.95			37.4	
L	0.20		0.45	7.9		17.7
L1		0.24			9.4	
L2			0.13			5.1
K	0.20			7.9		



7387339A

Tape & Reel SOT23-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



Tape & Reel QFNxx/DFNxx (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

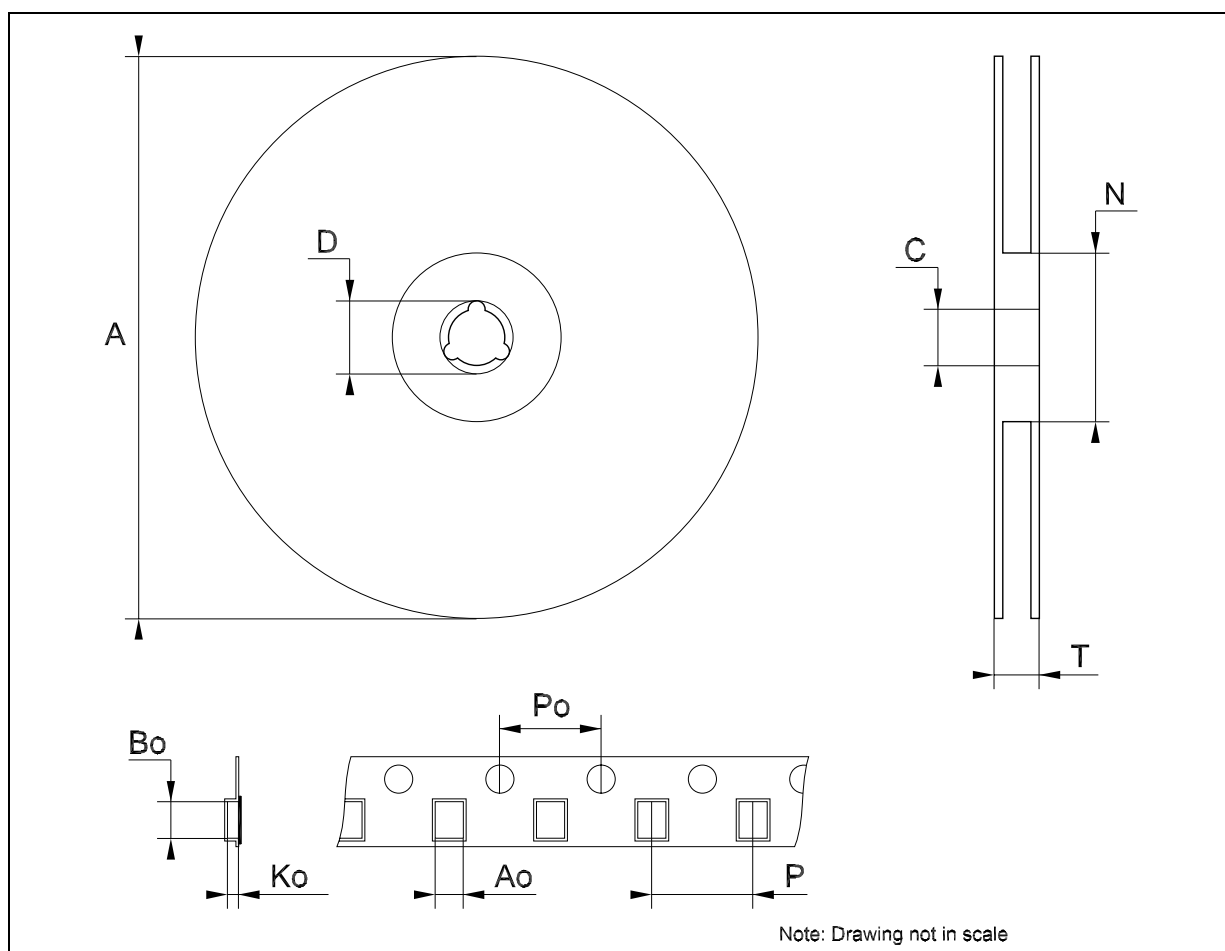


Table 6: Revision History

Date	Revision	Description of Changes
02-Dic-2004	1	First Release.

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