TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WBL125FK

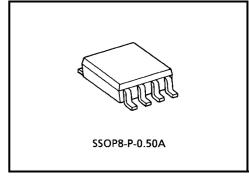
Dual Low-Voltage Bus Switch

The TC7WBL125FK is a low on-resistance, high-speed CMOS 2-bit bus switch with low voltage operation. This bus switch allows the connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

When output enable (\overline{OE}) is at low level, the switch is on; when at high level, the switch is off.

P-MOS and N-MOS channel block also allows that the device is suitable for analog signal transmission.

All inputs are equipped with protection circuits to protect the device from static discharge.

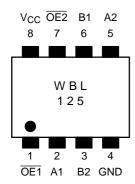


Weight: 0.01 g (typ.)

Features

- Operating voltage: $V_{CC} = 2 \sim 3.6 \text{ V}$
- High speed operation: tpd = 0.25 ns (max) @3 V
- Ultra-low on resistance: $R_{ON} = 5 \Omega$ (typ.) @3 V
- Electro-static discharge (ESD) performance: ±200 V or more (JEITA)
 - ±2000 V or more (MIL)
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power-down protection for inputs and I/O terminal.
- Package: US8

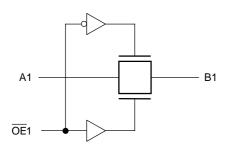
Pin Assignment (top view)

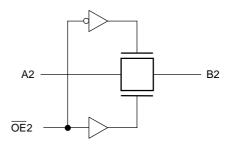


Truth Table

Inputs	Function			
ŌĒ	Function			
L	A port = B port			
Н	Disconnect			

System Diagram





Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	-0.5~7.0	V
Control pin input voltage	V _{IN}	-0.5~7.0	V
Switch terminal I/O voltage	Vs	-0.5~7.0	V
Clump diode current	I _{IK}	-50	mA
Switch I/O current	IS	128	mA
Power dissipation	P _D	200	mW
DC V _{CC} /GND current	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65~150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	2.0~3.6	V
Control pin input voltage	V _{IN}	0~5.5	V
Switch I/O voltage	Vs	0~5.5	V
Operating temperature	T _{opr}	-40~85	°C
Control pin input rise/fall time	dt/dv	0~10	ns/V

Electrical Characteristics

DC Characteristics ($Ta = -40 \sim 85$ °C)

Character	ristics	Symbol	Test Condition V _{CC} (V)		Min	Тур.	Max	Unit	
Control pin input	"H" level	V _{IH}	_		2.0~3.6	0.7 × V _{CC}	_	_	V
voltage	"L" level	V _{IL}	_		2.0~3.6	_	_	0.3 × V _{CC}	V
Input leakage cur	rent	I _{IN}	V _{IN} = 0~5.5 V		2.0~3.6	_	_	±1.0	μΑ
Power off leakage	current	I _{OFF}	A, B, $\overline{OE} = 0 \sim 5.5 \text{ V}$		0	_	_	±1.0	μΑ
Off-state leakage (switch off)	current	I _{SZ}	A, B = 0~5.5 V, OE = V _{CC}		2.0~3.6	_	_	±1.0	μА
			$V_{IS} = 0 \text{ V}, I_{IS} = 30 \text{ mA}$	(Note 1)	3.0	_	2	7	
			$V_{IS} = 3.0 \text{ V}, I_{IS} = 30 \text{ mA}$	(Note 1)	3.0	_	3	7	
ON resistance (Note 3)	D	V _{IS} = 2.4 V, I _{IS} = 15 mA	(Note 1)	3.0	_	5	15	Ω	
	KON	V _{IS} = 0 V, I _{IS} = 24 mA	(Note 2)	2.3	_	3	10	22	
		V _{IS} = 2.3 V, I _{IS} = 24 mA	(Note 2)	2.3	_	4	15		
			V _{IS} = 1.7 V, I _{IS} = 15 mA	(Note 2)	2.3	_	9	25	
Quiescent supply	current	Icc	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$		3.6	_	_	10	μΑ

Note 1: The typical values are at $V_{CC} = 3.3 \text{ V}$, $Ta = 25^{\circ}\text{C}$.

Note 2: The typical values are at $V_{CC} = 2.5 \text{ V}$, $Ta = 25^{\circ}\text{C}$.

Note 3: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on two (A or B) pins.

AC Characteristics ($Ta = -40 \sim 85$ °C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time (bus to bus)	t _{pLH}	Figure 1, Figure 2 (Note 4)	3.0		0.25	ns
Output enable time	t_{pZL}	Figure 1, Figure 3	3.0		TBD	ns
Output enable time	t _{pZH}	rigure 1, rigure 3	2.3	_	TBD	115
Output disable time	t _{pLZ}	Figure 1, Figure 3	3.0	_	TBD	ns
Output disable time	t _{pHZ}	rigure i, rigure o	2.3	_	TBD	110

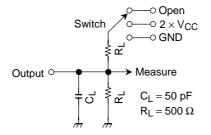
Note 4: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Control pin input capacitance	C _{IN}	(Note 5)	3.0	3	pF
Switch terminal capacitance	C _{I/O}	$\overline{OE} = V_{CC}$ (Note 5)	3.0	10	pF

Note 5: This item is guaranteed by design.

AC Test Circuit



Parameter	Switch		
t _{pLH} , t _{pHL}	Open		
t _{pLZ} , t _{pZL}	$2 \times V_{CC}$		
t _{pHZ} , t _{pZH}	GND		

Figure 1

AC Waveform

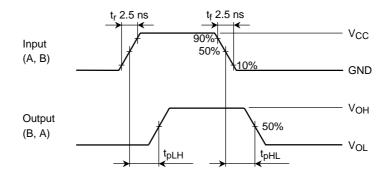


Figure 2 t_{pLH}, t_{pHL}

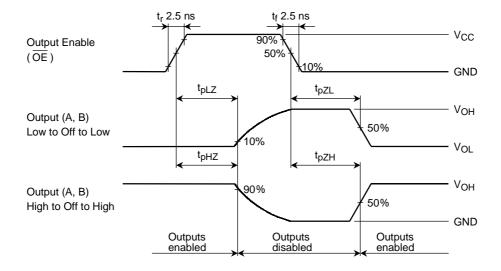
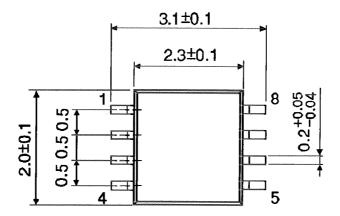
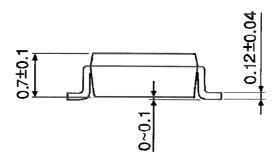


Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Package Dimensions

SSOP8-P-0.50A Unit: mm





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Weight: 0.01 g (typ.)

2001-10-16

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