Triple Line Receiver

The MC10114 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

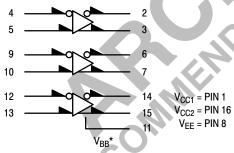
Another feature of the MC10114 is that the OR outputs go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumen—tation systems. The MC10114 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A V_{BB} reference is provided which is useful in making the MC10114 a Schmit trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary. See MECL Design Handbook (HB205) pages 226 and 228.

- $P_D = 145 \text{ mW typ/pkg}$
- $t_{pd} = 2.4$ ns typ (Single Ended Input)
- $t_{pd} = 2.0$ ns typ (Differential Input)
- t_r , $t_f = 2.1$ ns typ (20%–80%)

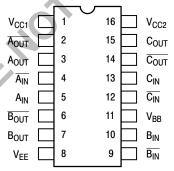
LOGIC DIAGRAM



 $^*V_{BB}$ to be used to supply bias to the MC10114 only and bypassed (when used) with 0.01 μ F to 0.1 μ F capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, its respective output pin with bubble goes positive.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS

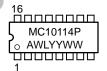


CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot YY = Year

WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10114L	CDIP-16	25 Units / Rail
MC10114P	PDIP-16	25 Units / Rail
MC10114FN	PLCC-20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic Symbol Test Min Max Min Typ Max Min I			Pin		Test Limits		1	-			
Power Supply Drain Current IE 8 39 28 35			Under		–30°C					1	
Input Current				Min		Min			Min	Max	Uni
Coutput Voltage	-						28			39	mAc
Output Voltage Logic 1 V _{OH} 2 -1.060 -0.890 -0.960 -0.810 -0.890 -0.890 -0.960 -0.810 -0.890 -0.890 -0.960 -0.810 -0.890 -0.890 -0.960 -0.810 -0.890 -0.890 -0.960 -0.810 -0.890 -0.890 -0.960 -0.810 -0.890 -0.890 -0.810 -0.890 -0.890 -0.810 -0.890 -0.825 -0.80 -1.650 -1.825 -0.825 -0.80 -1.825 -0.980 -1.825 -0.980 -0.980 -0.980 -0.91	nt				 					45	μAd
3										1.0	μAd
Threshold Voltage Logic 1 V _{OHA} 2 -1.890 -1.675 -1.850 -1.825 -1.080 -1.080 -0.980 -0.980 -0.910 -			3			-0.960				-0.700 -0.700	Vdo
Threshold Voltage Logic 0 V _{OLA} 2	age Logi	ic 0 V _{OL}	2 3							-1.615 -1.615	Vdd
Reference Voltage V _{BB} 11 -1.420 -1.280 -1.350 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.295 -1.230 -1.230 -1.295 -1.230 -1.230 -1.295 -1.230 -1.	'oltage Logi	ic 1 V _{OH}	2 3								Vdd
Common Mode Rejection Test V _{OH} 2 department of the state of th	'oltage Logi	ic 0 V _{OL} A								-1.595 -1.595	Vdd
Test $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	/oltage	V _{BB}	11	-1.420	-1.280	-1.350		-1.230	-1.295	-1.150	Vdd
Switching Times (50Ω Load) Propagation Delay $t_{4+2+} = 2 \\ t_{4+3-} = 3 \\ t_{4-3+} = 3 \\ t_{3+} = 3 \\ Tall Time $ (20 to 80%) $t_{2-} = 2 \\ t_{3-} = 3 \\ t_{3-} = 3 $ (20 to 80%) $t_{2-} = 2 \\ t_{3-} = 3 \\ t_{3-} = 3 $ (20 to 80%) $t_{2-} = 2 \\ t_{3-} = 3 \\ t_{3-} = 3 $ (20 to 80%) $t_{2-} = 2 \\ t_{3-} = 3 \\ t_{3-} = 3 $ (20 to 80%) $t_{2-} = 2 \\ t_{3-} = 3 \\ t_{3-} = 3 $ (20 to 80%) $t_{3-} = 3 \\ t_{3-} = 3 $ (20 to 80%) $t_{3-} = 3 \\ t_{3-} = 3 $ (20 to 80%) $t_{3-} = 3 \\ t_{3-} = 3 $ (20 to 80%) $t_{3-} = 3 \\ t_{3-} = 3 $ (20 to 80%) $t_{3-} = 3 \\ t_{3-} = 3 $ (30 to 80%) $t_{3-} = 3 \\ t_{3-} = 3 $ (4.4	ode Rejection	V _{OH}								-0.700 -0.700	Vdo
Propagation Delay $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		V _{OL}								-1.615 -1.615	Vdo
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	imes (50Ω Lo	ad)		Min	Max	Min	Тур	Max	Min	Max	ns
Fall Time (20 to 80%) $\begin{array}{c ccccccccccccccccccccccccccccccccccc$	·	t ₄₋₂₋ t ₄₊₃₋ t ₄₋₃₊	2 3 . 3	1.0 1.0 1.0	4.4 4.4 4.4	1.0 1.0 1.0	2.4 2.4 2.4	4.0 4.0 4.0	0.9 0.9 0.9	4.3 4.3 4.3 4.3	
t ₃₋ 3 1.5 3.8 1.5 2.1 3.5 1.5		t ₃₊	3		3.8					3.7 3.7	
13_ 3_ 1.5 3.6 1.5 2.1 3.5 1.5	(20 to 80		2	1.5	3.8					3.7 3.7	
OENICE NOT RECOMME			A LECO								

ELECTRICAL CHARACTERISTICS (continued)

				TEST VOL	TAGE VALU			1
	@ Test Te	mperature	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{BB}	
		–30°C	-0.890	-1.890	-1.205	-1.500	From	
		+25°C	-0.810	-1.850	-1.105	-1.475	Pin	
	-	+85°C	-0.700	-1.825	-1.035	-1.440	11	
		Pin Under	TEST V	OLTAGE AP	PLIED TO PI	NS LISTED I	BELOW	
Characteristic	Symbol	Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{BB}	
Power Supply Drain Current	Ι _Ε	8		4, 9, 12			5, 10, 13	r
Input Current	I _{inH}	4	4	9, 12			5, 10, 13	ļ
	l _{inL}	4		9, 12			5, 10, 13	
Output Voltage Logic 1	I V _{OH}	2 3	4 9, 12	9, 12 4			5, 10, 13 5, 10, 13	
Output Voltage Logic 0	V _{OL}	2 3	9, 12 4	4 9, 12			5, 10, 13 5, 10, 13	
Threshold Voltage Logic 1	I V _{OHA}	2 3	9, 12	9, 12	4	4	5, 10, 13 5, 10, 13	
Threshold Voltage Logic C) V _{OLA}	2 3	9, 12	9, 12	4	4	5, 10, 13 5, 10, 13	
Reference Voltage	V _{BB}	11					5, 10, 13	
Common Mode Rejection Test	V _{OH}	2 3		1	04			
	V _{OL}	2 3		1,0	5			
Switching Times (50Ω Load))			X	Pulse In	Pulse Out		l
Propagation Delay	t ₄₊₂₊	2			4	2	5, 10, 13	
	t ₄₋₂₋	2 2 3			4 4	2 3	5, 10, 13 5, 10, 13	
	t ₄₊₃₋ t ₄₋₃₊	3			4	3	5, 10, 13	
Rise Time (20 to 80%)) t ₂₊	2			4	2	5, 10, 13	
	t ₃₊	3			4	3		
Fall Time (20 to 80%)) t ₂₋	2			4	2		
Fall Time (20 to 80%)					4	3	5, 10, 13 5, 10, 13 5, 10, 13	

ELECTRICAL CHARACTERISTICS (continued)

					TEST VOI	TAGE VALU	JES (Volts)		
		@ Test Te	mperature	V _{IHH} *	V _{ILH} *	V _{IHL} *	V _{ILL} *	V _{EE}	
			-30°C	+0.110	-0.890	-1.890	-2.890	-5.2	
			+25°C	+0.190	-0.850	-1.810	-2.850	-5.2	
			+85°C	+0.300	-0.825	-1.700	-2.825	-5.2	
			Pin	TEST V	OLTAGE AP	PLIED TO P	INS LISTED	BELOW	
Characteristic		Symbol	Under Test	V _{IHH} *	V _{ILH} *	V _{IHL} *	V _{ILL} *	V _{EE}	(V _{CC}) Gnd
Power Supply Drain C	urrent	Ι _Ε	8					8	1, 16
Input Current		l _{inH}	4					8	1, 16
		I _{inL}	4					8, 4	1, 16
Output Voltage	Logic 1	V _{OH}	2 3					8 8	1, 16 1, 16
Output Voltage	Logic 0	V _{OL}	2 3					8	1, 16 1, 16
Threshold Voltage	Logic 1	V _{OHA}	2 3					8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V _{OLA}	2 3					8 8	1, 16 1, 16
Reference Voltage		V_{BB}	11					8	1, 16
Common Mode Reject	tion Test	V _{OH}	2 3	4	5	5	4	8 8	1, 16 1, 16
		V _{OL}	2 3	4	5	5	4	8 8	1, 16 1, 16
Switching Times	(50 Ω Load)							-3.2 V	+2.0 V
Propagation Delay		t ₄₊₂₊ t ₄₋₂₋ t ₄₊₃₋ t ₄₋₃₊	2 2 3 3					8 8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time	(20 to 80%)	t ₂₊	2 3					8 8	1, 16 1, 16
Fall Time	(20 to 80%)	t ₂₋ t ₃₋	2 3					8 8	1, 16 1, 16

^{*} V_{IHH} = Input Logic 1 level shifted positive one volt for common mode rejection tests

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibitum has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

V_{ILH} = Input Logic 0 level shifted positive one volt for common mode rejection tests

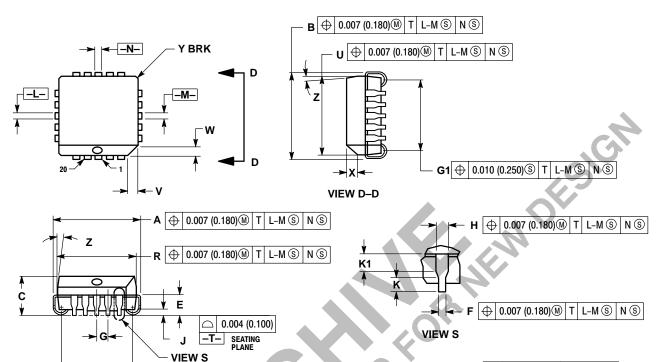
V_{IHL} = Input Logic 1 level shifted negative one volt for common mode rejection tests

V_{ILL} = Input Logic 0 level shifted negative one volt for common mode rejection tests

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



NOTES:

G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OF VICE NOT PRESCO

- OTES:

 1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

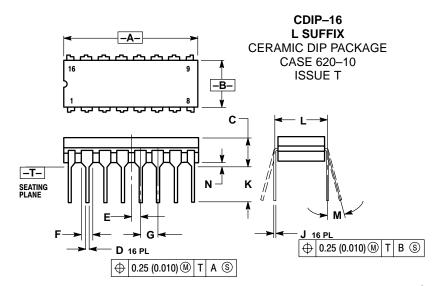
 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

 4. DIMENSIONING AND TOLERANCING PER ANSI V14 5M 1982
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.385	0.395	9.78	10.03
В	0.385	0.395	9.78	10.03
С	0.165	0.180	4.20	4.57
Ε	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
Н	0.026	0.032	0.66	0.81
J	0.020		0.51	
K	0.025		0.64	
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
Χ	0.042	0.056	1.07	1.42
Y		0.020		0.50
Z	2°	10°	2°	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040		1.02	

PACKAGE DIMENSIONS



NOTES:

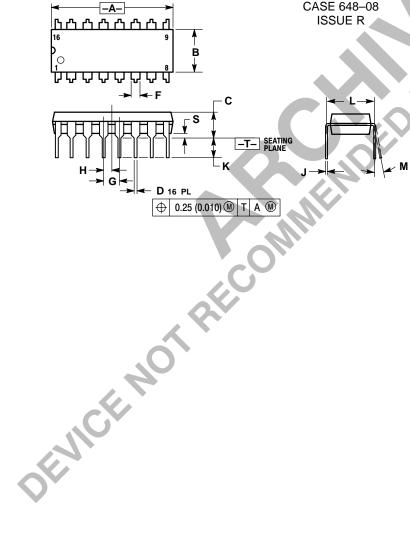
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION LTO CENTER OF LEAD WHEN CONTROLLING DIMENSION LTO CENTER OF LEAD WHEN

- FORMED PARALLEL

 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC
 BODY.

	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	0.750	0.785	19.05	19.93		
В	0.240	0.295	6.10	7.49		
C		0.200		5.08		
D	0.015	0.020	0.39	0.50		
E	0.050	BSC	1.27 BSC			
F	0.055	0.065	1.40	1.65		
G	0.100	BSC	2.54 BSC			
Н	0.008	0.015	0.21	0.38		
K	0.125	0.170	3.18	4.31		
L	0.300	BSC	7.62 BSC			
M	0 °	15°	0 °	15°		
N	0.020	0.040	0.51	1.01		

PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
C	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

Notes





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