Quad Line Receiver

The MC10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

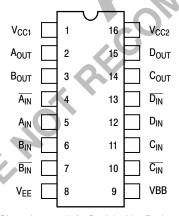
- $P_D = 110 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 2.0 \text{ ns typ}$
- t_r , $t_f = 2.0$ ns typ (20%–80%)

LOGIC DIAGRAM 4 5 2 7 6 3 10 11 14 13 12 V_{BB}* 9

 V_{CC1} = PIN 1 V_{CC2} = PIN 16 V_{EE} = PIN 8

 * V_{BB} to be used to supply bias to the MC10115 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA. When the input pin with the bubble goes positive, the output goes negative.

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



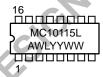
ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS



CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648 MC10115P
O AWLYYWW



PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot YY = Year WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10115L	CDIP-16	25 Units / Rail
MC10115P	PDIP-16	25 Units / Rail
MC10115FN	PLCC-20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

				Test Limits							
			Pin Under	-30)°C		+25°C		+85	5°C	
Characteristic		Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Drain (Current	Ι _Ε	8		29			26		29	mAdc
Input Current		I _{inH}	4		150			95		95	μAdc
		I _{CBO}	4		1.5			1.0		1.0	μAdc
Output Voltage	Logic 1	V _{OH}	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
Output Voltage	Logic 0	V _{OL}	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
Threshold Voltage	Logic 1	V _{OHA}	2	-1.080		-0.980			-0.910		Vdc
Threshold Voltage	Logic 0	V _{OLA}	2		-1.655			-1.630		-1.595	Vdc
Reference Voltage		V_{BB}	9	1.420	1.280	-1.350		-1.230	1.295	-1.150	Vdc
Switching Times (509	Ω Load)									. (6	ns
Propagation Delay		t ₄₋₂₊ t ₄₊₂₋	2 2	1.0 1.0	3.1 3.1	1.0 1.0		2.9 2.9	1.0 1.0	3.3 3.3	
Rise Time (20	to 80%)	t ₂₊	2	1.1	3.6	1.1		3.3	1.1	3.7	
Fall Time (20	to 80%)	t ₂₋	2	1.1	3.6	1.1		3.3	1.1	3.7	

ELECTRICAL CHARACTERISTICS (continued)

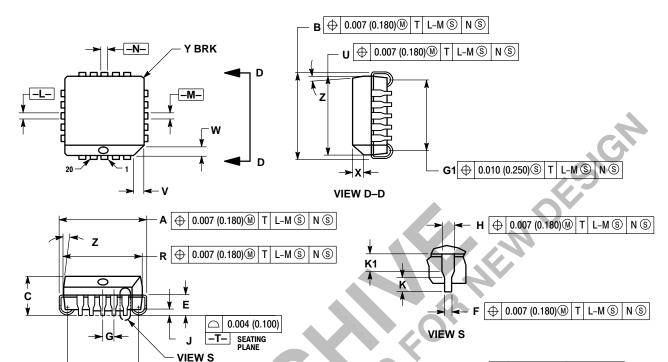
ELECTRICAL CHARACTERIC	(,	T			62.			
			TEST VOLTAGE VALUES (Volts)						
@ Test Temperature				V _{ILmin}	V_{IHAmin}	V _{ILAmax}	V_{BB}	V _{EE}	
-30°C				-1.890	-1.205	-1.500	From	-5.2	
+25°C			-0.810	-1.850	-1.105	-1.475	Pin	-5.2	
+85°C			-0.700	-1.825	-1.035	-1.440	9	-5.2	
		Pin	TE	ST VOLTAGE	APPLIED	TO PINS LI	STED BELC	w	
Characteristic	Symbol	Under Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{BB}	V _{EE}	(V _{CC}) Gnd
Power Supply Drain Current	Ι _Ε	8		4,7,10,13			5,6,11,12	8	1, 16
Input Current	I _{inH}	4	4	7,10,13			5,6,11,12	8	1, 16
	I _{CBO}	4	19.	7,10,13			5,6,11,12	8,4	1, 16
Output Voltage Logic 1	V _{OH}	2	7,10,13	4			5,6,11,12	8	1, 16
Output Voltage Logic 0	V _{OL}	2	4	7,10,13			5,6,11,12	8	1, 16
Threshold Voltage Logic 1	V _{OHA}	2		7,10,13		4	5,6,11,12	8	1, 16
Threshold Voltage Logic 0	V _{OLA}	2		7,10,13	4		5,6,11,12	8	1, 16
Reference Voltage	V_{BB}	9					5,6,11,12	8	1, 16
Switching Times (50Ω Load)	·		Pu	lse In	Puls	e Out		-3.2 V	+2.0 V
Propagation Delay	t ₄₋₂₊ t ₄₊₂₋	2 2		4		2	5,6,11,12 5,6,11,12	8 8	1, 16 1, 16
Rise Time (20 to 80%)	t ₂₊	2		4		2	5,6,11,12	8	1, 16
Fall Time (20 to 80%)	t ₂₋	2		4	2	2	5,6,11,12	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



NOTES:

G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OF VICE NOT PRESCO

- OTES:

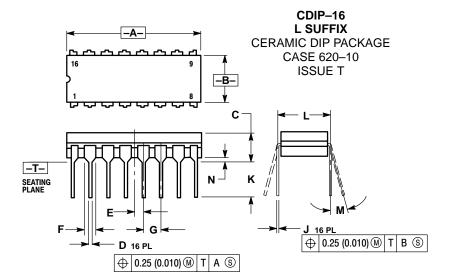
 1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

 4. DIMENSIONING AND TOLERANCING PER ANSI V14 5M 1982
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIM	ETERS	
DIM	MIN MAX		MIN	MAX	
Α	0.385	0.395	9.78	10.03	
В	0.385	0.395	9.78	10.03	
С	0.165	0.180	4.20	4.57	
Ε	0.090	0.110	2.29	2.79	
F	0.013	0.019	0.33	0.48	
G	0.050	BSC	1.27	BSC	
Н	0.026	0.032	0.66	0.81	
J	0.020		0.51		
K	0.025		0.64		
R	0.350	0.356	8.89	9.04	
U	0.350	0.356	8.89	9.04	
٧	0.042	0.048	1.07	1.21	
W	0.042	0.048	1.07	1.21	
Χ	0.042	0.056	1.07	1.42	
Υ		0.020		0.50	
Z	2°	10°	2°	10 °	
G1	0.310	0.330	7.88	8.38	
K1	0.040		1.02		



NOTES:

- ANIES.

 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

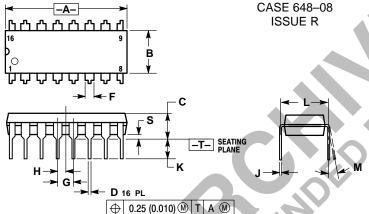
 CONTROLLING DIMENSION: INCH.

 DIMENSION L TO CENTER OF LEAD WHEN

- FORMED PARALLEL.
 DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
С		0.200		5.08	
D	0.015	0.020	0.39	0.50	
E	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300 BSC		7.62	BSC 4	
M	0°	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	

PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE



- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIM	ETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27	BSC	
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10°	0°	10 °	
S	0.020	0.040	0.51	1.01	

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