

# MC100LVELT23

## 3.3V Dual Differential LVPECL to LVTTTL Translator

The MC100LVELT23 is a dual differential LVPECL to LVTTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The small outline 8-lead package and the dual gate design of the LVELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The LVELT23 is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external  $V_{BB}$  reference, the LVELT23 does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the MC100LVELT23 can accept any standard differential LVPECL input referenced from a  $V_{CC}$  of +3.3 V.

- 2.0 ns Typical Propagation Delay
- Maximum Frequency > 180 MHz
- Differential LVPECL Inputs
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V to } 3.8\text{ V}$  with  $GND = 0\text{ V}$
- 24 mA LVTTTL Outputs
- Flow Through Pinouts
- Internal Pulldown and Pullup Resistors



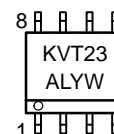
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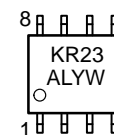
### MARKING DIAGRAMS\*



**SO-8  
D SUFFIX  
CASE 751**



**TSSOP-8  
DT SUFFIX  
CASE 948R**



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

Device	Package	Shipping**
MC100LVELT23D	SO-8	98 Units/Rail
MC100LVELT23DR2	SO-8	2500 Units/Reel
MC100LVELT23DT	TSSOP-8	98 Units/Rail
MC100LVELT23DTR2	TSSOP-8	2500 Units/Reel

†For additional tape and reel information, refer to Brochure BRD8011/D.

MC100LVELT23

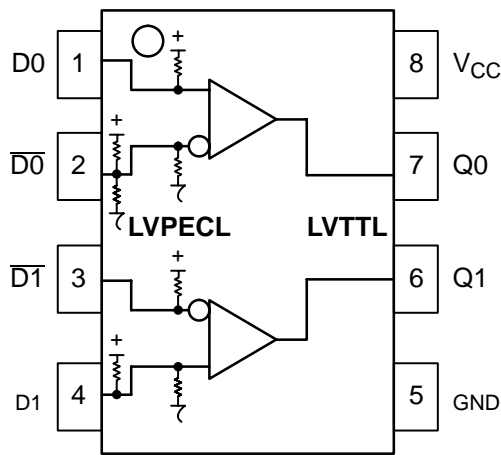


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

PIN DESCRIPTION

PIN	FUNCTION
Qn Dn, $\overline{Dn}$ V <sub>CC</sub> GND	TTL Outputs PECL Differential Inputs Positive Supply Ground

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 K $\Omega$
Internal Input Pullup Resistor	37.5 K $\Omega$
ESD Protection	Human Body Model Machine Model > 1.2 kV > 150 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in
Transistor Count	91
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. ,Refer to Application Note AND8003/D for additional information.

# MC100LVELT23

## MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Power Supply	GND = 0 V		3.8	V
V <sub>I</sub>	Input Voltage	GND = 0 V, V <sub>I</sub> not more positive than V <sub>CC</sub>		3.8	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SO-8 SO-8	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SO-8	41 to 44 ± 5%	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
T <sub>sol</sub>	Solder Temperature	< 2 to 3 Seconds: 245°C desired		265	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.

## LVPECL INPUT DC CHARACTERISTICS V<sub>CC</sub> = 3.3 V; GND = 0 V (Note 3)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>CCH</sub>	Power Supply Current (Outputs set to HIGH)	10	18	25	10	18	25	10	18	25	mA
I <sub>CCL</sub>	Power Supply Current (Outputs set to LOW)	15	26	33	15	26	33	15	26	33	mA
V <sub>IH</sub>	Input HIGH Voltage (Note 5)	2135		2420	2135		2420	2135		2420	mV
V <sub>IL</sub>	Input LOW Voltage (Note 5)	1490		1825	1490		1825	1490		1825	mV
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Notes 4 and 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	D D		0.5			0.5			0.5	μA
		-150			-150			-150			

NOTE: Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. All values vary 1:1 with V<sub>CC</sub>. V<sub>CC</sub> can vary ±0.3 V.

4. V<sub>IHCMR</sub> min varies 1:1 with GND, max varies 1:1 with V<sub>CC</sub>.

5. LVTTTL output R<sub>L</sub> = 500 Ω to GND.

## MC100LVELT23

### LVTTTL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$ ; GND = 0V (Note 6)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage ( $I_{OH} = -3.0\text{ mA}$ ) (Note 7)	2.4			2.4			2.4			V
$V_{OL}$	Output LOW Voltage ( $I_{OL} = 24\text{ mA}$ ) (Note 7)			0.5			0.5			0.5	V
$I_{OS}$	Output Short Circuit Current	-180		-50	-180		-50	-180		-50	mA

NOTE: Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

6. All values vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.3\text{ V}$ .

7. LVTTTL output  $R_L = 500\ \Omega$  to GND.

### AC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$ ; GND = 0 V (Notes 8, 9)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$F_{max}$	Maximum Toggle Frequency (Note 10)	180			180			180			MHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential	1.0	1.5	2.5	1.0	1.7	2.5	1.0	1.7	2.5	ns
$t_{SK++}$ , $t_{SK--}$ , $t_{SKPP}$	Output-to-Output Skew++ Output-to-Output Skew-- Part-to-Part Skew (Note 11)			60 25 500			60 25 500			60 25 500	ps
$t_{JITTER}$	Random Clock Jitter (RMS)		0.5			0.5			0.5		ps
$V_{PP}$	Input Voltage Swing (Differential) (Note 12)	200	800	1000	200	800	1000	200	800	1000	mV
$t_r$ , $t_f$	Output Rise/Fall Times (0.8 V - 2.0 V) $Q, \bar{Q}$	330	600	900	330	600	900	330	650	900	ps

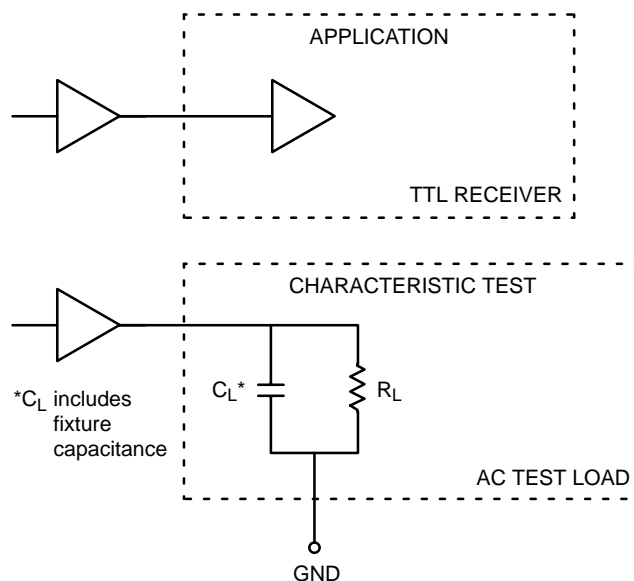
8. All values vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.3\text{ V}$ .

9. LVTTTL output  $R_L = 500\ \Omega$  to GND and  $C_L = 20\text{ pF}$  to GND. Refer to Figure 2.

10.  $F_{max}$  guaranteed for functionality only.  $V_{OL}$  and  $V_{OH}$  levels are guaranteed at DC only.

11. Skews are measured between outputs under identical conditions.

12. 200 mV input guarantees full logic swing at the output.



**Figure 2. TTL Output Loading Used for Device Evaluation**

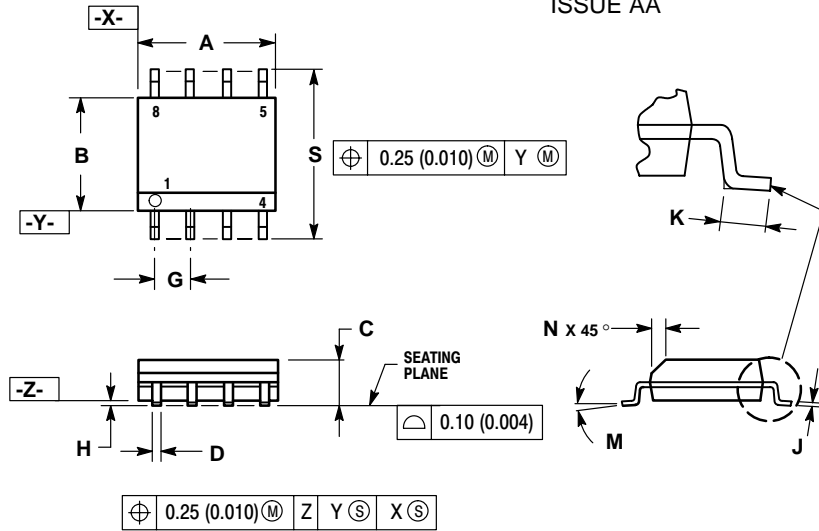
## Resource Reference of Application Notes

- AN1404** - ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** - ECL Clock Distribution Techniques
- AN1406** - Designing with PECL (ECL at +5.0 V)
- AN1503** - ECLinPS I/O SPICE Modeling Kit
- AN1504** - Metastability and the ECLinPS Family
- AN1560** - Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** - Interfacing Between LVDS and ECL
- AN1596** - ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** - Using Wire-OR Ties in ECLinPS Designs
- AN1672** - The ECL Translator Guide
- AND8001** - Odd Number Counters Design
- AND8002** - Marking and Date Codes
- AND8020** - Termination of ECL Logic Devices
- AND8090** - AC Characteristics of ECL Devices

# MC100LVELT23

## PACKAGE DIMENSIONS

**SO-8**  
**D SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751-07  
 ISSUE AA



### NOTES:

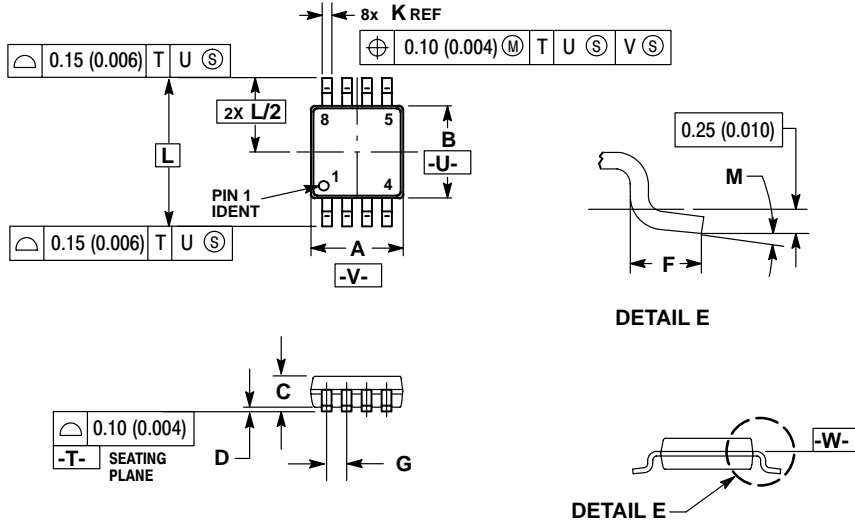
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
E	1.27 BSC		0.050 BSC	
F	0.10	0.25	0.004	0.010
G	0.19	0.25	0.007	0.010
H	0.40	1.27	0.016	0.050
J	0°	8°	0°	8°
K	0.25	0.50	0.010	0.020
M	5.80	6.20	0.228	0.244
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

# MC100LVELT23

## PACKAGE DIMENSIONS


**TSSOP-8**  
**DT SUFFIX**  
 PLASTIC TSSOP PACKAGE  
 CASE 948R-02  
 ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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