# MC74AC257, MC74ACT257

# Quad 2-Input Multiplexer with 3-State Outputs

The MC74AC257/74ACT257 is a quad 2–input multiplexer with 3–state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus–oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Noninverting 3–State Outputs
- Outputs Source/Sink 24 mA
- ′ACT257 Has TTL Compatible Inputs

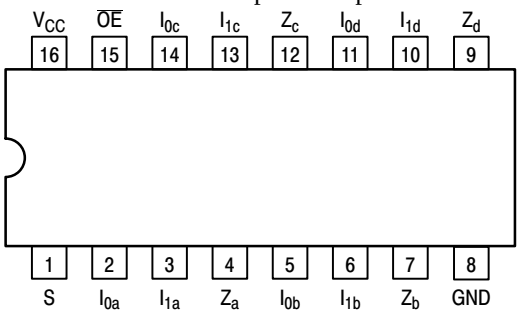


**Figure 1. Pinout: 16–Lead Packages Conductors**
(Top View)

**PIN NAME**

| PIN | FUNCTION |
|---|---|
| S | Common Data Select Input |
| $\overline{OE}$ | 3–State Output Enable Input |
| $I_{0a}$–$I_{0d}$ | Data Inputs from Source 0 |
| $I_{1a}$–$I_{1d}$ | Data Inputs from Source 1 |
| $Z_a$–$Z_d$ | 3–State Multiplexer Outputs |

**TRUTH TABLE**

| Output Enable | Select Input | Data Inputs | | Outputs |
|---|---|---|---|---|
| $\overline{OE}$ | S | $I_0$ | $I_1$ | Z |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | L | X | L |
| L | L | H | X | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

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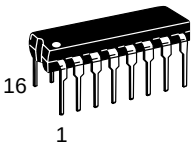
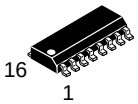
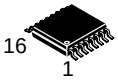


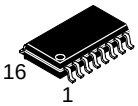

**DIP–16**
**N SUFFIX**
**CASE 648**




**SO–16**
**D SUFFIX**
**CASE 751B**




**TSSOP–16**
**DT SUFFIX**
**CASE 948F**




**EIAJ–16**
**M SUFFIX**
**CASE 966**

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MC74AC257N | PDIP–16 | 25 Units/Rail |
| MC74ACT257N | PDIP–16 | 25 Units/Rail |
| MC74AC257D | SOIC–16 | 48 Units/Rail |
| MC74ACT257D | SOIC–16 | 48 Units/Rail |
| MC74AC257DR2 | SOIC–16 | 2500 Tape & Reel |
| MC74ACT257DR2 | SOIC–16 | 2500 Tape & Reel |
| MC74AC257DT | TSSOP–16 | 96 Units/Rail |
| MC74ACT257DT | TSSOP–16 | 96 Units/Rail |
| MC74AC257DTR2 | TSSOP–16 | 2500 Tape & Reel |
| MC74ACT257DTR2 | TSSOP–16 | 2500 Tape & Reel |
| MC74ACT257M | EIAJ–16 | 50 Units/Rail |
| MC74AC257MEL | EIAJ–16 | 2000 Tape & Reel |
| MC74ACT257MEL | EIAJ–16 | 2000 Tape & Reel |

**DEVICE MARKING INFORMATION**

See general marking information in the device marking section on page 7 of this data sheet.

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July, 2002 – Rev. 6
Publication Order Number:
MC74AC257/D

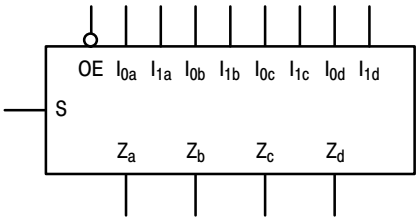



**Figure 2. Logic Symbol**

## FUNCTIONAL DESCRIPTION

The MC74AC257/74ACT257 is a quad 2–input multiplexer with 3–state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the $I_{0x}$ inputs are selected and when Select is HIGH, the $I_{1x}$ inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4–pole, 2–position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

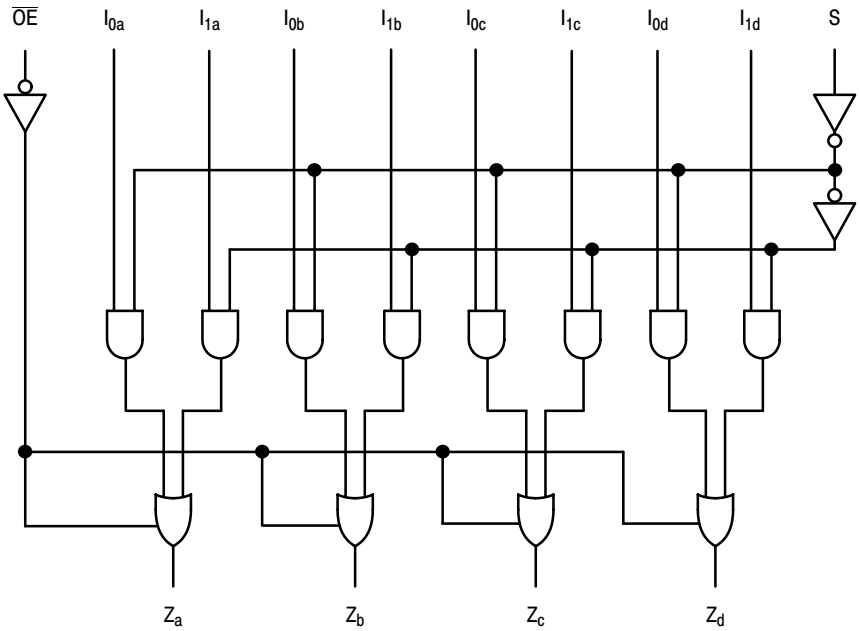
$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$

$Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$

$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$

$Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3–state devices whose outputs are tied together are designed so there is no overlap.




NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Figure 3. Logic Diagram**

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | –0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | –0.5 to $V_{CC}$ +0.5 | V |
| $V_{OUT}$ | DC Output Voltage (Referenced to GND) | –0.5 to $V_{CC}$ +0.5 | V |
| $I_{IN}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{OUT}$ | DC Output Sink/Source Current, per Pin | ±50 | mA |
| $I_{CC}$ | DC $V_{CC}$ or GND Current per Output Pin | ±50 | mA |
| $T_{stg}$ | Storage Temperature | –65 to +150 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | ′AC | 2.0 | 5.0 | 6.0 | V |
| | | ′ACT | 4.5 | 5.0 | 5.5 | |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage (Ref. to GND) | | 0 | – | $V_{CC}$ | V |
| $t_r$, $t_f$ | Input Rise and Fall Time (Note 1)<br>′AC Devices except Schmitt Inputs | $V_{CC}$ @ 3.0 V | – | 150 | – | ns/V |
| | | $V_{CC}$ @ 4.5 V | – | 40 | – | |
| | | $V_{CC}$ @ 5.5 V | – | 25 | – | |
| $t_r$, $t_f$ | Input Rise and Fall Time (Note 2)<br>′ACT Devices except Schmitt Inputs | $V_{CC}$ @ 4.5 V | – | 10 | – | ns/V |
| | | $V_{CC}$ @ 5.5 V | – | 8.0 | – | |
| $T_J$ | Junction Temperature (PDIP) | | – | – | 140 | °C |
| $T_A$ | Operating Ambient Temperature Range | | –40 | 25 | 85 | °C |
| $I_{OH}$ | Output Current – High | | – | – | –24 | mA |
| $I_{OL}$ | Output Current – Low | | – | – | 24 | mA |

1. 1. $V_{in}$ from 30% to 70% $V_{CC}$; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. 2. $V_{in}$ from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

**DC CHARACTERISTICS**

| Symbol | Parameter | $V_{CC}$ (V) | 74AC $T_A$ = +25°C Typ | 74AC $T_A$ = +25°C Guaranteed Limits | 74AC $T_A$ = –40°C to +85°C Guaranteed Limits | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Level Input Voltage | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75 | 2.1<br>3.15<br>3.85 | 2.1<br>3.15<br>3.85 | V | $V_{OUT}$ = 0.1 V or $V_{CC}$ – 0.1 V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75 | 0.9<br>1.35<br>1.65 | 0.9<br>1.35<br>1.65 | V | $V_{OUT}$ = 0.1 V or $V_{CC}$ – 0.1 V |
| $V_{OH}$ | Minimum High Level Output Voltage | 3.0<br>4.5<br>5.5 | 2.99<br>4.49<br>5.49 | 2.9<br>4.4<br>5.4 | 2.9<br>4.4<br>5.4 | V | $I_{OUT}$ = –50 μA |
| | | 3.0<br>4.5<br>5.5 | –<br>–<br>– | 2.56<br>3.86<br>4.86 | 2.46<br>3.76<br>4.76 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OH}$ –12 mA<br>–24 mA<br>–24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 3.0<br>4.5<br>5.5 | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V | $I_{OUT}$ = 50 μA |
| | | 3.0<br>4.5<br>5.5 | –<br>–<br>– | 0.36<br>0.36<br>0.36 | 0.44<br>0.44<br>0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OL}$ 12 mA<br>24 mA<br>24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | – | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OZ}$ | Maximum 3–State Current | 5.5 | – | ±0.5 | ±5.0 | μA | $V_I$ (OE) = $V_{IL}$, $V_{IH}$<br>$V_I$ = $V_{CC}$, GND<br>$V_O$ = $V_{CC}$, GND |
| $I_{OLD}$ | †Minimum Dynamic Output Current | 5.5 | – | – | 75 | mA | $V_{OLD}$ = 1.65 V Max |
| $I_{OHD}$ | | 5.5 | – | – | –75 | mA | $V_{OHD}$ = 3.85 V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | – | 8.0 | 80 | μA | $V_{IN}$ = $V_{CC}$ or GND |

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: $I_{IN}$ and $I_{CC}$ @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V $V_{CC}$.

**AC CHARACTERISTICS** (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

| Symbol | Parameter | $V_{CC}$* (V) | 74AC $T_A$ = +25°C $C_L$ = 50 pF | | | 74AC $T_A$ = –40°C to +85°C $C_L$ = 50 pF | | Unit | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay<br>$I_n$ to $Z_n$ | 3.3<br>5.0 | 1.5<br>1.5 | 5.0<br>4.0 | 8.5<br>6.0 | 1.0<br>1.0 | 9.0<br>7.0 | ns | 3–5 |
| $t_{PHL}$ | Propagation Delay<br>$I_n$ to $Z_n$ | 3.3<br>5.0 | 1.5<br>1.5 | 6.0<br>4.5 | 8.5<br>6.0 | 1.0<br>1.0 | 9.0<br>7.0 | ns | 3–5 |
| $t_{PLH}$ | Propagation Delay<br>S to $Z_n$ | 3.3<br>5.0 | 1.5<br>1.5 | 7.0<br>5.0 | 10.5<br>7.5 | 1.5<br>1.0 | 11.5<br>8.5 | ns | 3–6 |
| $t_{PHL}$ | Propagation Delay<br>S to $Z_n$ | 3.3<br>5.0 | 1.5<br>1.5 | 7.5<br>5.5 | 10.5<br>7.5 | 1.5<br>1.0 | 11.5<br>8.5 | ns | 3–6 |
| $t_{PZH}$ | Output Enable Time | 3.3<br>5.0 | 1.5<br>1.5 | 6.5<br>5.0 | 9.5<br>7.5 | 1.0<br>1.0 | 10.5<br>8.5 | ns | 3–7 |
| $t_{PZL}$ | Output Enable Time | 3.3<br>5.0 | 1.5<br>1.5 | 5.5<br>5.0 | 9.0<br>8.5 | 1.0<br>1.0 | 10.0<br>9.5 | ns | 3–8 |
| $t_{PHZ}$ | Output Disable Time | 3.3<br>5.0 | 1.5<br>1.5 | 5.5<br>5.0 | 10.0<br>9.0 | 1.0<br>1.0 | 11.0<br>10.0 | ns | 3–7 |
| $t_{PLZ}$ | Output Disable Time | 3.3<br>5.0 | 1.5<br>1.5 | 5.5<br>5.0 | 9.0<br>8.0 | 1.0<br>1.0 | 10.0<br>9.0 | ns | 3–8 |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

**DC CHARACTERISTICS**

| Symbol | Parameter | $V_{CC}$ (V) | 74ACT $T_A$ = +25°C Typ | 74ACT $T_A$ = +25°C Guaranteed Limits | 74ACT $T_A$ = –40°C to +85°C Guaranteed Limits | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 2.0<br>2.0 | 2.0<br>2.0 | V | $V_{OUT}$ = 0.1 V or $V_{CC}$ – 0.1 V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 0.8<br>0.8 | 0.8<br>0.8 | V | $V_{OUT}$ = 0.1 V or $V_{CC}$ – 0.1 V |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5<br>5.5 | 4.49<br>5.49 | 4.4<br>5.4 | 4.4<br>5.4 | V | $I_{OUT}$ = –50 μA |
| | | 4.5<br>5.5 | –<br>– | 3.86<br>4.86 | 3.76<br>4.76 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OH}$ –24 mA<br>–24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5<br>5.5 | 0.001<br>0.001 | 0.1<br>0.1 | 0.1<br>0.1 | V | $I_{OUT}$ = 50 μA |
| | | 4.5<br>5.5 | –<br>– | 0.36<br>0.36 | 0.44<br>0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OL}$ 24 mA<br>24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | – | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $\Delta I_{CCT}$ | Additional Max. $I_{CC}$/Input | 5.5 | 0.6 | – | 1.5 | mA | $V_I$ = $V_{CC}$ – 2.1 V |
| $I_{OZ}$ | Maximum 3–State Current | 5.5 | – | ±0.5 | ±5.0 | μA | $V_I$ (OE) = $V_{IL}$, $V_{IH}$<br>$V_I$ = $V_{CC}$, GND<br>$V_O$ = $V_{CC}$, GND |
| $I_{OLD}$ | †Minimum Dynamic Output Current | 5.5 | – | – | 75 | mA | $V_{OLD}$ = 1.65 V Max |
| $I_{OHD}$ | | 5.5 | – | – | –75 | mA | $V_{OHD}$ = 3.85 V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | – | 8.0 | 80 | μA | $V_{IN}$ = $V_{CC}$ or GND |

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

**AC CHARACTERISTICS** (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

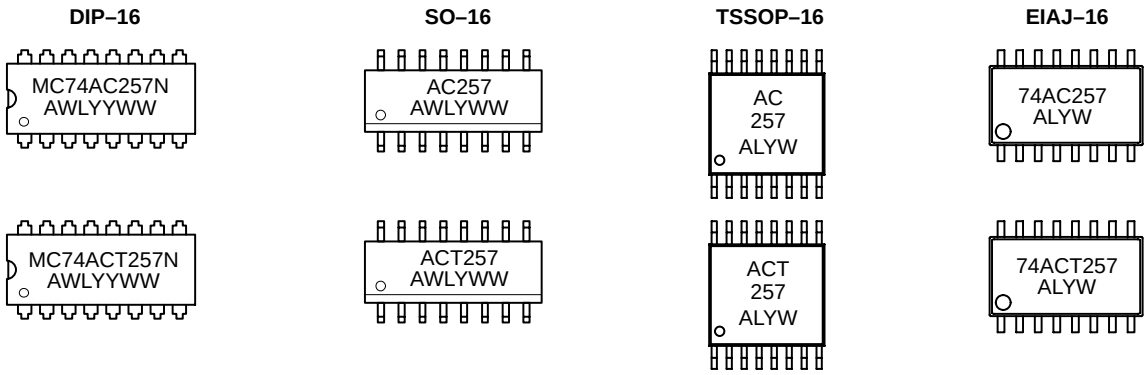
| Symbol | Parameter | $V_{CC}$* (V) | 74ACT $T_A$ = +25°C $C_L$ = 50 pF | | | 74ACT $T_A$ = –40°C to +85°C $C_L$ = 50 pF | | Unit | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay $I_n$ to $Z_n$ | 5.0 | 1.5 | 5.0 | 7.0 | 1.0 | 7.5 | ns | 3–6 |
| $t_{PHL}$ | Propagation Delay $I_n$ to $Z_n$ | 5.0 | 2.0 | 6.0 | 7.5 | 1.5 | 8.5 | ns | 3–6 |
| $t_{PLH}$ | Propagation Delay S to $Z_n$ | 5.0 | 2.0 | 7.0 | 9.5 | 1.5 | 10.5 | ns | 3–6 |
| $t_{PHL}$ | Propagation Delay S to $Z_n$ | 5.0 | 2.5 | 7.0 | 10.5 | 2.0 | 11.5 | ns | 3–6 |
| $t_{PZH}$ | Output Enable Time | 5.0 | 2.0 | 6.0 | 8.0 | 1.5 | 9.0 | ns | 3–7 |
| $t_{PZL}$ | Output Enable Time | 5.0 | 2.0 | 6.0 | 8.0 | 1.5 | 9.0 | ns | 3–8 |
| $t_{PHZ}$ | Output Disable Time | 5.0 | 2.5 | 6.5 | 9.0 | 1.5 | 10.0 | ns | 3–7 |
| $t_{PLZ}$ | Output Disable Time | 5.0 | 2.0 | 6.0 | 7.5 | 1.5 | 8.5 | ns | 3–8 |

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

**CAPACITANCE**

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | 50 | pF | $V_{CC}$ = 5.0 V |

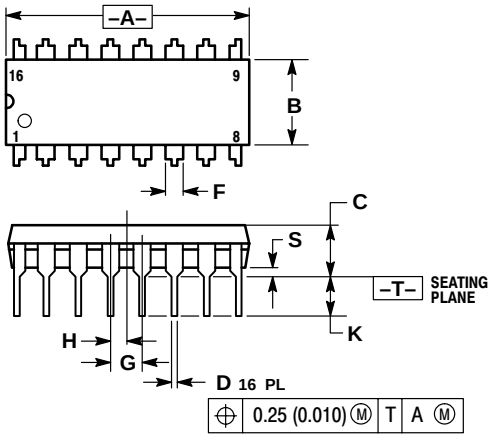
**MARKING DIAGRAMS**

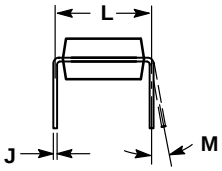



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## PACKAGE DIMENSIONS

**PDIP–16**
**N SUFFIX**
16 PIN PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

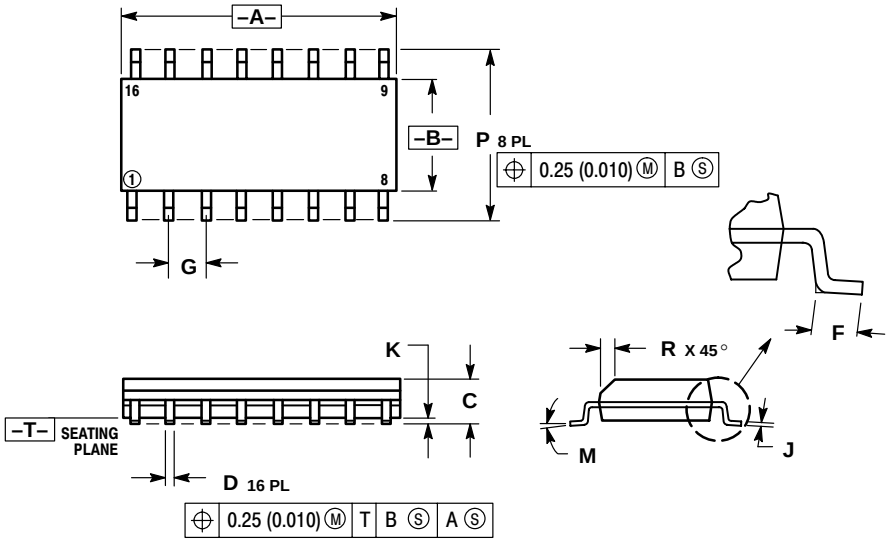



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

**SO–16**
**D SUFFIX**
16 PIN PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

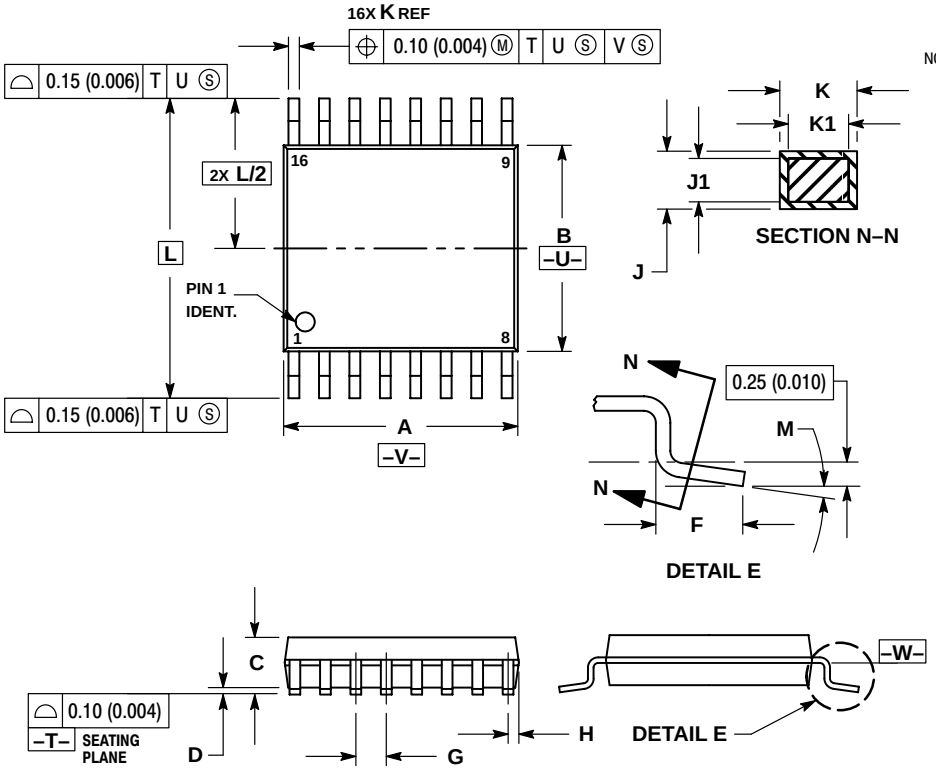



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

## PACKAGE DIMENSIONS

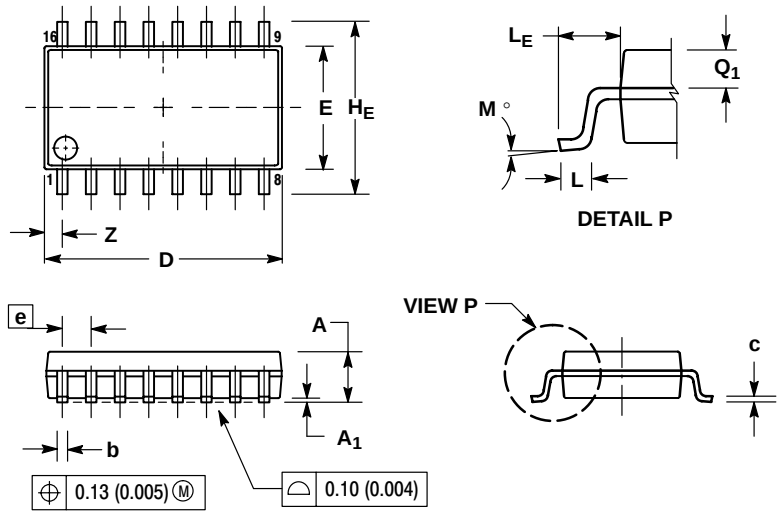
### TSSOP–16
### DT SUFFIX
16 PIN PLASTIC TSSOP PACKAGE
CASE948F–01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### EIAJ–16
### M SUFFIX
16 PIN PLASTIC EIAJ PACKAGE
CASE966–01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

# Notes

# Notes

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