MC10198

Monostable Multivibrator

The MC10198 is a retriggerable monostable multivibrator. Two enable inputs permit triggering on any combination of positive or negative edges as shown in the accompanying table. The trigger input is buffered by Schmitt triggers making it insensitive to input rise and fall times.

The pulse width is controlled by an external capacitor and resistor. The resistor sets a current which is the linear discharge rate of the capacitor. Also, the pulse width can be controlled by an external current source or voltage (see applications information).

For high–speed response with minimum delay, a hi–speed input is also provided. This input bypasses the internal Schmitt triggers and the output responds within 2 nanoseconds typically.

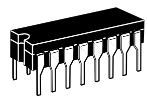
Output logic and threshold levels are standard MECL 10,000. Test conditions are per Table 2. Each “Precondition” referred to in Table 2 is per the sequence of Table 1.

- P_D = 415 mW typ/pkg (No Load)
- t_{pd} = 4.0 ns typ Trigger Input to Q
- 2.0 ns typ Hi–Speed Input to Q
- Min Timing Pulse Width — PW_{Qmin} — 10 ns typ[1]
- Max Timing Pulse Width — PW_{Qmax} — >10 ms typ[2]
- Min Trigger Pulse Width — PW_T — 2.0 ns typ
- Min Hi–Speed Trigger Pulse Width — PW_{HS} — 3.0 ns typ
- Enable Setup Time — t_{set} — 1.0 ns typ
- Enable Hold Time — t_{hold} — 1.0 ns typ
- [1] C_{Ext} = 0 (Pin 4 open), R_{Ext} = 0 (Pin 6 to V_{EE})
- [2] C_{Ext} = 10 mF, R_{Ext} = 2.7 kW

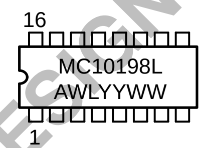
ON Semiconductor

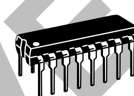
http://onsemi.com

MARKING DIAGRAMS

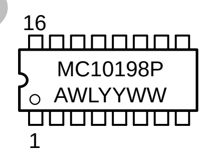


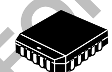
CDIP–16
L SUFFIX
CASE 620



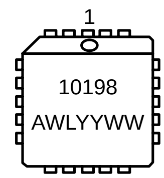


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

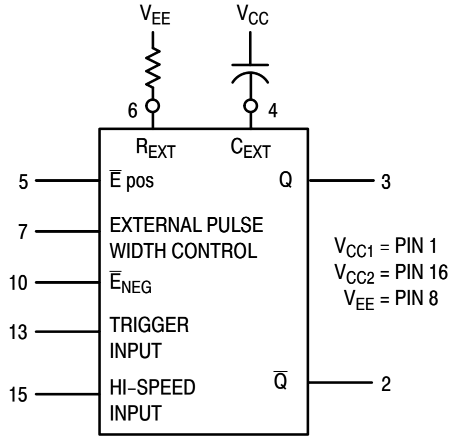


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

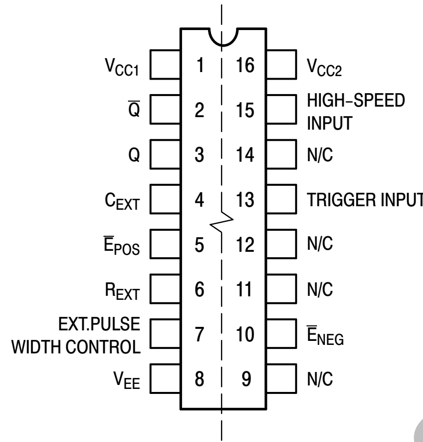
ORDERING INFORMATION

Device	Package	Shipping
MC10198L	CDIP–16	25 Units / Rail
MC10198P	PDIP–16	25 Units / Rail
MC10198FN	PLCC–20	46 Units / Rail

LOGIC DIAGRAM



DIP PIN ASSIGNMENT

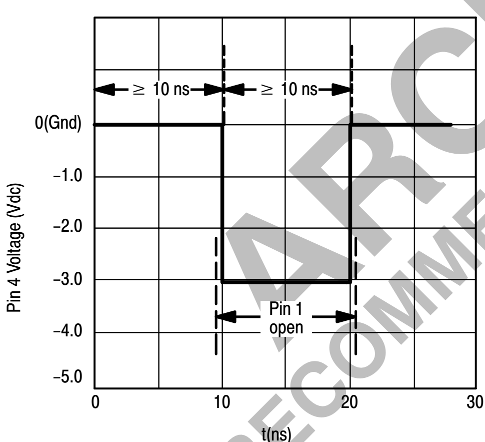


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

TRUTH TABLE

INPUT		OUTPUT
$\overline{E}_{Pos}$	$\overline{E}_{Neg}$	
L	L	Triggers on both positive & negative input slopes
L	H	Triggers on positive input slope
H	L	Triggers on negative input slope
H	H	Trigger is disabled

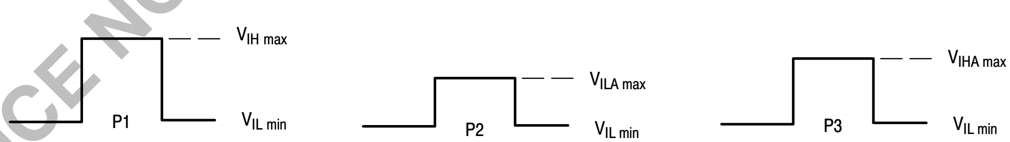
TABLE 1 — PRECONDITION SEQUENCE



1. At t = 0 a.) Apply V_{IHmax} to Pin 5 and 10.
   b.) Apply V_{ILmin} to Pin 15.
   c.) Ground Pin 4.
2. At t ≥ 10 ns a.) Open Pin 1.
   b.) Apply –3.0 Vdc to Pin 4. Hold these conditions for ≥ 10 ns.
3. Return Pin 4 to Ground and perform test as indicated in Table 2.

TABLE 2 — CONDITIONS FOR TESTING OUTPUT LEVELS

(See Table 1 for Precondition Sequence)



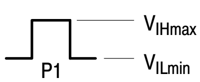
Pins 1, 16 = V_{CC} = Ground
Pins 6, 8 = V_{EE} = –5.2 Vdc
Outputs loaded 50 Ω to –2.0 Vdc

Test	P.U.T.	Pin Conditions 5	10	13	15
Precondition					
V_{OH}	2			$V_{IL\ min}$	
V_{OH}	3			P1	
Precondition					
V_{OL}	3			$V_{IL\ min}$	
V_{OL}	2			P1	
Precondition					
V_{OHA}	2				$V_{ILA\ max}$
V_{OHA}	3				$V_{IHA\ min}$
Precondition					
V_{OHA}	2			$V_{IL\ min}$	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2			P2	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2		$V_{IH\ max}$	P2	
V_{OHA}	3		$V_{IH\ max}$	P3	
Precondition					
V_{OHA}	2		$V_{IH\ max}$	P1	
V_{OHA}	3		$V_{IH\ max}$	P1	

Test	P.U.T.	Pin Conditions 5	10	13	15
Precondition					
V_{OHA}	2		$V_{IHA\ min}$	P1	
V_{OHA}	3		$V_{ILA\ max}$	P1	
Precondition					
V_{OLA}	3				$V_{ILA\ max}$
V_{OLA}	2				$V_{IHA\ min}$
Precondition					
V_{OLA}	2			$V_{IL\ min}$	
V_{OLA}	3			$V_{IL\ min}$	
Precondition					
V_{OLA}	3			P2	
V_{OLA}	2			P3	
Precondition					
V_{OLA}	3		$V_{IH\ max}$	P2	
V_{OLA}	2		$V_{IH\ max}$	P3	
Precondition					
V_{OLA}	3	$V_{IHA\ min}$	$V_{IH\ max}$	P1	
V_{OLA}	2	$V_{ILA\ max}$	$V_{IH\ max}$	P1	
Precondition					
V_{OLA}	3	$V_{IH\ max}$	$V_{IHA\ min}$	P1	
V_{OLA}	2	$V_{IH\ max}$	$V_{ILA\ max}$	P1	

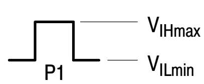
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		110		80	100		110	mAdc
Input Current	I_{inH}	5, 10 13 15		415 350 560			260 220 350		260 220 350	µAdc
	I_{inL}	5	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										
Trigger Input	t_{T+Q+} t_{T-Q+}	3 3	2.5 2.5	6.5 6.5	2.5 2.5	4.0 4.0	5.5 5.5	2.5 2.5	6.5 6.5	ns
High Speed Trigger Input	t_{HS+Q+}	3	1.5	3.2	1.5	2.0	2.8	1.5	3.2	ns
Minimum Timing Pulse Width	PW_{Qmin}	3				10.0				ns
Maximum Timing Pulse Width	PW_{Qmax}	3				>10				ms
Min Trigger Pulse Width	PW_T	3				2.0				ns
Min Hi–Spd Trig Pulse Width	PW_{HS}	3				3.0				ns
Rise Time (20 to 80%)		3	1.5	4.0	1.5		3.5	1.5	4.0	ns
Fall Time (20 to 80%)		3	1.5	4.0	1.5		3.5	1.5	4.0	ns
Enable Setup Time	t_{setup} (E)	3				1.0				ns
Enable Hold Time	t_{hold} (E)	3				1.0				ns

1. The monostable is in the timing mode at the time of this test.
2. C_{EXT} = 0 (Pin 4 Open); R_{EXT} = 0 (Pin 6 tied to V_{EE}).
3. C_{EXT} = 10µF (Pin); R_{EXT} = 2.7k (Pin 6).
4. 

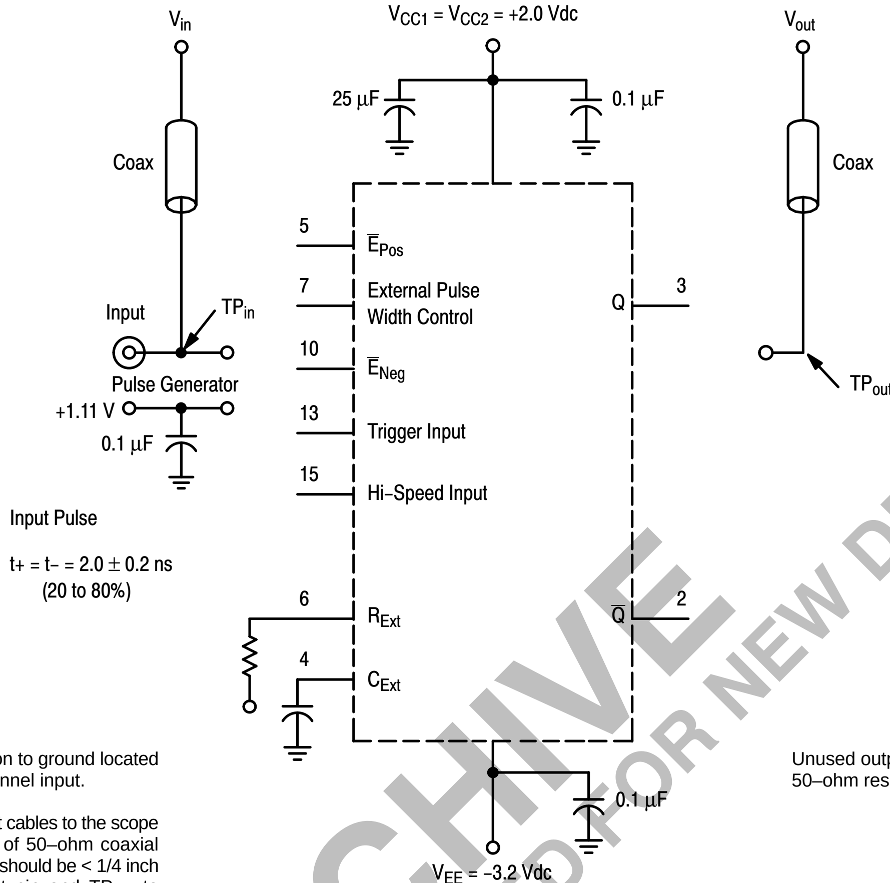
ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)					
		@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
		–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
		+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
		+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
		Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
Characteristic	**Symbol**		V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					6, 8	1, 4, 16
Input Current	I_{inH}	5, 10	5,10				6, 8	1, 4, 16
		13	13				6, 8	1, 4, 16
		15	15				6, 8	1, 4, 16
	I_{inL}	5		5			6, 8	1, 4, 16
Output Voltage Logic 1	V_{OH}	2		13			6, 8	1, 4, 16
		3	13 (4.)				6, 8	1, 4, 16
Output Voltage Logic 0	V_{OL}	2	13 (4.)				6, 8	1, 4, 16
		3		13			6, 8	1, 4, 16
Threshold Voltage Logic 1	V_{OHA}	2				15	6, 8	1, 16, 4
		3			15		6, 8	1, 16, 4
Threshold Voltage Logic 0	V_{OLA}	2			15		6, 8	1, 16, 4
		3				15	6, 8	1, 16, 4
Switching Times (50Ω Load)			+1.11V		Pulse In	Pulse Out	–3.2 V	+2.0 V
Trigger Input	t_{T+Q+}	3	10		13	3	6, 8	1, 16, 4
	$t_{T–Q+}$	3	5		13	3	6, 8	1, 16, 4
High Speed Trigger Input	t_{HS+Q+}	3			15	3	6, 8	1, 16, 4
Minimum Timing Pulse Width	PW_{Qmin}	3				Note 2.	6, 8	1, 16, 4
Maximum Timing Pulse Width	PW_{Qmax}	3				Note 3.	6, 8	1, 16, 4
Minimum Trigger Pulse Width	PW_T	3			13	3	6, 8	1, 16, 4
Minimum Hi–Spd Trigger Pulse Width	PW_{HS}	3			15	3	6, 8	1, 16, 4
Rise Time (20 to 80%)		3					6, 8	1, 16, 4
Fall Time (20 to 80%)		3					6, 8	1, 16, 4
Enable Setup Time	t_{setup} (E)	3			5	3	6, 8	1, 16, 4
Enable Hold Time	t_{hold} (E)	3			5	3	6, 8	1, 16, 4

1. The monostable is in the timing mode at the time of this test.
2. C_{EXT} = 0 (Pin 4 Open); R_{EXT} = 0 (Pin 6 tied to V_{EE}).
3. C_{EXT} = 10µF (Pin); R_{EXT} = 2.7k (Pin 6).
4. 

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

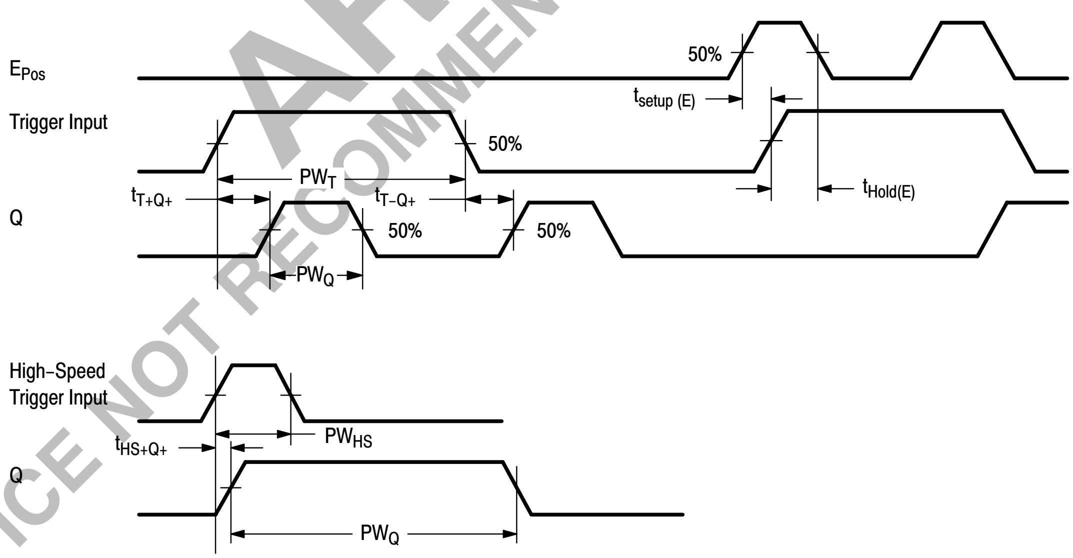
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50–ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50–ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are tied to a 50–ohm resistor to ground.



APPLICATIONS INFORMATION

Circuit Operation:

1. PULSE WIDTH TIMING — The pulse width is determined by the external resistor and capacitor. The MC10198 also has an internal resistor (nominally 284 ohms) that can be used in series with R_{Ext}. Pin 7, the external pulse width control, is a constant voltage node (–3.60 V nominally). A resistance connected in series from this node to V_{EE} sets a constant timing current I_T. This current determines the discharge rate of the capacitor:

where

ΔT = pulse width

ΔV = 1.9 V change in capacitor voltage

Then: $I_T = C_{Ext} \dfrac{\Delta V}{\Delta T}$

If $R_{Ext} + R_{Int}$ are in series to V_{EE}:

$I_T = [(-3.60\ V) - (-5.2\ V)] \div [R_{Ext} + 284\ \Omega]$

$I_T = 1.6\ V/(R_{Ext} + 284)$

The timing equation becomes: $\Delta T = C_{Ext} \dfrac{1.9\ V}{I_T}$

$\Delta T = [(C_{Ext})(1.9\ V)] \div [1.6\ V/(R_{Ext} + 284)]$

$\Delta T = C_{Ext}\ (R_{Ext} + 284)\ 1.19$

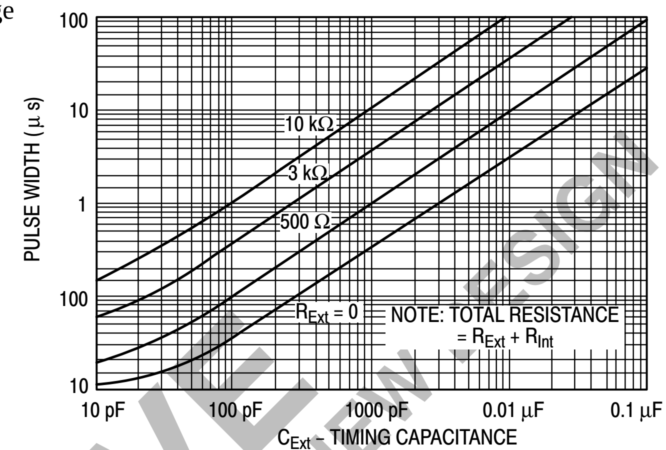
where ΔT = Sec

R_{Ext} = Ohms

C_{Ext} = Farads

Figure 2 shows typical curves for pulse width versus C_{Ext} and R_{Ext} (total resistance includes R_{Int}). Any low leakage capacitor can be used and R_{Ext} can vary from 0 to 16 k–ohms.

FIGURE 2 – TIMING PULSE WIDTH versus C_{Ext} and R_{Ext}



2. TRIGGERING —The $\overline{E}_{pos}$ and $\overline{E}_{Neg}$ inputs control the trigger input. The MC10198 can be programmed to trigger on the positive edge, negative edge, or both. Also, the trigger input can be totally disabled. The truth table is shown on the first page of the data sheet.

The device is totally retriggerable. However, as duty cycle approaches 100%, pulse width jitter can occur due to the recovery time of the circuit. Recovery time is basically dependent on capacitance C_{Ext}. Figure 3 shows typical recovery time versus capacitance at I_T = 5 mA.

FIGURE 1 —

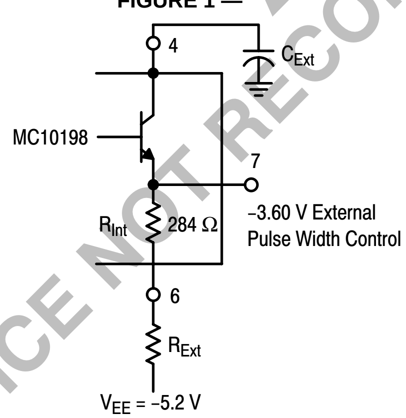
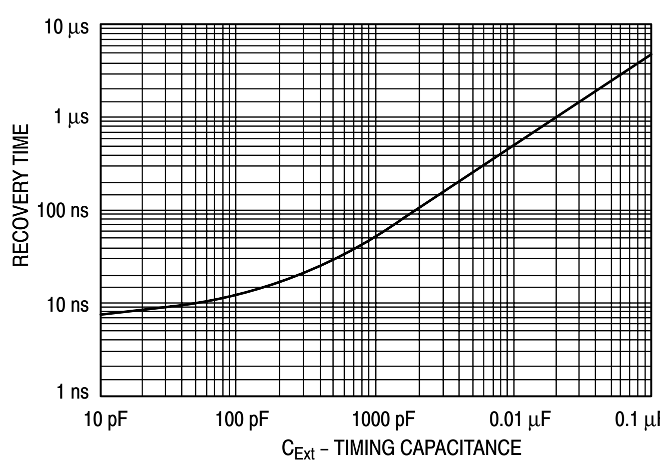


FIGURE 3 — RECOVERY TIME versus C_{Ext} @ I_T = 5 mA



3. HI–SPEED INPUT — This input is used for stretching very narrow pulses with minimum delay between the output pulse and the trigger pulse. The trigger input should be disabled when using the high–speed input. The MC10198 triggers on the rising edge, using this input, and input pulse width should narrow, typically less than 10 nanoseconds.

USAGE RULES:

1. Capacitor lead lengths should be kept very short to minimize ringing due to fast recovery rise times.
2. The $\overline{E}$ inputs should <u>not</u> be tied to ground to establish a high logic level. A resistor divider or diode can be used to establish a –0.7 to –0.9 voltage level.
3. For optimum temperature stability; 0.5 mA is the best timing current I_T. The device is designed to have a constant voltage at the EXTERNAL PULSE WIDTH CONTROL over temperature at this current value.
4. Pulse Width modulation can be attained with the EXTERNAL PULSE WIDTH CONTROL. The timing current can be altered to vary the pulse width. Two schemes are:
   a. The internal resistor is not used. A dependent current source is used to set the timing current as shown in Figure 4. A graph of pulse width versus timing current (C_{Ext} = 13 pF) is shown in Figure 5.
   b. A control voltage can also be used to vary the pulse width using an additional resistor (Figure 6). The current ($I_T + I_C$) is set by the voltage drop across $R_{Int} + R_{Ext}$. The control current IC modifies I_T and alters the pulse width. Current I_C should never force I_T to zero. R_C typically 1 kΩ.

FIGURE 4 —

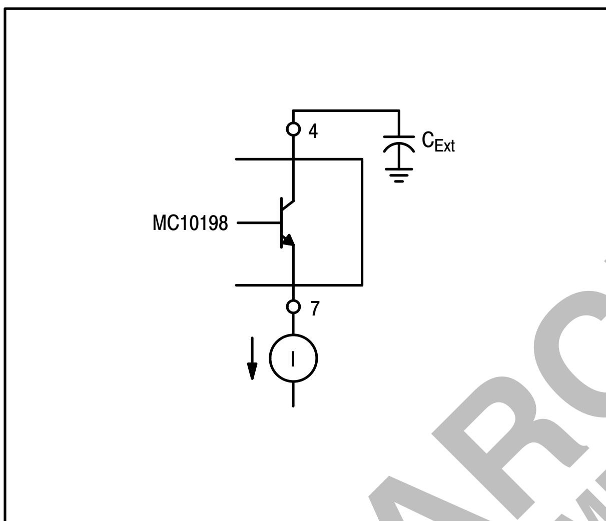


FIGURE 5 — PULSE WIDTH versus I_T @ C_{Ext} = 13 pF

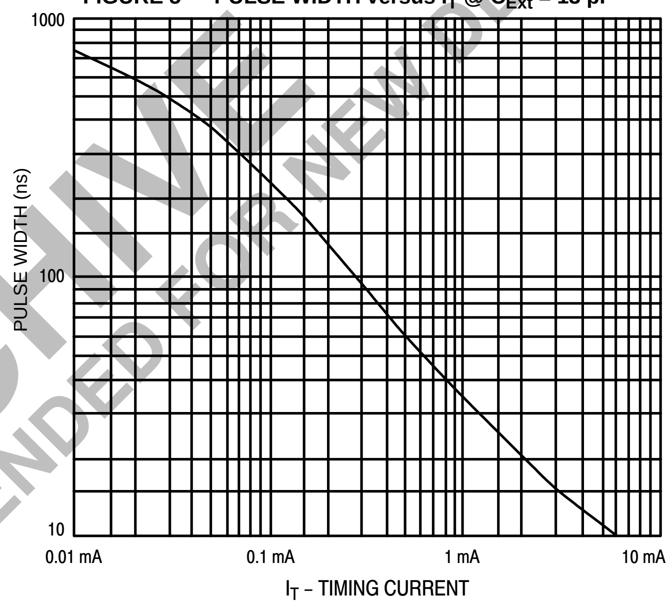
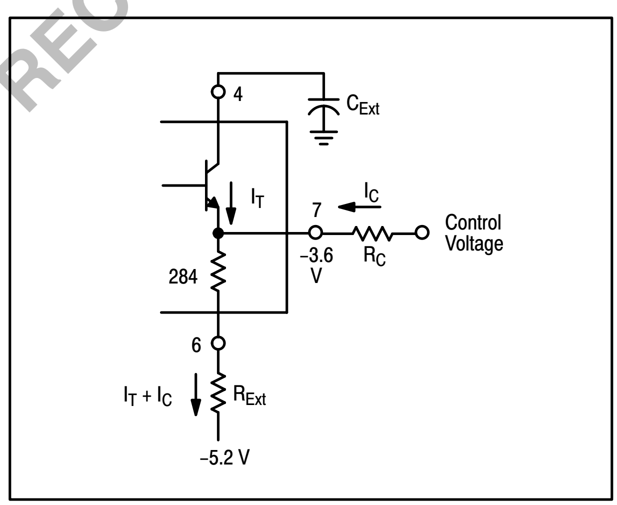
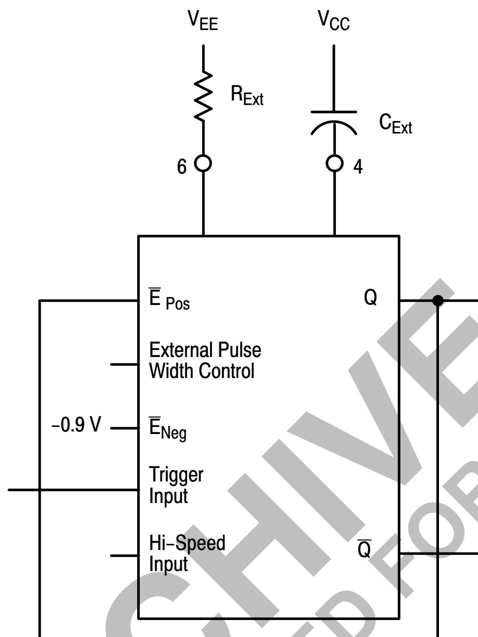


FIGURE 6 —



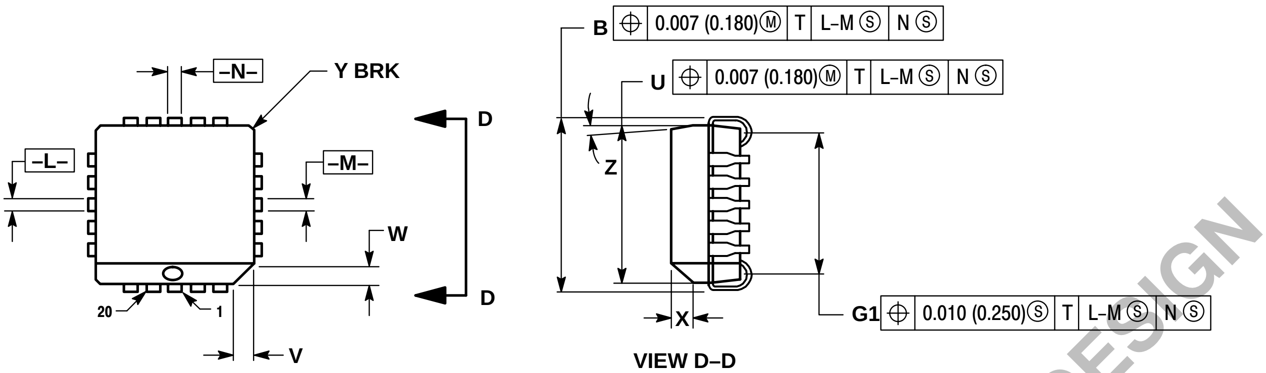
5. The MC10198 can be made non–retriggerable. The Q output is fed back to disable the trigger input during the triggered state (Logic Diagram). Figure 7 shows a positive triggered configuration; a similar configuration can be made for negative triggering.

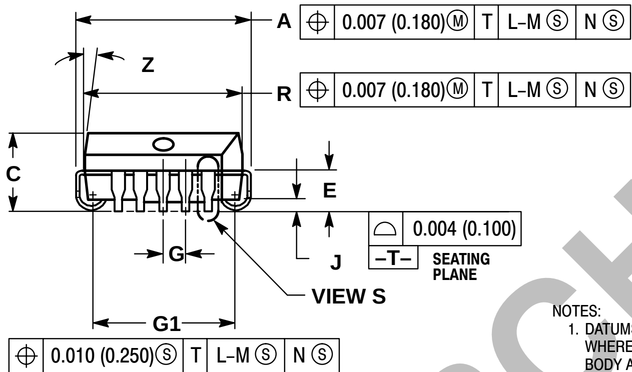
FIGURE 7 —

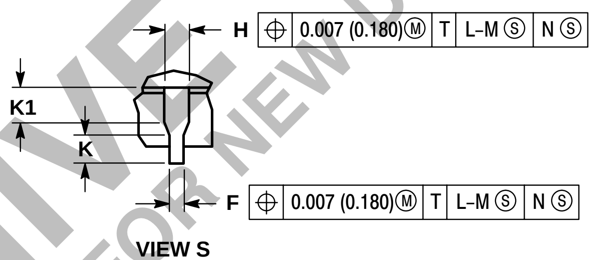


PACKAGE DIMENSIONS

PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C





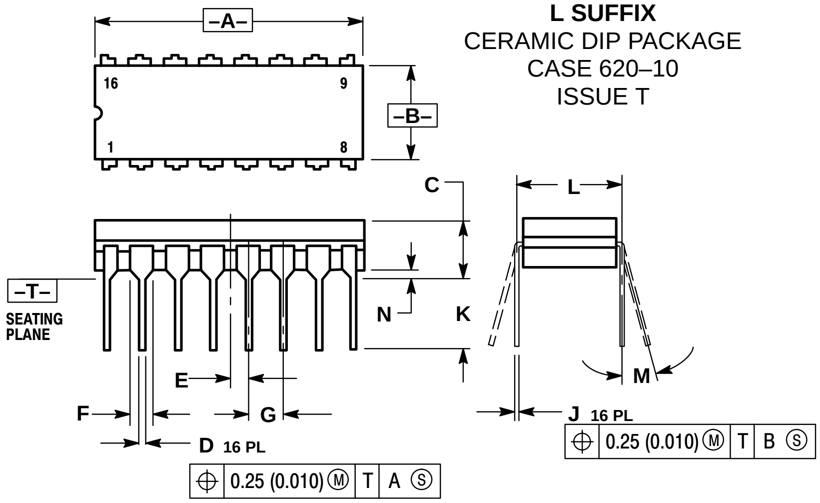


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

PACKAGE DIMENSIONS

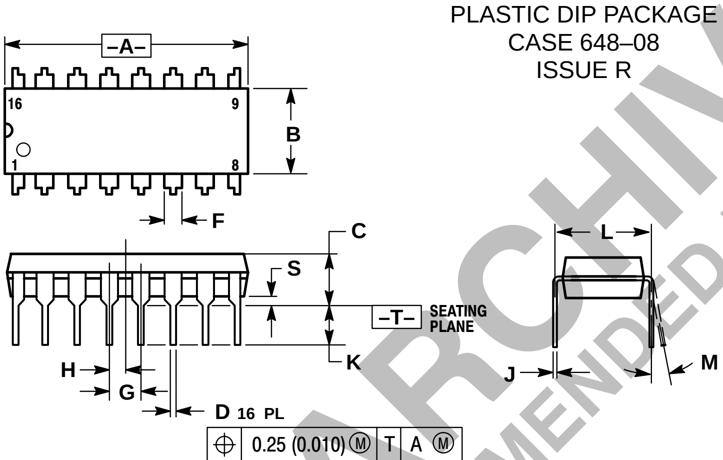
CDIP–16
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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