

# NTD32N06L

## Power MOSFET 32 Amps, 60 Volts, Logic Level N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Features

- Smaller Package than MTB30N06VL
- Lower  $R_{DS(on)}$
- Lower  $V_{DS(on)}$
- Lower Total Gate Charge
- Lower and Tighter  $V_{SD}$
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	60	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 10\text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-to-Source Voltage	$V_{GS}$	$\pm 15$	Vdc
– Continuous	$V_{GS}$	$\pm 20$	
– Non-Repetitive ( $t_p \leq 10\text{ ms}$ )			
Drain Current	$I_D$	32	Adc
– Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	22	
– Continuous @ $T_A = 100^\circ\text{C}$	$I_{DM}$	90	Apk
– Single Pulse ( $t_p \leq 10\text{ }\mu\text{s}$ )			
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	93.75	W
Derate above $25^\circ\text{C}$		0.625	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1.)		2.88	W
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2.)		1.5	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	$-55$ to $+175$	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ (Note 3.) ( $V_{DD} = 50\text{ Vdc}$ , $V_{GS} = 5\text{ Vdc}$ , $L = 1.0\text{ mH}$ , $I_{L(pk)} = 25\text{ A}$ , $V_{DS} = 60\text{ Vdc}$ , $R_G = 25\text{ }\Omega$ )	$E_{AS}$	313	mJ
Thermal Resistance	$R_{\theta JC}$	1.6	$^\circ\text{C/W}$
– Junction-to-Case	$R_{\theta JA}$	52	
– Junction-to-Ambient (Note 1.)	$R_{\theta JA}$	100	
– Junction-to-Ambient (Note 2.)			
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

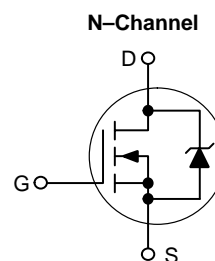
1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in<sup>2</sup>).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).
3. Repetitive rating; pulse width limited by maximum junction temperature.



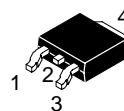
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**32 AMPERES**  
**60 VOLTS**  
 $R_{DS(on)} = 28\text{ m}\Omega$



### MARKING DIAGRAM

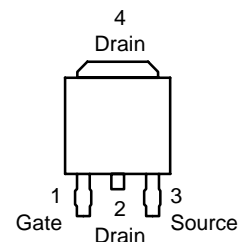


**CASE 369A**  
**DPAK**  
**STYLE 2**



NTD32N06L = Device Code  
Y = Year  
WW = Work Week  
T = MOSFET

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping
NTD32N06L	DPAK	75 Units/Rail
NTD32N06L-1	DPAK	75 Units/Rail
NTD32N06LT4	DPAK	2500 Tape & Reel

# NTD32N06L

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 1) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 –	70 62	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±15 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	–	–	±100	nAdc

### ON CHARACTERISTICS (Note 1)

Gate Threshold Voltage (Note 1) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 –	1.7 4.8	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 1) (V <sub>GS</sub> = 5 Vdc, I <sub>D</sub> = 16 Adc)	R <sub>DS(on)</sub>	–	23.7	28	mΩ
Static Drain-to-Source On-Resistance (Note 1) (V <sub>GS</sub> = 5 Vdc, I <sub>D</sub> = 20 Adc) (V <sub>GS</sub> = 5 Vdc, I <sub>D</sub> = 32 Adc) (V <sub>GS</sub> = 5 Vdc, I <sub>D</sub> = 16 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	– – –	0.48 0.78 0.61	0.67 – –	Vdc
Forward Transconductance (Note 1) (V <sub>DS</sub> = 6 Vdc, I <sub>D</sub> = 16 Adc)	g <sub>FS</sub>	–	27	–	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	–	1214	1700	pF
Output Capacitance		C <sub>oss</sub>	–	343	480	
Transfer Capacitance		C <sub>rss</sub>	–	87	180	

### SWITCHING CHARACTERISTICS (Note 2)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 32 Adc, V <sub>GS</sub> = 5 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 1)	t <sub>d(on)</sub>	–	12.8	30	ns
Rise Time		t <sub>r</sub>	–	221	450	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	37	80	
Fall Time		t <sub>f</sub>	–	128	260	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 32 Adc, V <sub>GS</sub> = 5 Vdc) (Note 1)	Q <sub>T</sub>	–	23	50	nC
		Q <sub>1</sub>	–	4.5	–	
		Q <sub>2</sub>	–	14	–	

### SOURCE-DrAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc) (Note 1) (I <sub>S</sub> = 32 Adc, V <sub>GS</sub> = 0 Vdc) (Note 1) (I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	– – –	0.89 0.95 0.74	1.0 – –	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 32 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs) (Note 1)	t <sub>rr</sub>	–	56	–	ns
		t <sub>a</sub>	–	31	–	
		t <sub>b</sub>	–	25	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.093	–	μC

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperatures.

# NTD32N06L

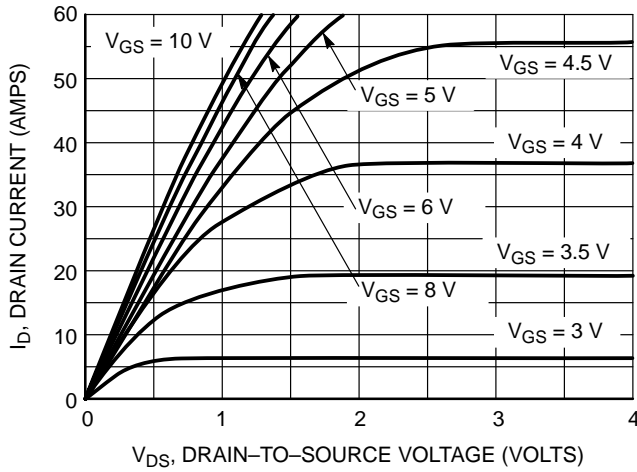


Figure 1. On-Region Characteristics

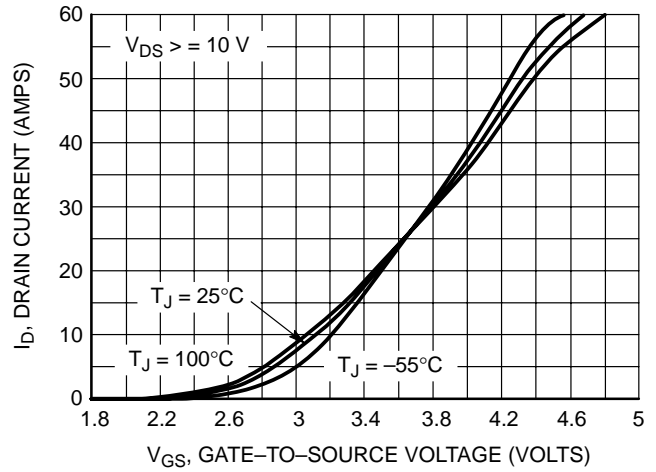


Figure 2. Transfer Characteristics

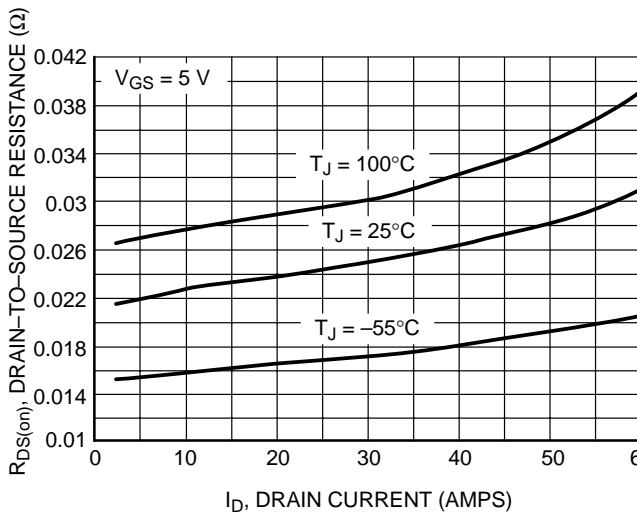


Figure 3. On-Resistance vs. Drain Current

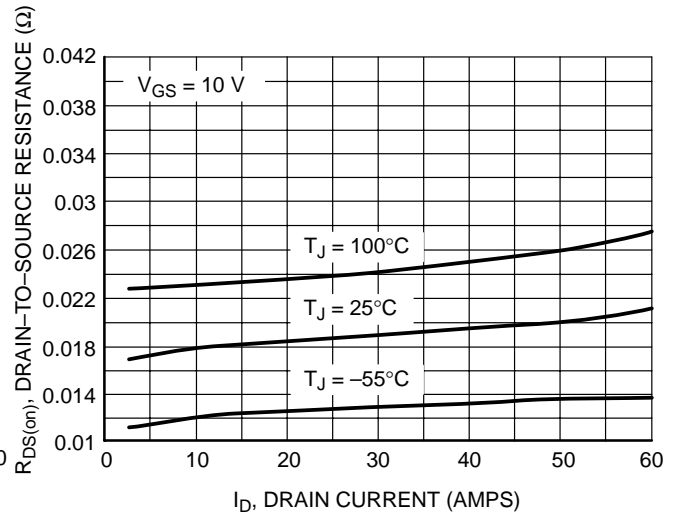


Figure 4. On-Resistance vs. Drain Current

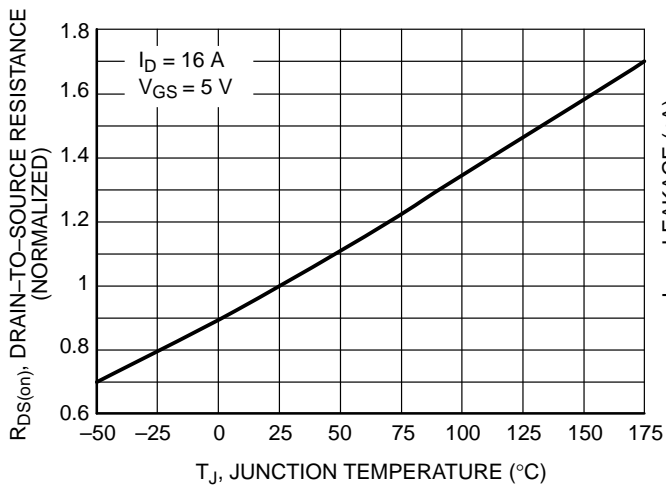


Figure 5. On-Resistance Variation with Temperature

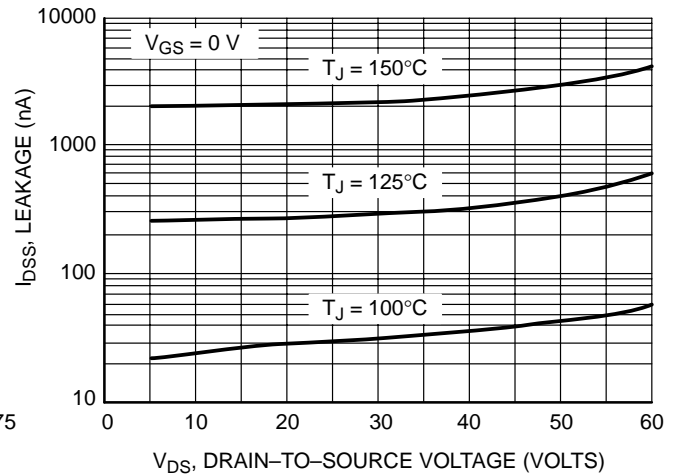


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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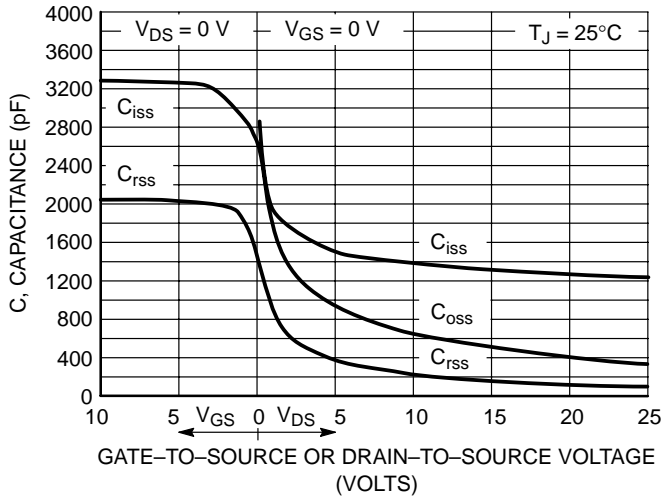


Figure 7. Capacitance Variation

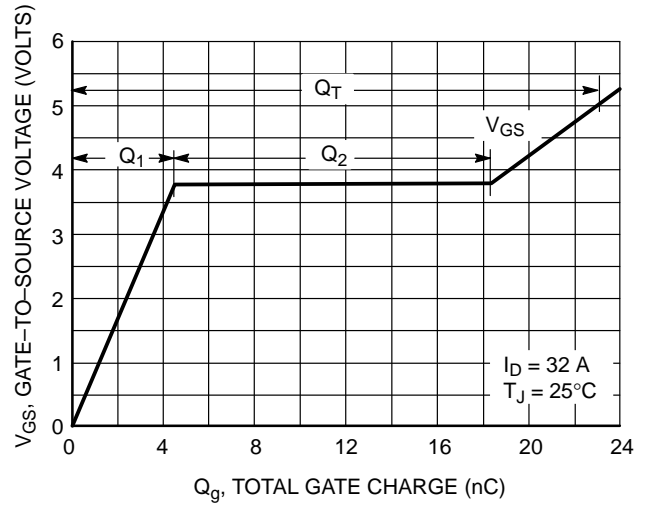


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

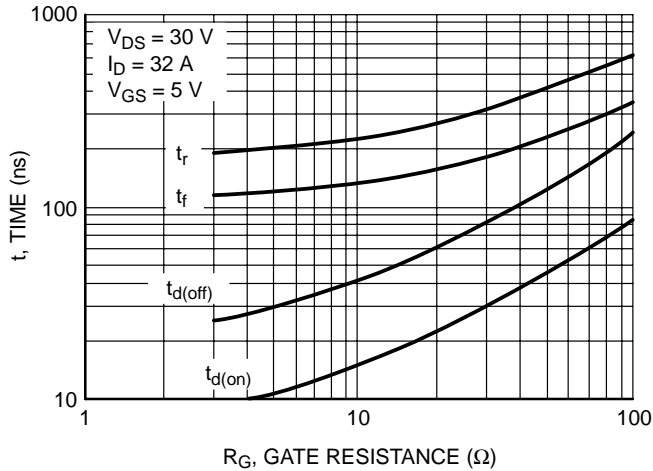


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

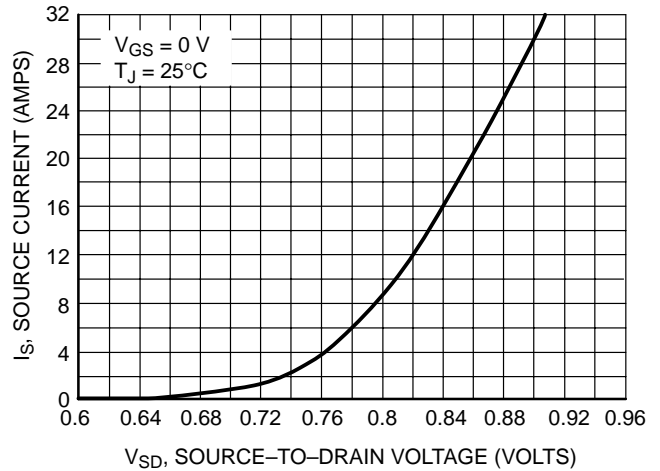


Figure 10. Diode Forward Voltage vs. Current

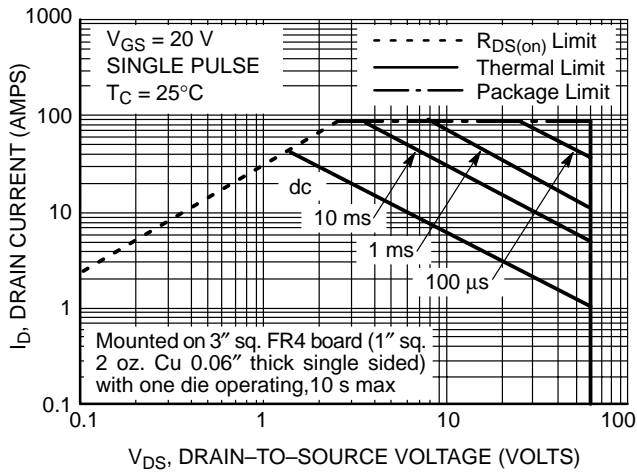


Figure 11. Maximum Rated Forward Biased Safe Operating Area

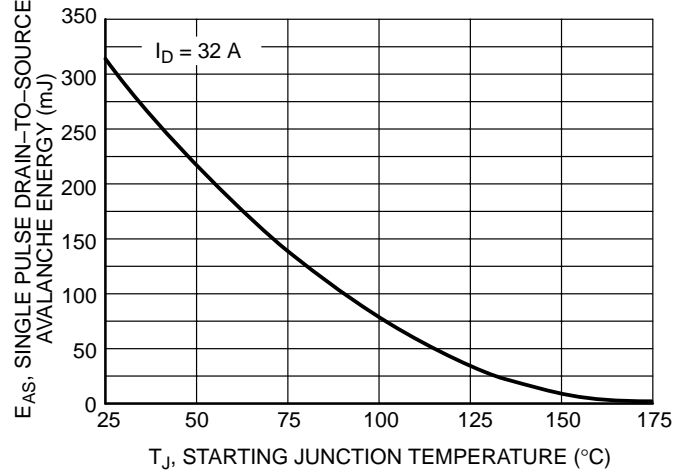


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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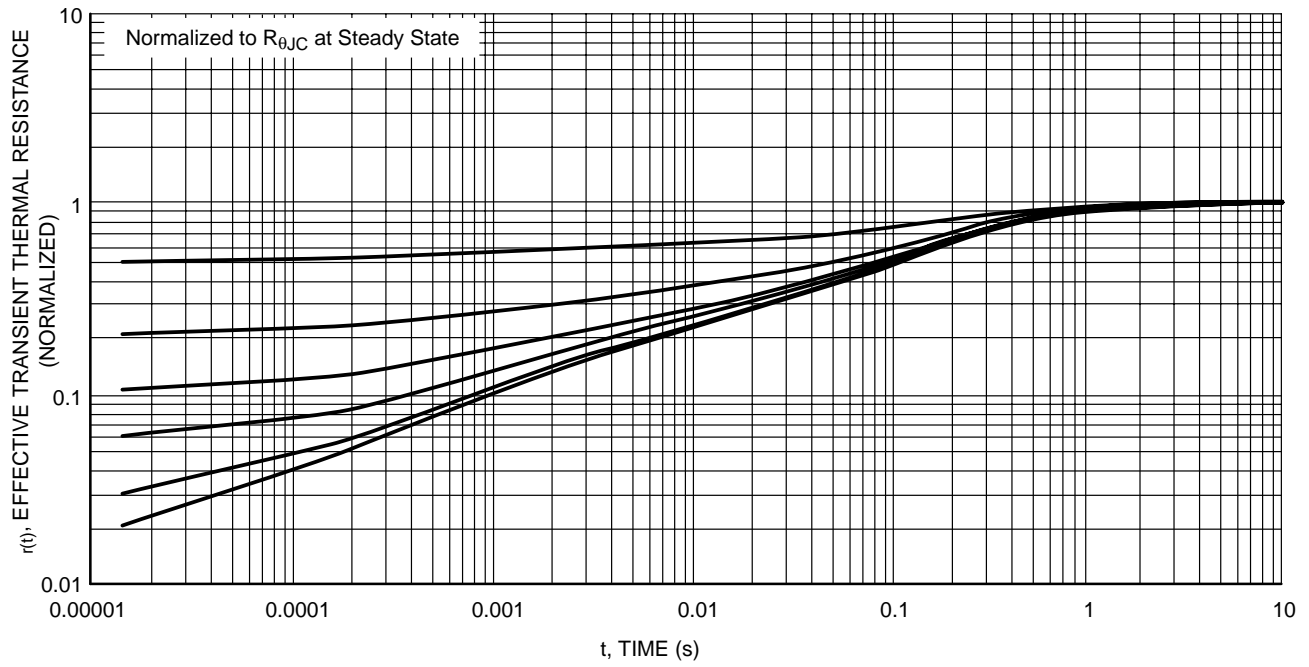


Figure 13. Thermal Response

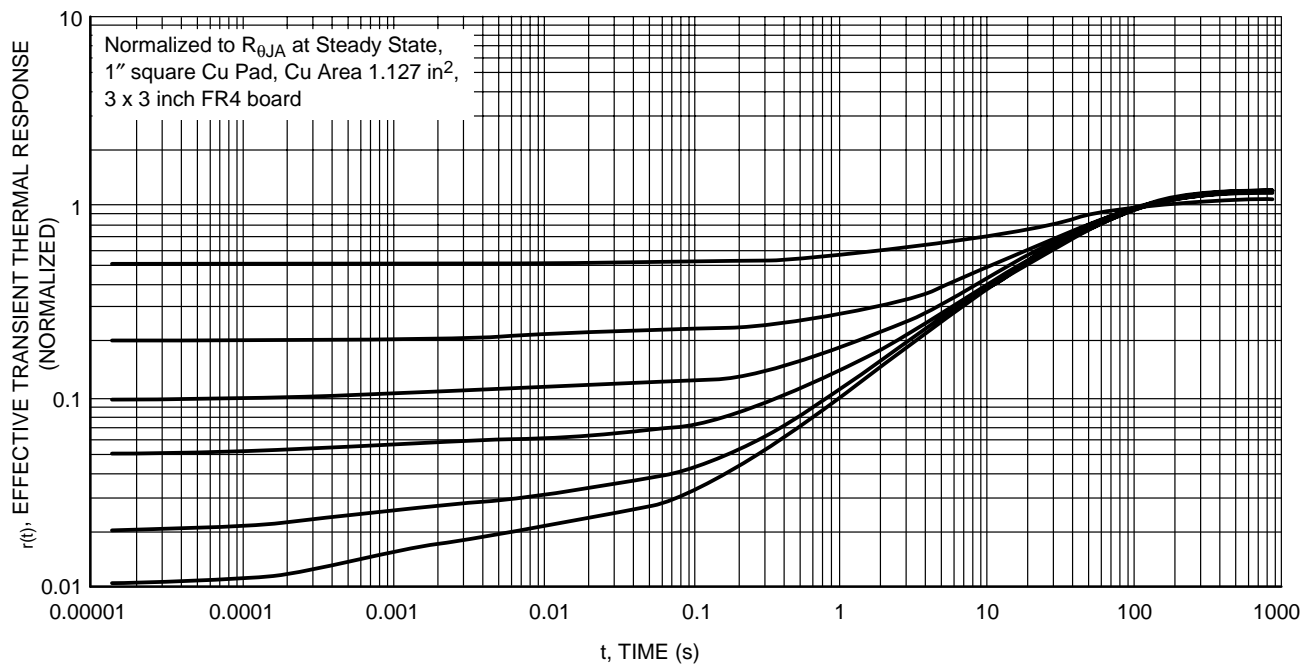
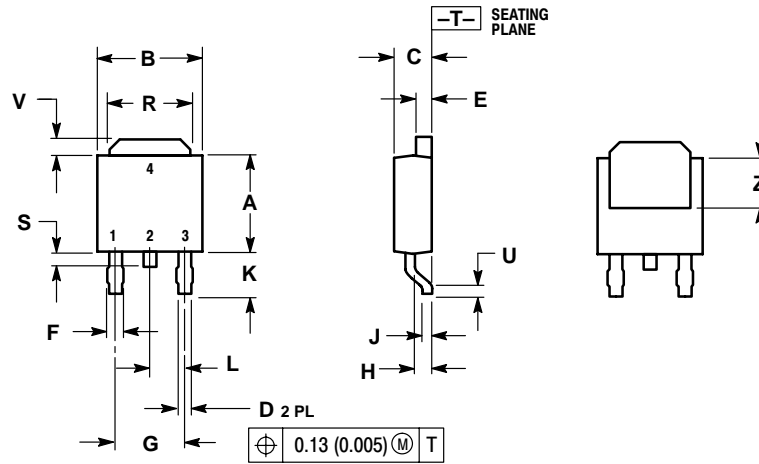


Figure 14. Thermal Response

# NTD32N06L

## PACKAGE DIMENSIONS

**DPAK**  
CASE 369A-13  
ISSUE AB




### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	----	0.51	----
V	0.030	0.050	0.77	1.27
Z	0.138	----	3.51	----

## **Notes**

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