

# Low-Voltage CMOS Octal Buffer

## With 5V-Tolerant Inputs and Outputs (3-State, Inverting)

The MC74LCX240 is a high performance, inverting octal buffer operating from a 2.3 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5V allows MC74LCX240 inputs to be safely driven from 5V devices. The MC74LCX240 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

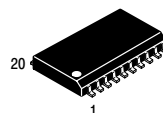
Current drive capability is 24mA at the outputs. The Output Enable ( $\overline{OE}$ ) input, when HIGH, disables the outputs by placing them in a HIGH Z condition.

- Designed for 2.3 to 3.6V  $V_{CC}$  Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 $\mu$ A)  
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

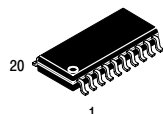
# MC74LCX240

# LCX

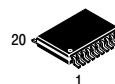
## LOW-VOLTAGE CMOS OCTAL BUFFER



**DW SUFFIX**  
PLASTIC SOIC  
CASE 751D-04



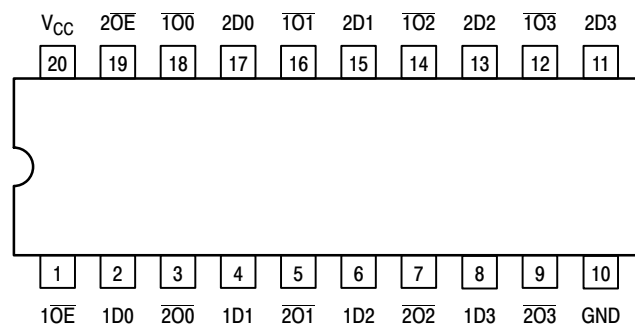
**M SUFFIX**  
PLASTIC SOIC EIAJ  
CASE 967-01



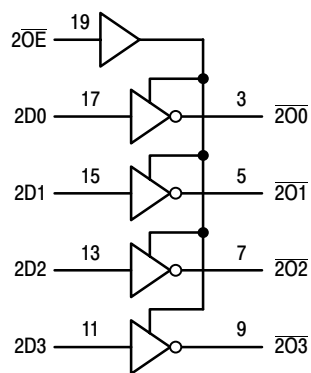
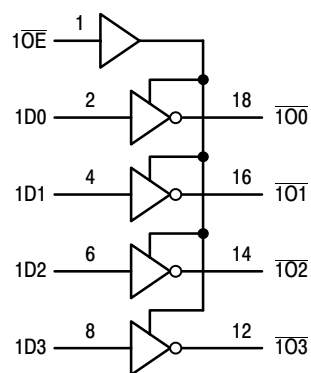
**DT SUFFIX**  
PLASTIC TSSOP  
CASE 948E-02

### PIN NAMES

Pins	Function
$\overline{nOE}$	Output Enable Inputs
1Dn, 2Dn	Data Inputs
1On, 2On	3-State Outputs



**Figure 1. Pinout: 20-Lead (Top View)**



**Figure 2. LOGIC DIAGRAM**

INPUTS		OUTPUTS
$\overline{1OE}$ 2OE	1Dn 2Dn	$\overline{1On}, \overline{2On}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for  $I_{CC}$  reasons, DO NOT FLOAT Inputs

## ABSOLUTE MAXIMUM RATINGS\*

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	−0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	−0.5 ≤ V <sub>I</sub> ≤ +7.0		V
V <sub>O</sub>	DC Output Voltage	−0.5 ≤ V <sub>O</sub> ≤ +7.0	Output in 3-State	V
		−0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	Note 1.	V
I <sub>IK</sub>	DC Input Diode Current	−50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	−50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	−65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I<sub>O</sub> absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	2.0	3.3	3.6	V
	Operating Data Retention Only	1.5	3.3	3.6	
V <sub>I</sub>	Input Voltage	0		5.5	V
V <sub>O</sub>	Output Voltage (HIGH or LOW State)	0		V <sub>CC</sub>	V
	(3-State)	0		5.5	
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			−24	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			24	mA
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			−12	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			12	mA
T <sub>A</sub>	Operating Free-Air Temperature	−40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8V to 2.0V, V <sub>CC</sub> = 3.0V	0		10	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = −40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OH</sub> = −100μA	V <sub>CC</sub> − 0.2		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = −12mA	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = −18mA	2.4		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = −24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 100μA		0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 12mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 24mA		0.55	

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

## DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
I <sub>I</sub>	Input Leakage Current	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>I</sub> ≤ 5.5V		±5.0	μA
I <sub>OZ</sub>	3-State Output Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>O</sub> ≤ 5.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>I</sub> = GND or V <sub>CC</sub>		10	μA
		2.7 ≤ V <sub>CC</sub> ≤ 3.6V; 3.6 ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V		±10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA

## AC CHARACTERISTICS (t<sub>R</sub> = t<sub>F</sub> = 2.5ns; C<sub>L</sub> = 50pF; R<sub>L</sub> = 500Ω)

Symbol	Parameter	Waveform	Limits			Unit
			T <sub>A</sub> = −40°C to +85°C			
			V <sub>CC</sub> = 3.0V to 3.6V		V <sub>CC</sub> = 2.7V	
			Min	Max	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Input to Output	1	1.5 1.5	6.5 6.5	7.5 7.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	2	1.5 1.5	8.0 8.0	9.0 9.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time From High and Low Level	2	1.5 1.5	7.0 7.0	8.0 8.0	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 3.)			1.0 1.0		ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

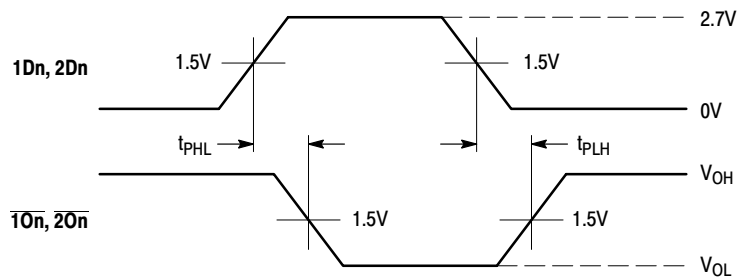
## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = +25°C			Unit
			Min	Typ	Max	
V <sub>OLP</sub>	Dynamic LOW Peak Voltage (Note 4.)	V <sub>CC</sub> = 3.3V, C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V		0.8		V
V <sub>OLV</sub>	Dynamic LOW Valley Voltage (Note 4.)	V <sub>CC</sub> = 3.3V, C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V		0.8		V

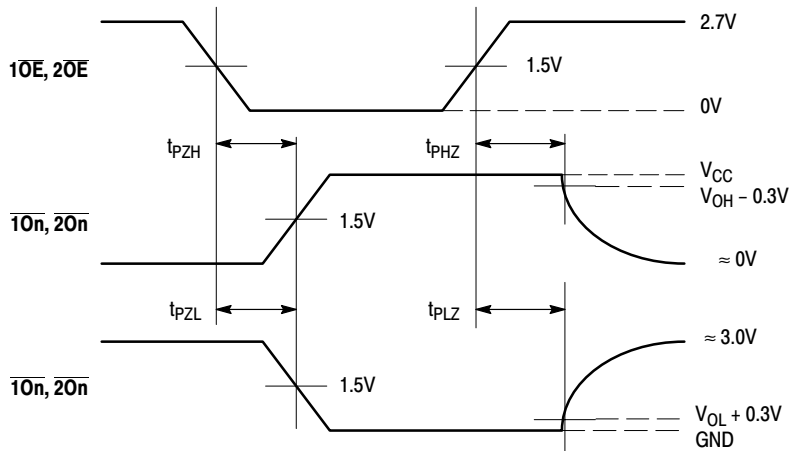
4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10MHz, V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	25	pF

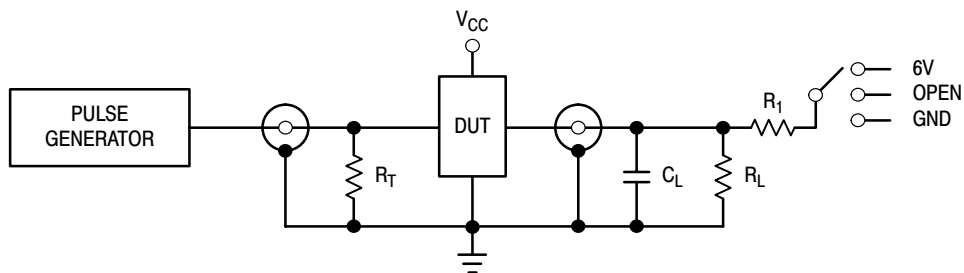


**WAVEFORM 1 - PROPAGATION DELAYS**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



**WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

**Figure 3. Waveforms**



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

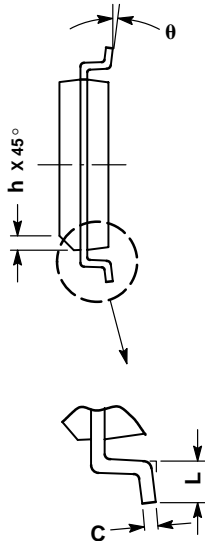
$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)

$R_L = R_1 = 500\Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 4. Test Circuit**

**DW SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751D-04  
ISSUE E



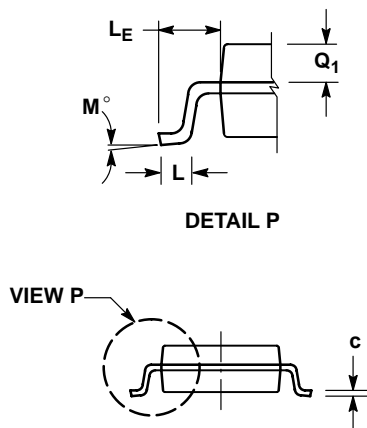
**NOTES:**

- 1. DIMENSIONS ARE IN MILLIMETERS.**
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.**
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.**
- 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.**
- 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.**

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).




	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

**DT SUFFIX**  
PLASTIC TSSOP PACKAGE  
CASE 948E-02  
ISSUE A



1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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