Advance Information

Power MOSFET

28 A, 24 V N-Channel SO-8 Leadless

The SO-8LL (Leadless) package uses the power QFN package technology. It's footprint matches that of the standard SO-8 single die device. This Leadless SO-8 package provides low parasitic inductance compared to the standard SO-8 package allowing for higher frequency operation.

Features

- Planar HD3E Process for Fast Switching Performance.
- Body Diode for Low t_{rr} and Q_{rr}, Optimized for Synchronous Operation
- Low R_{DSon} to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Optimized Q_{dg} X R_{SDon} (FOM) for Shootthrough Protection
- Low Gate Charge

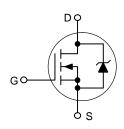
Product Summary

Symbol	Value
V _{DS}	24 V
R _{DSon} @ 10 V	3.7 mΩ
Q_g	24 nC
I _D	28 A
Q _{gd}	12 nC



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MARKING DIAGRAM





SO-8 Leadless **CASE 751S**

= Specific Device Code XXXXX

= Year WW = Work Week

PIN ASSIGNMENT

PIN	FUNCTION
1	S – SOURCE
2	G – GATE
3	D – DRAIN

ORDERING INFORMATION

Device	Package	Shipping
NTLMS4504N	SO-8 Leadless	2500 Tape & Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ Unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	24	V _{dc}
Gate-to-Source Voltage	- Continuous	V _{GS}	±20	V _{dc}
Co	ntinuous @ T_A = 25°C (Note 1) ntinuous @ T_A = 25°C (Note 2) ngle Pulse (t_p = 10 μ s) (Note 4)	I _D I _D I _{DM}	18 28 74	A A A
Maximum Power Dissipation (Steady State) @ $T_A = 25$ °C (Note 1) Single Pulse ($t_p = 10$ Secs) $T_A = 25$ °C (Note 2)		P _D	2.4 6.0	W
Operating and Storage Temperature		T _J and T _{stg}	-55 to 150	°C
Single Pulse Drain–to Source Avalanche Energy – Starting T _J = 25°C		E _{AS}	220	mJ
Thermal Resistance	Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2) Junction-to-Ambient (Note 3)	$R_{ heta JA} \ R_{ heta JA} \ R_{ heta JA}$	52 22 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 Secs		TL	260	°C

- When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in²).
 1" pad (Cu Area 0.911 in²), t < 10 sec.
 When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).
 Chip current capability limited by package.

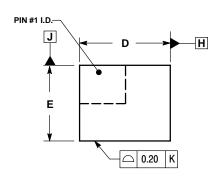
ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

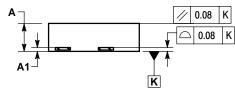
Characteristics		Symbol	Min.	Тур.	Max.	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 5 ($V_{GS} = 0 \ V_{dc}, \ I_D = 250 \ \mu A_{dc}$) Temperature Coefficient (Positive))	V(br) _{DSS}	24 -	28 25	- -	V _{dc} mV/°C
Zero Gate Voltage Drain Current $ \begin{aligned} (V_{DS} = 20 \ V_{dc}, V_{GS} = 0 \ V_{dc}) \\ (V_{DS} = 20 V_{dc}, V_{GS} = 0 \ V_{dc}, T_J = 150^{\circ}C) \end{aligned} $		I _{DSS}	_ _	_ _	0.8 10	μA _{dc}
Gate-Body Leakage Current	$(V_{GS} = \pm 20 \ V_{dc}, \ V_{DS} = 0 \ V_{dc})$	I _{GSS}	_	-	±100	nA _{dc}
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage (Note 5) $ (V_{DS} = V_{GS}, I_D = 250 \mu A_{dc}) $ Threshold Temperature Coefficient (Negative)		V _{GS} (th)	1.0	1.5 -4.0	2.0	V _{dc} mV/°C
Static Drain-to-Source On-Resistance (Note 5)		R _{DS} (on)	_ _	3.7 4.6	5 6.2	mΩ
Forward Transconductance (Note 5)	$(V_{DS} = 10 V_{dc}, I_D = 15 A_{dc})$	9FS	_	80	_	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	$(V_{DS} = 20 V_{dc}, V_{GS} = 0 V f = 1 MHz)$	C _{iss}	_	3320	3652	pF
Output Capacitance	f = 1 MHz)	C _{oss}	_	1420	1562	
Transfer Capacitance]	C _{rss}	_	135	160	
SWITCHING CHARACTERISTICS (Note 6)						
Turn-On Delay Time	$(V_{GS} = 4.5 V_{dc}, V_{DD} = 10$	t _d (on)	_	14	18	ns
Rise Time	$V_{dc} I_D = 28 A_{dc}, R_G = 2.5 \Omega$	t _r	_	85	109	
Turn-Off Delay Time]	t _d (off)	-	25	30]
Fall Time]	tf	-	15	20	
Gate Charge	$(V_{GS} = 4.5 V_{dc}, I_D = 28 A_{dc} V_{DS} = 10 V_{dc})$ (Note 5)	$Q_{T(g)}$	_	24	26.5	nC
		Q _{1(gs)}	_	5.5	_	
		Q _{2(gd)}	_	12	_	
		Q _{sw}	_	TBD	_	
		Q _{oss}	-	TBD	_	<u> </u>
SOURCE-DRAIN DIODE CHARACTERISTI	cs					
Forward On-Voltage	$(I_S = 14 A_{dc}, V_{GS} = 0 V_{dc})$ (Note 5) $(I_S = 1.5 A_{dc}, V_{GS} = 0 V_{dc}, T_J = 150^{\circ}C)$	V_{SD}				V_{dc}
			_	0.82	1.2	
			_	0.8	_	
Reverse Recovery Time	$(I_S = 14 A_{dc}, V_{GS} = 0 V_{dc}, V_{DD} = 20 V, dI_S/dt = 100 A/\mu s)$ (Note 5)	t _{rr}	-	33	46	ns
		t _a	-	18.5	_	
		t _b	-	15	-	
Reverse Recovery Stored Charge	1	Q _{RR}	_	0.020	_	μС

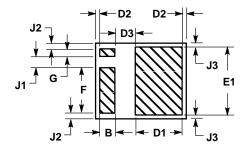
^{5.} Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperatures.

PACKAGE DIMENSIONS

SO-8 Leadless CASE 751S-02 ISSUE A







NOTES

- DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		
DIM	MIN MAX		
Α	1.750	1.950	
A1	0.254 REF		
В	0.900	1.100	
D	6.000 BSC		
D1	3.046	3.246	
D2	0.154	0.354	
D3	1.246	1.446	
Е	5.000	BSC	
E1	4.392	4.592	
F	2.940	3.140	
G	0.400	0.600	
J1	0.680	0.880	
J2	0.250	0.450	
J3	0.154	0.354	

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