

NTP15N40, NTB15N40

Preferred Device

Advance Information

Power MOSFET 15 Amps, 400 Volts N-Channel TO-220 and D2PAK

Designed for high voltage, high speed switching applications in power supplies, converters, power motor controls and bridge circuits.

Features

- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter V_{SD} Specifications
- Avalanche Energy Specified

Typical Applications

- Switch Mode Power Supplies
- PWM Motor Controls
- Converters
- Bridge Circuits

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	400	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	400	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
– Continuous	V_{GSM}	± 40	
– Non-Repetitive ($t_p \leq 10\text{ ms}$)			
Drain	I_D	15	Adc
– Continuous	I_D	12	
– Continuous @ 100°C	I_{DM}	53	
– Single Pulse ($t_p \leq 10\text{ }\mu\text{s}$)			
Total Power Dissipation	P_D	202	Watts
Derate above 25°C		1.61	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 100\text{ V}$, $V_{GS} = 10\text{ Vdc}$, $I_L = 15\text{ A}$, $L = 6\text{ mH}$, $R_G = 25\text{ }\Omega$)	E_{AS}	675	mJ
Thermal Resistance	$R_{\theta JC}$	0.62	$^\circ\text{C}/\text{W}$
– Junction-to-Case	$R_{\theta JA}$	62.5	
– Junction-to-Ambient	$R_{\theta JA}$	50	
– Junction-to-Ambient (Note 1.)			
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

1. When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



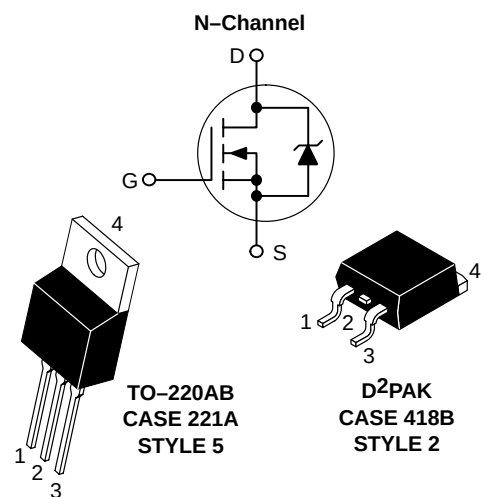
ON Semiconductor™

<http://onsemi.com>

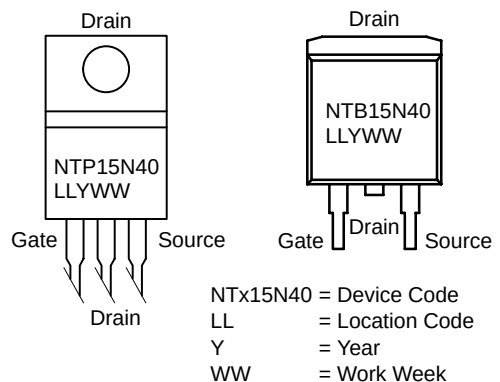
15 AMPERES

400 VOLTS

$R_{DS(on)} = 260\text{ m}\Omega$



MARKING DIAGRAMS AND PIN ASSIGNMENTS



ORDERING INFORMATION

Device	Package	Shipping
NTP15N40	TO-220AB	50 Units/Rail
NTB15N40	D2PAK	50 Units/Rail
NTB15N40T4	D2PAK	800/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

NTP15N40, NTB15N40

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 0.25\text{ mAdc}$) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	400 –	– 510	– –	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Collector Current ($V_{DS} = 400\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = 400\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	– –	– –	10 100	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0$)	$I_{GSS(f)}$ $I_{GSS(r)}$	– –	– –	100 100	nAdc

ON CHARACTERISTICS (Note 2.)

Gate Threshold Voltage $I_D = 0.25\text{ mA}$, $V_{DS} = V_{GS}$ Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 –	2.5 6.8	4.0 –	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 7.5\text{ Adc}$)	$R_{DS(on)}$	–	230	260	mOhm
Drain-to-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 15\text{ Adc}$) ($V_{GS} = 10\text{ Vdc}$, $I_D = 7.5\text{ Adc}$, $T_J = 125^\circ\text{C}$)	$V_{DS(on)}$	– –	– –	4.7 4.1	Vdc
Forward Transconductance ($V_{DS} = 15\text{ Vdc}$, $I_D = 7.5\text{ Adc}$)	g_{FS}	10	13	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{iss}	–	1800	2520	pF
Output Capacitance		C_{oss}	–	630	880	
Transfer Capacitance		C_{rss}	–	40	80	

SWITCHING CHARACTERISTICS (Note 3.)

Turn-On Delay Time	$(V_{DD} = 200\text{ Vdc}$, $I_D = 15\text{ Adc}$, $V_{GS} = 10\text{ Vdc}$, $R_G = 9.1\ \Omega$)	$t_{d(on)}$	–	13	30	ns
Rise Time		t_r	–	40	80	
Turn-Off Delay Time		$t_{d(off)}$	–	49	100	
Fall Time		t_f	–	46	90	
Gate Charge	$(V_{DS} = 320\text{ Vdc}$, $I_D = 15\text{ Adc}$, $V_{GS} = 10\text{ Vdc}$)	Q_T	–	37	50	nC
		Q_1	–	8.0	–	
		Q_2	–	12	–	
		Q_3	–	20	–	

SOURCE-DrAIN DIODE CHARACTERISTICS

Forward On-Voltage (Note 2.)	$(I_S = 15\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$) $(I_S = 15\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	V_{SD}	– –	0.90 0.80	1.0 –	Vdc
Reverse Recovery Time	$(I_S = 15\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $di_S/dt = 100\text{ A}/\mu\text{s}$)	t_{rr}	–	290	–	ns
		t_a	–	170	–	
		t_b	–	120	–	
Reverse Recovery Stored Charge		Q_{RR}	–	3.5	–	μC

INTERNAL PACKAGE INDUCTANCE

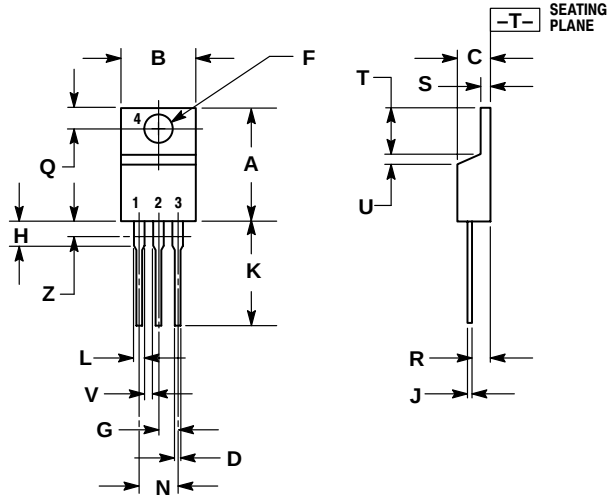
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_D	– –	3.5 4.5	– –	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L_S	–	7.5	–	

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperature.

NTP15N40, NTB15N40

PACKAGE DIMENSIONS

TO-220 THREE-LEAD TO-220AB CASE 221A-09 ISSUE AA



NOTES:

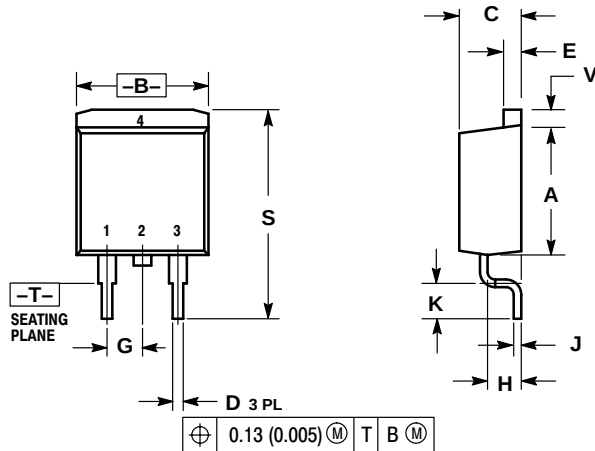
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

D²PAK CASE 418B-03 ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com
Toll-Free from Mexico: Dial 01-800-288-2872 for Access –
then Dial 866-297-9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.