## 4-Bit Magnitude Comparator

The SN74LS85 is a 4-Bit Magnitude Camparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A $_0$ -A $_3$ , B $_0$ -B $_3$ ); A $_3$ , B $_3$  being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" (OA>B), "A less than B" (OA<B), "A equal to B" (OA=B). Three Expander Inputs, IA>B, IA<B, IA=B, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: IA<B=IA>B=L, IA=B=H. For serial (ripple) expansion, the OA>B, OA<B and OA=B Outputs are connected respectively to the IA>B, IA<B, and IA=B Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- O<sub>A>B</sub>, O<sub>A<B</sub>, and O<sub>A=B</sub> Outputs Available

### **GUARANTEED OPERATING RANGES**

Symbol	Parameter	Min	Тур	Max	Unit
VCC	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
ІОН	Output Current – High			-0.4	mA
lOL	Output Current – Low			8.0	mA



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# LOW POWER SCHOTTKY



PLASTIC N SUFFIX CASE 648



SOIC D SUFFIX CASE 751B



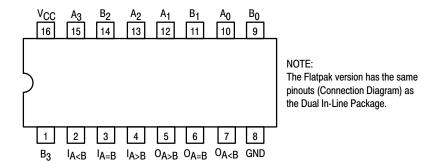
SOEIAJ M SUFFIX CASE 966

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS85N	16 Pin DIP	2000 Units/Box
SN74LS85D	SOIC-16	38 Units/Rail
SN74LS85DR2	SOIC-16	2500/Tape & Reel
SN74LS85M	SOEIAJ-16	See Note 1
SN74LS85MEL	SOEIAJ-16	See Note 1

 For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

## **CONNECTION DIAGRAM DIP (TOP VIEW)**

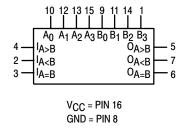


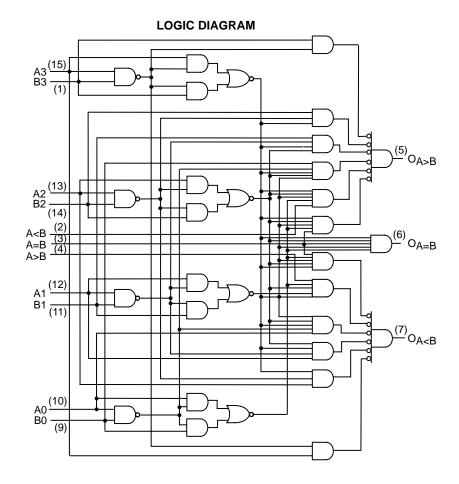
	_	LOADING	(Note a)
PIN NAMES	_	HIGH	LOW
A <sub>0</sub> - A <sub>3</sub> , B <sub>0</sub> - B <sub>3</sub>	Parallel Inputs	1.5 U.L.	0.75 U.L.
$I_A = B$	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
$I_A < B$ , $I_A > B$	A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
$O_{A > B}$	A Greater than B Output	10 U.L.	5 U.L.
$O_{A < B}$	B Greater than A Output	10 U.L.	5 U.L.
$O_A = B$	A Equal to B Output	10 U.L.	5 U.L.

#### NOTES

a) 1 TTL Unit Load (U.L.) = 40  $\mu\text{A}$  HIGH/1.6 mA LOW.

## **LOGIC SYMBOL**





## **TRUTH TABLE**

	TROTTI TABLE								
COMPARING INPUTS			_	SCADII INPUTS	_		OUTPUT	5	
A <sub>3</sub> ,B <sub>3</sub>	A <sub>2</sub> ,B <sub>2</sub>	A <sub>1</sub> ,B <sub>1</sub>	$A_0,B_0$	I <sub>A&gt;B</sub>	I <sub>A<b< sub=""></b<></sub>	I <sub>A=B</sub>	O <sub>A&gt;B</sub>	O <sub>A<b< sub=""></b<></sub>	O <sub>A=B</sub>
A3>B3	Х	Х	Χ	Х	Х	Х	Н	L	L
A3 <b3< td=""><td>Χ</td><td>Χ</td><td>Χ</td><td>Х</td><td>Χ</td><td>X</td><td>L</td><td>Н</td><td>L</td></b3<>	Χ	Χ	Χ	Х	Χ	X	L	Н	L
A3=B3	A2>B2	Χ	Χ	Х	Χ	X	Н	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> <b<sub>2</b<sub>	Χ	Χ	Х	Χ	Χ	L	Н	L
A <sub>3</sub> =B <sub>3</sub>	$A_2 = B_2$	A <sub>1</sub> >B <sub>1</sub>	Χ	Х	Χ	Χ	Н	L	L
A <sub>3</sub> =B <sub>3</sub>	$A_2=B_2$	A <sub>1</sub> <b<sub>1</b<sub>	Χ	Х	Χ	X	L	Н	L
A <sub>3</sub> =B <sub>3</sub>	$A_2=B_2$	A <sub>1</sub> =B1	$A_0 > B_0$	Х	Χ	X	Н	L	L
A3=B3	$A_2=B_2$	A <sub>1</sub> =B <sub>1</sub>	$A_0 < B_0$	Х	Χ	X	L	Н	L
A <sub>3</sub> =B <sub>3</sub>	$A_2=B_2$	A <sub>1</sub> =B <sub>1</sub>	$A_0=B_0$	Н	L	L	Н	L	L
A3=B3	$A_2=B_2$	A <sub>1</sub> =B <sub>1</sub>	$A_0=B_0$	L	Н	L	L	Н	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	$A_0 = B_0$	Х	Χ	Н	L	L	Н
A <sub>3</sub> =B <sub>3</sub>	$A_2=B_2$	A <sub>1</sub> =B <sub>1</sub>	$A_0 = B_0$	Н	Н	L	L	L	L
A <sub>3</sub> =B <sub>3</sub>	$A_2 = B_2$	A <sub>1</sub> =B <sub>1</sub>	$A_0 = B_0$	L	L	L	Н	Н	L

H = HIGH Level L = LOW Level

X = IMMATERIAL

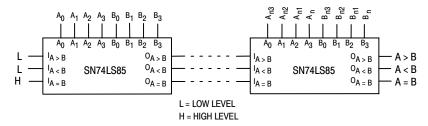


Figure 1. Comparing Two n-Bit Words

## **APPLICATIONS**

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result

when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table 1.

Table 1

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2–6
25-120 Bits	8–31

### NOTE:

The SN74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the  $A_0$ – $A_3$  and  $B_0$ – $B_3$  inputs of another SN74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

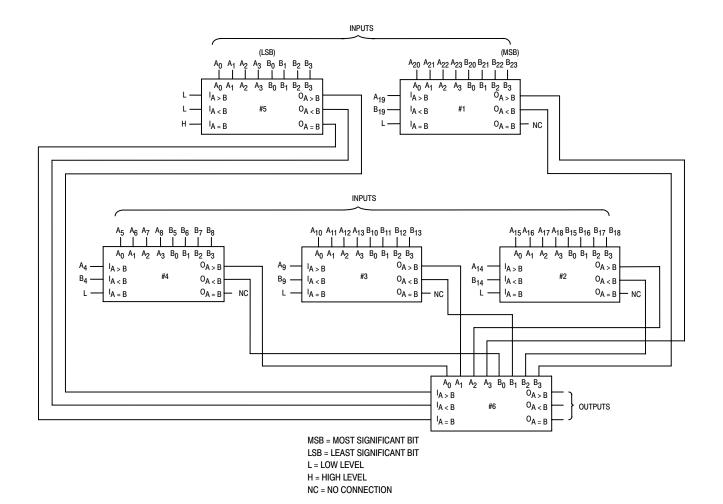


Figure 2. Comparison of Two 24-Bit Words

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

		Limits					
Symbol	Parameter	Min	Тур	Max	Unit	Tes	t Conditions
VIH	Input HIGH Voltage	2.0			V	Guaranteed Input All Inputs	HIGH Voltage for
VIL	Input LOW Voltage			0.8	V	Guaranteed Input All Inputs	LOW Voltage for
VIK	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> =	: –18 mA
VOH	Output HIGH Voltage	2.7	3.5		V	$V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table	
	0		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN,
VOL	Output LOW Voltage		0.35	0.5	V		VIN = VIL or VIH per Truth Table
I <sub>I</sub> IH	Input HIGH Current A < B, A > B Other Inputs			20 60	μΑ	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
	A < B, A > B Other Inputs			0.1 0.3	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
Ι <sub>Ι</sub> L	Input LOW Current A < B, A > B Other Inputs			-0.4 -1.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
los	Output Short Circuit Current (Note 2)	-20		-100	mA	V <sub>CC</sub> = MAX	
lcc	Power Supply Current			20	mA	V <sub>CC</sub> = MAX	

<sup>2.</sup> Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^{\circ}C$ , $V_{CC} = 5.0 \text{ V}$ )

			Limits			
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
<sup>t</sup> PLH <sup>t</sup> PHL	Any A or B to A < B, A > B		24 20	36 30	ns	
<sup>t</sup> PLH <sup>t</sup> PHL	Any A or B to A = B		27 23	45 45	ns	
<sup>t</sup> PLH <sup>t</sup> PHL	A < B or A = B to A > B		14 11	22 17	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$
tPLH tPHL	A = B to A = B		13 13	20 26	ns	
<sup>t</sup> PLH <sup>t</sup> PHL	A > B or A = B to A < B		14 11	22 17	ns	

## **AC WAVEFORMS**

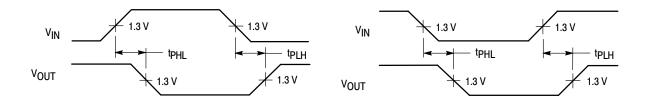
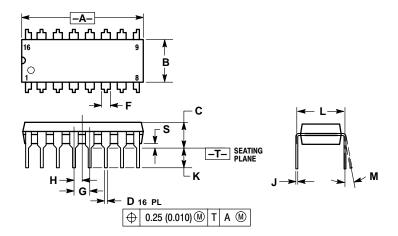


Figure 3. Figure 4.

## **PACKAGE DIMENSIONS**

## **N SUFFIX** PLASTIC PACKAGE

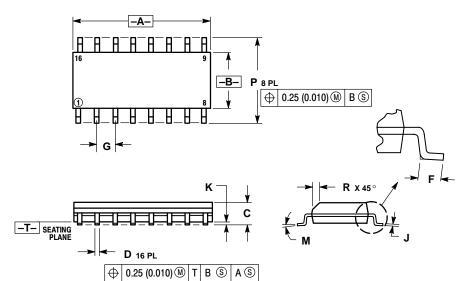
CASE 648-08 ISSUE R



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI
- DIMENSIONING AND TOLERANGING FER ANS Y14.5M, 1982. CONTROLLING DIMENSION: INCH. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS
DIM	MIN MAX		MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
Н	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10 °	0°	10 °
S	0.020	0.040	0.51	1.01

## **D SUFFIX** PLASTIC SOIC PACKAGE CASE 751B-05 **ISSUE J**



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MOLD PROTRUSION.

  MAXIMUM MOLD PROTRUSION 0.15 (0.006)
  PER SIDE.

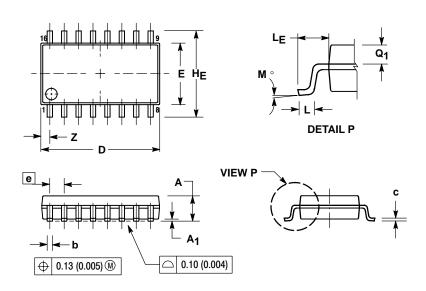
  DIMENSION D DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.127 (0.005) TOTAL
  IN EXCESS OF THE D DIMENSION AT
  MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0 °	7°	0°	7°	
P	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

## **PACKAGE DIMENSIONS**

## **M SUFFIX**

SOEIAJ PACKAGE CASE 966-01 **ISSUE O** 



### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE
- PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006)
  PER SIDE.

  4. TERMINAL NUMBERS ARE SHOWN FOR
  REFERENCE ONLY.

  5. THE LEAD WIDTH DIMENSION (b) DOES NOT
  INCLUDE DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
  TOTAL IN EXCESS OF THE LEAD WIDTH
  DIMENSION AT MAXIMUM MATERIAL CONDITION.
  DAMBAR CANNOT BE LOCATED ON THE LOWER
  RADIUS OR THE FOOT. MINIMUM SPACE
  BETWEEN PROTRUSIONS AND ADJACENT LEAD
  TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
Α <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10 °
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z		0.78		0.031

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