

# MC14569B

## Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

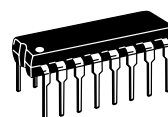
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



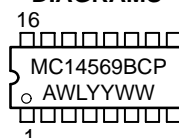
ON Semiconductor

<http://onsemi.com>

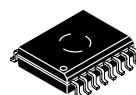
### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



TSSOP-16  
DT SUFFIX  
CASE 948F



SOIC-16  
DW SUFFIX  
CASE 751G



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

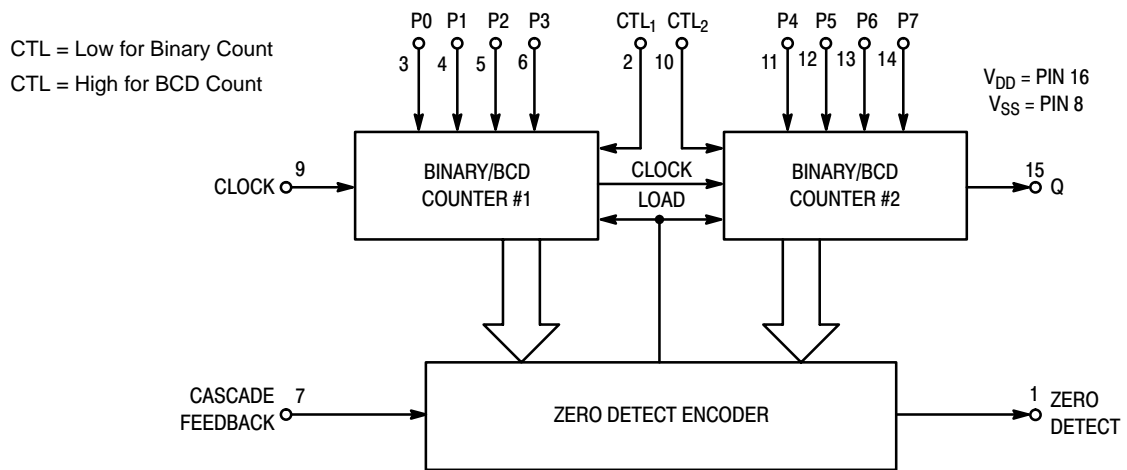
Device	Package	Shipping
MC14569BCP	PDIP-16	2000/Box
MC14569BDT	TSSOP-16	96/Rail
MC14569BDW	SOIC-16	47/Rail
MC14569BDWR2	SOIC-16	1000/Tape & Reel

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## PIN ASSIGNMENT

ZERO DETECT	1 •	16	V <sub>DD</sub>
CTL1	2	15	Q
P0	3	14	P7
P1	4	13	P6
P2	5	12	P5
P3	6	11	P4
CASCADE FEEDBACK	7	10	CTL <sub>2</sub>
V <sub>SS</sub>	8	9	CLOCK

## BLOCK DIAGRAM



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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (3.)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	“0” Level $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)  ( $V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	“0” Level $V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	“1” Level $V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)  ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	Source $I_{OH}$	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
	Sink $I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	5.0	—	0.005	5.0	—	150	$\mu$ Adc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0 10 15	$I_T = (0.58 \mu A/kHz) f + I_{DD}$ $I_T = (1.20 \mu A/kHz) f + I_{DD}$ $I_T = (1.95 \mu A/kHz) f + I_{DD}$							$\mu$ Adc

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.001$ .

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## SWITCHING CHARACTERISTICS\* (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	All Types			Unit
			Min	Typ (6.)	Max	
Output Rise Time	t <sub>TLH</sub>	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	t <sub>THL</sub>	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-On Delay Time Zero Detect Output	t <sub>PLH</sub>	5.0 10 15	— — —	420 175 125	700 300 250	ns
Q Output		5.0 10 15	— — —	675 285 200	1200 500 400	ns
Turn-Off Delay Time Zero Detect Output		5.0 10 15	— — —	380 150 100	600 300 200	ns
Q Output		5.0 10 15	— — —	530 225 155	1000 400 300	ns
Clock Pulse Width	t <sub>WH</sub>	5.0 10 15	300 150 115	100 45 30	— — —	ns
Clock Pulse Frequency		5.0 10 15	— — —	3.5 9.5 13.0	2.1 5.1 7.8	MHz
Clock Pulse Rise and Fall Time		5.0 10 15	NO LIMIT			μs

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## SWITCHING WAVEFORMS

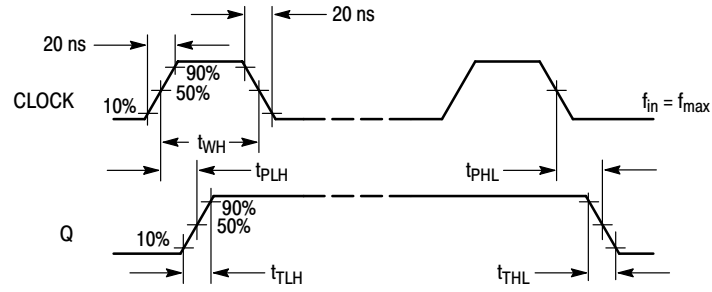


Figure 1.

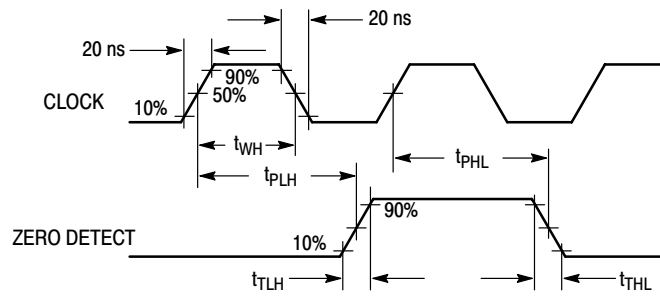


Figure 2.

## PIN DESCRIPTIONS

## INPUTS

**P0, P1, P2, P3 (Pins 3, 4, 5, 6)** — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

**P4, P5, P6, P7 (Pins 11, 12, 13, 14)** — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

**Clock (Pin 9)** — Preset data is decremented by one on each positive transition of this signal.

## OUTPUTS

**Zero Detect (Pin 1)** — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

**Q (Pin 15)** — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

## CONTROLS

**Cascade Feedback (Pin 7)** — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are “don’t cares.” Refer to Table 1 for output characteristics.

**CTL<sub>1</sub> (Pin 2)** — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

**CTL<sub>2</sub> (Pin 10)** — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

## SUPPLY PINS

**V<sub>SS</sub> (Pin 18)** — Negative Supply Voltage. This pin is usually connected to ground.

**V<sub>DD</sub> (Pin 16)** — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

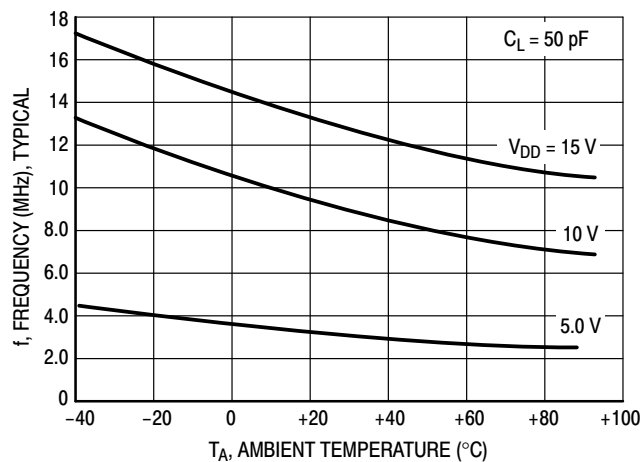
## OPERATING CHARACTERISTICS

The MC14569B is a programmable divide-by-N dual 4-bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL<sub>1</sub> and CTL<sub>2</sub>.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles,

one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to “0”, Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V<sub>DD</sub>.



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**Table 1. Mode Controls** (Cascade Feedback = Low)

Counter Control Values		Divide Ratio	
CTL <sub>1</sub>	CTL <sub>2</sub>	Zero Detect	Q
0	0	256	256
0	1	160	160
1	0	160	160
1	1	100	100

NOTE: Data Preset Inputs (P0–P7) are “Don’t Cares” while Cascade Feedback is Low.

**Table 2. Mode Controls** (CTL<sub>1</sub> = Low, CTL<sub>2</sub> = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	256	256	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	1	0	0	0	0	0	32	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	1	0	0	0	0	0	0	64	X	Q Output Active ↓
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	1	1	1	1	1	1	1	127	X	
1	0	0	0	0	0	0	0	128	128	
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1	0	0	0	1	0	0	0	136	136	
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.	.	.	.	.	.	.	.	.	.	
1	1	1	1	1	1	1	1	255	255	
2 <sup>7</sup> 128	2 <sup>6</sup> 64	2 <sup>5</sup> 32	2 <sup>4</sup> 16	2 <sup>3</sup> 8	2 <sup>2</sup> 4	2 <sup>1</sup> 2	2 <sup>0</sup> 1			Bit Value
Counter #2 Binary				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)

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**Table 3. Mode Controls** (CTL<sub>1</sub> = High, CTL<sub>2</sub> = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	1	1	0	0	1	19	X	
0	0	1	0	0	0	0	0	20	X	
.	.	.	.	.	.	.	.	.	X	
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.	.	.	.	.	.	.	.	.	X	
0	0	1	1	0	0	0	0	30	X	
.	.	.	.	.	.	.	.	.	X	
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.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	1	0	0	0	0	0	0	40	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	1	0	1	0	0	0	0	50	X	
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.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	1	1	0	0	0	0	0	60	X	
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.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	1	1	1	0	0	0	0	70	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
1	0	0	0	0	0	0	0	80	80	
.	.	.	.	.	.	.	.	.	.	Q Output Active ↓
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1	0	0	1	0	0	0	0	90	90	
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1	1	1	1	0	0	0	0	150	150	
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.	.	.	.	.	.	.	.	.	.	
1	1	1	1	1	0	0	1	159	159	
80	40	20	10	8	4	2	1			Bit Value
Counter #2 Binary				Counter #1 BCD						Counting Sequence

X = No Output (Always Low)



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**Table 4. Mode Controls** (CTL<sub>1</sub> = Low, CTL<sub>2</sub> = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	1	1	0	0	0	0	48	X	
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0	1	0	0	0	0	0	0	64	X	
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0	1	0	1	0	0	0	0	80	X	
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0	1	1	1	0	0	0	0	112	X	
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1	0	0	0	0	0	0	0	128	128	Q Output Active ↓
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1	0	0	1	0	0	0	0	144	144	
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.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	0	0	1	1	1	1	1	159	159	
2 <sup>7</sup> 128	2 <sup>6</sup> 64	2 <sup>5</sup> 32	2 <sup>4</sup> 16	2 <sup>3</sup> 8	2 <sup>2</sup> 4	2 <sup>1</sup> 2	2 <sup>0</sup> 1			Bit Value
Counter #2 BCD				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)

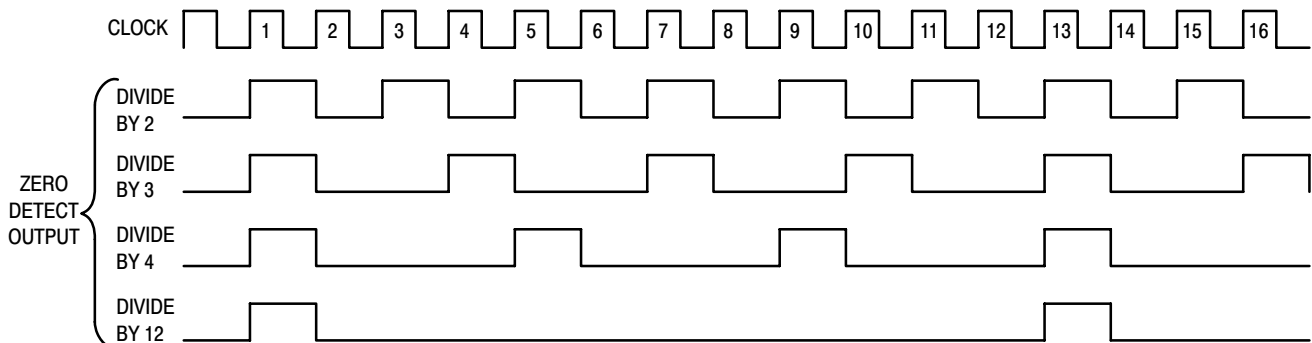
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**Table 5. Mode Controls** (CTL<sub>1</sub> = High, CTL<sub>2</sub> = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	100	100	Max Count illegal state Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
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0	0	1	1	0	0	0	0	30	X	
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0	1	0	0	0	0	0	0	40	X	
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.	.	.	.	.	.	.	.	.	X	
0	1	0	1	0	0	0	0	50	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	1	1	1	0	0	0	0	70	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
1	0	0	0	0	0	0	0	80	80	
.	.	.	.	.	.	.	.	.	.	Q Output Active ↓
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	0	0	1	0	0	0	0	90	90	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	0	0	1	1	0	0	1	99	99	
80	40	20	10	8	4	2	1			Bit Value
Counter #2 BCD				Counter #1 BCD						Counting Sequence

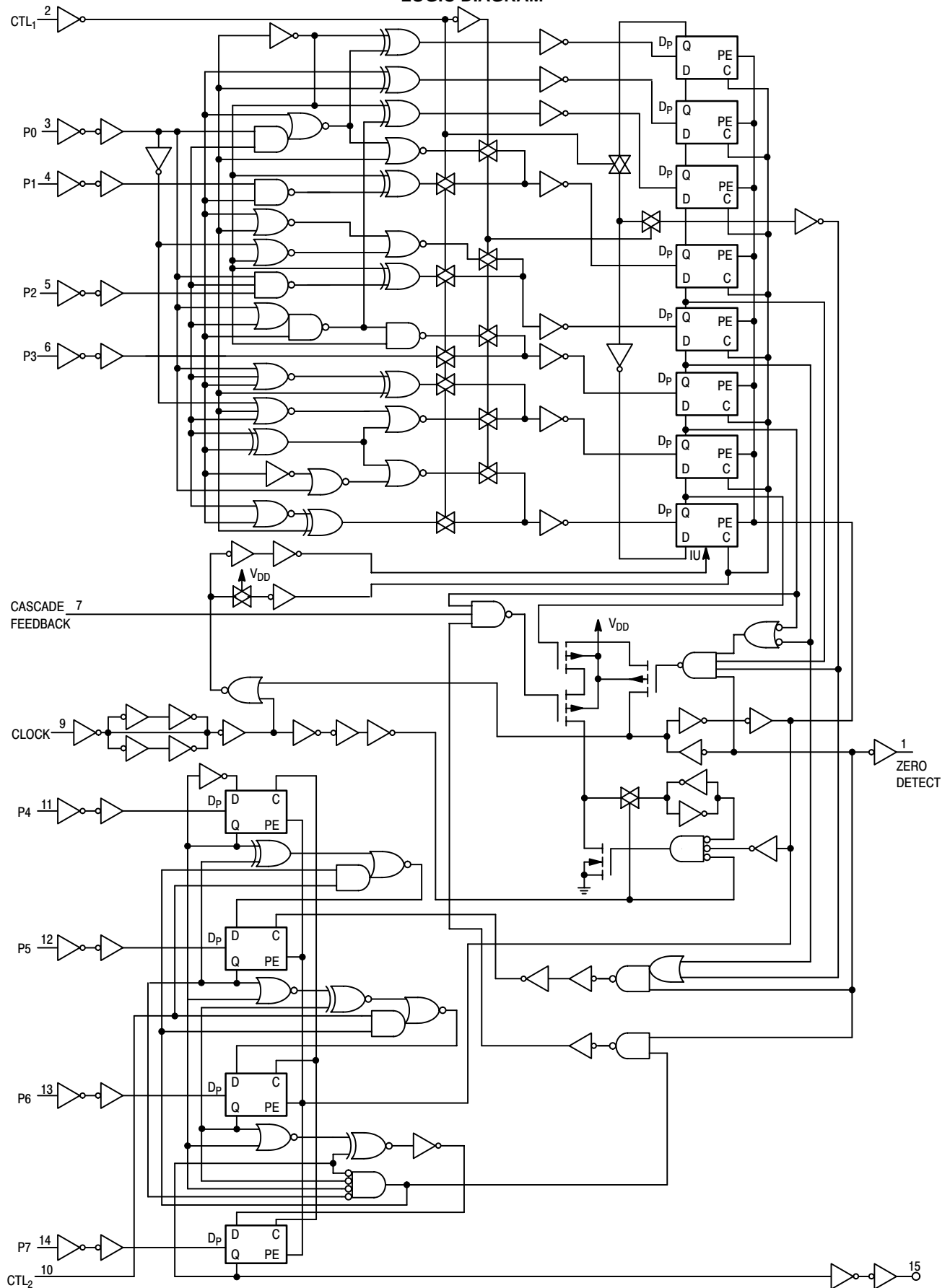
X = No Output (Always Low)

## TIMING DIAGRAM MC14569B



# MC14569B

## LOGIC DIAGRAM



# MC14569B

## TYPICAL APPLICATIONS

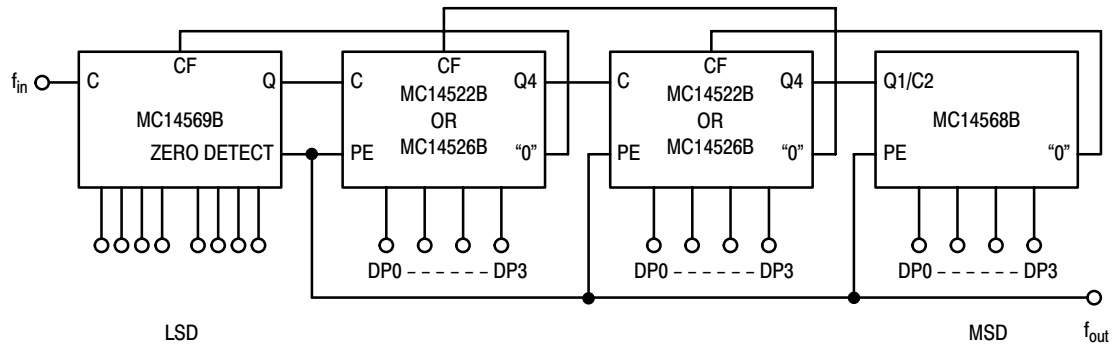
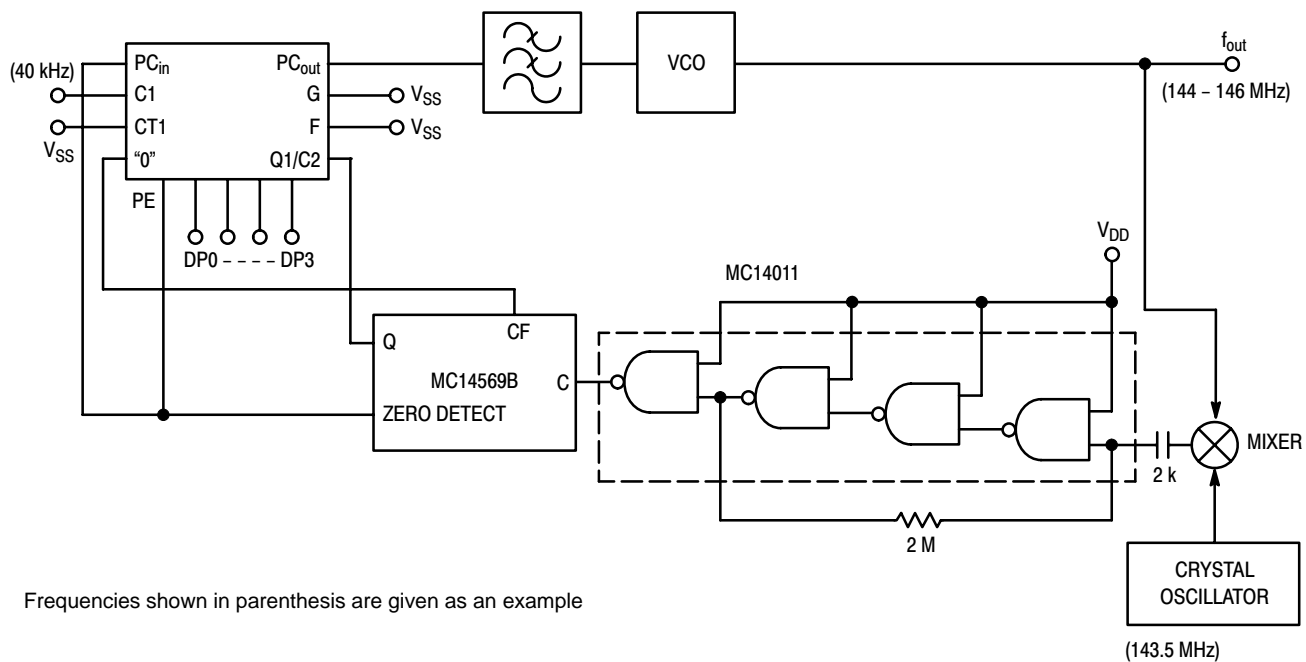


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B



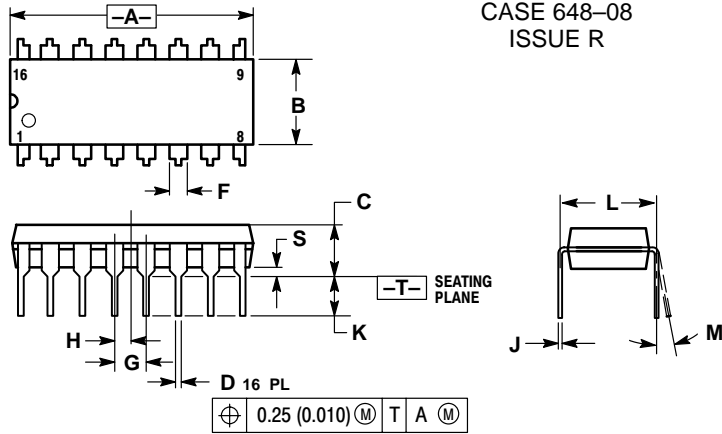
Frequencies shown in parenthesis are given as an example

Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

# MC14569B

## PACKAGE DIMENSIONS

PDIP-16  
P SUFFIX  
PLASTIC DIP PACKAGE  
CASE 648-08  
ISSUE R



### NOTES:

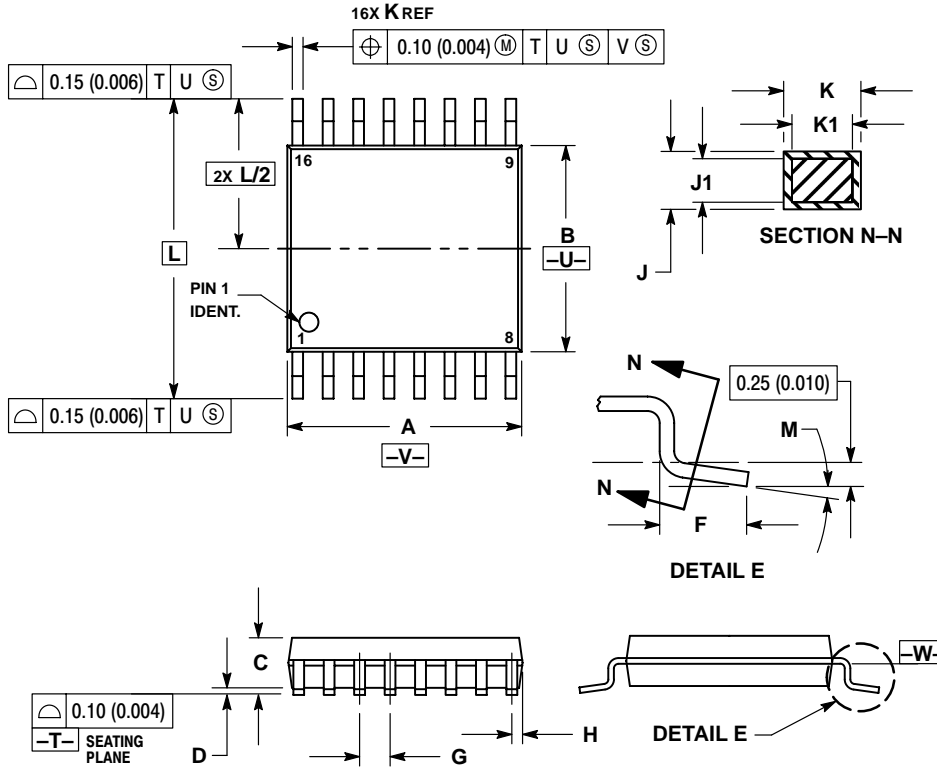
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

# MC14569B

## PACKAGE DIMENSIONS

**TSSOP-16**  
**DT SUFFIX**  
 PLASTIC TSSOP PACKAGE  
 CASE 948F-01  
 ISSUE O



### NOTES:

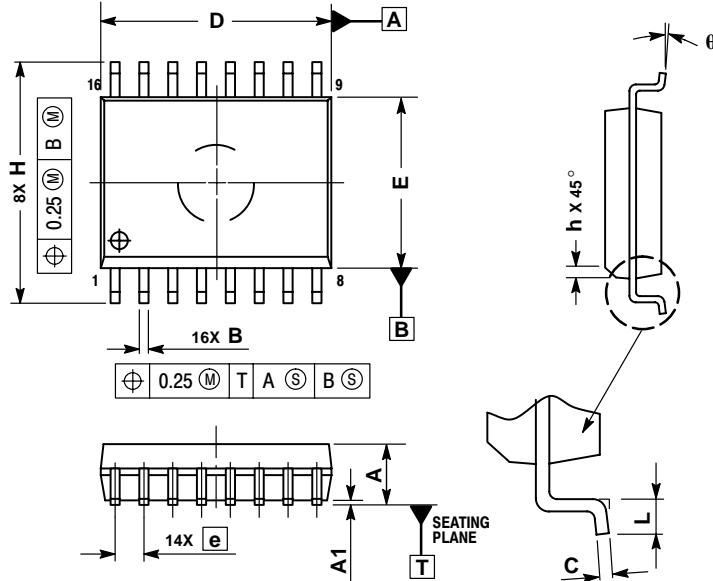
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

# MC14569B

## PACKAGE DIMENSIONS

SOIC-16  
DW SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751G-03  
ISSUE B



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27	BSC
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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