NTD60N02R

Power MOSFET
60 Amps, 24 Volts

N-Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	24	Vdc
Gate-to-Source Voltage - Continuous	V_{GS}	±20	Vdc
Thermal Resistance - Junction-to-Case Total Power Dissipation @ T_A = 25°C Drain Current Continuous @ T_A = 25°C, Chip Continuous @ T_A = 25°C, Limited by Package Continuous @ T_A = 25°C, Limited by Wires	$R_{\theta JC}$ P_D I_D I_D I_D	2.6 48 60 50 32	°C/W W A A A
Thermal Resistance Junction-to-Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current - Continuous @ T_A = 25°C	 $R_{\theta JA}$ P_D I_D	 80 1.56 9.3	 C/W W A
Thermal Resistance Junction-to-Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current - Continuous @ T_A = 25°C	 $R_{\theta JA}$ P_D I_D	 120 1.04 7.6	 °C/W W A
Operating and Storage Temperature	T_J, and T_{stg}	- 55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy - Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10.0 Vdc, I_L = 11 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	60	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in^2).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in^2).

ON Semiconductor®

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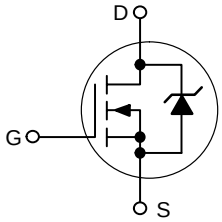
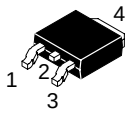
60 AMPERES
24 VOLTS
$R_{DS(on)}$ = 8.0 mΩ (Typ.)

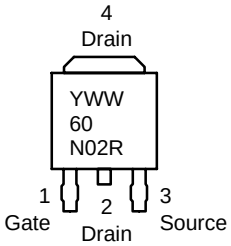
N-Channel





CASE 369A
DPAK
(Bend Lead)
STYLE 2

MARKING DIAGRAM
& PIN ASSIGNMENTS



Y = Year
WW = Work Week
60N02R = Device Code

ORDERING INFORMATION

Device	Package	Shipping
NTD60N02R	DPAK	75 Units/Rail
NTD60N02RT4	DPAK	2500 Tape & Reel
NTD60N02R1	DPAK	75 Units/Rail

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 24 -	 27.5 25.5	 - -	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 - -	 - -	 1.5 10	μAdc
Gate-Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	-	-	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 -	 1.5 4.1	 2.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V_{GS} = 4.5 Vdc, I_D = 15 Adc) (V_{GS} = 10 Vdc, I_D = 20 Adc) (V_{GS} = 10 Vdc, I_D = 30 Adc)		$R_{DS(on)}$	 - - -	 11.2 8.0 8.2	 12.5 10.5 -	mΩ
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 15 Adc) (Note 3)		g_{FS}	-	27	-	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	-	948	1330	pF
Output Capacitance		C_{oss}	-	456	640	
Transfer Capacitance		C_{rss}	-	160	225	
SWITCHING CHARACTERISTICS (Note 4)						
Turn-On Delay Time	(V_{GS} = 10.0 Vdc, V_{DD} = 10 Vdc, I_D = 30 Adc, R_G = 3.0 Ω)	$t_{d(on)}$	-	7.0	-	ns
Rise Time		t_r	-	53	-	
Turn-Off Delay Time		$t_{d(off)}$	-	14	-	
Fall Time		t_f	-	10	-	
Gate Charge	(V_{GS} = 4.5 Vdc, I_D = 30 Adc, V_{DS} = 10 Vdc) (Note 3)	Q_T	-	8.4	-	nC
		Q1	-	3.7	-	
		Q2	-	4.04	-	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	(I_S = 20 Adc, V_{GS} = 0 Vdc) (Note 3) (I_S = 30 Adc, V_{GS} = 0 Vdc) (I_S = 15 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 - - -	 0.88 1.10 0.80	 1.2 - -	Vdc
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	-	15.5	-	ns
		t_a	-	12.6	-	
		t_b	-	2.6	-	
Reverse Recovery Stored Charge		Q_{rr}	-	0.005	-	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

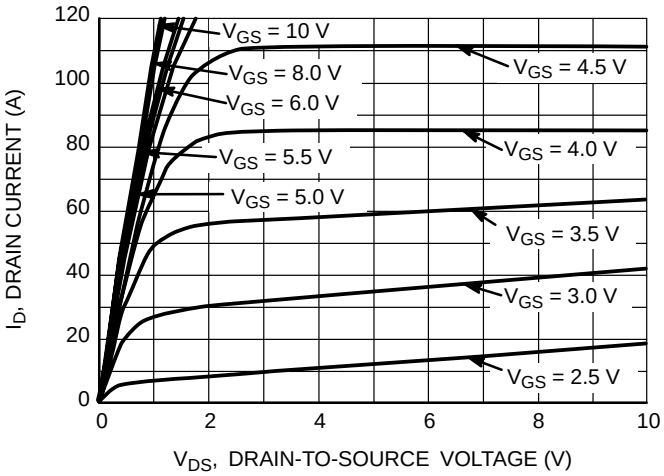


Figure 1. On-Region Characteristics

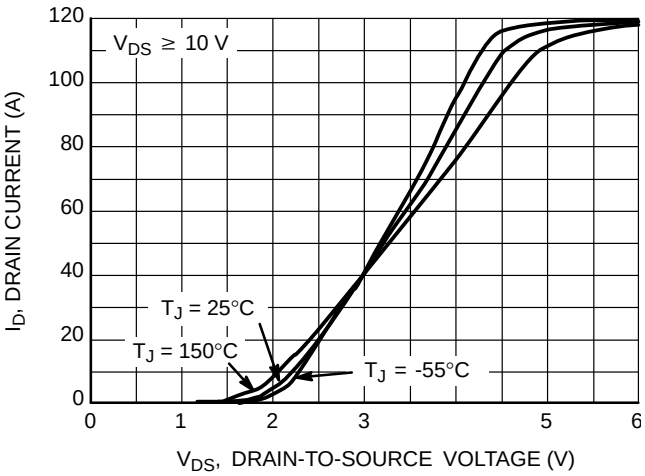


Figure 2. Transfer Characteristics

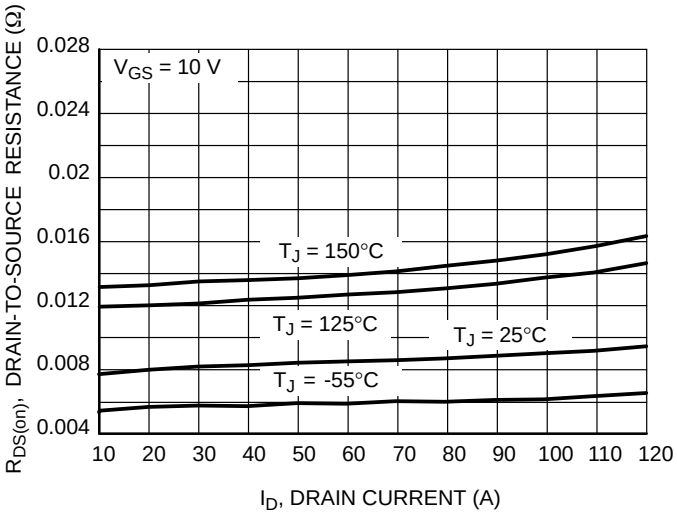


Figure 3. On-Resistance versus Drain Current and Temperature

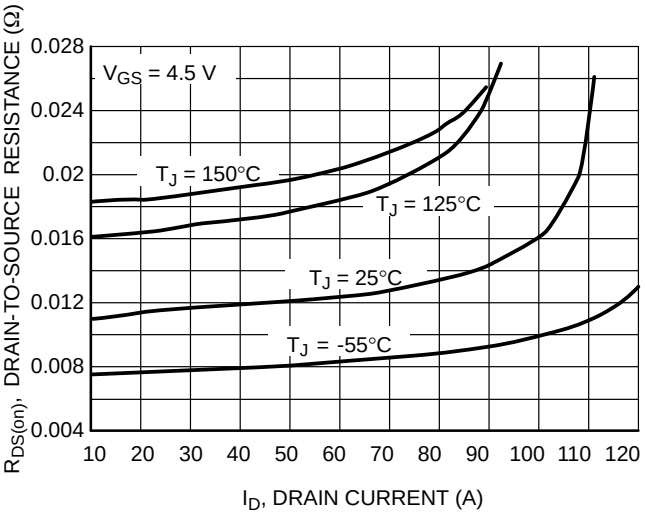


Figure 4. On-Resistance versus Drain Current and Temperature

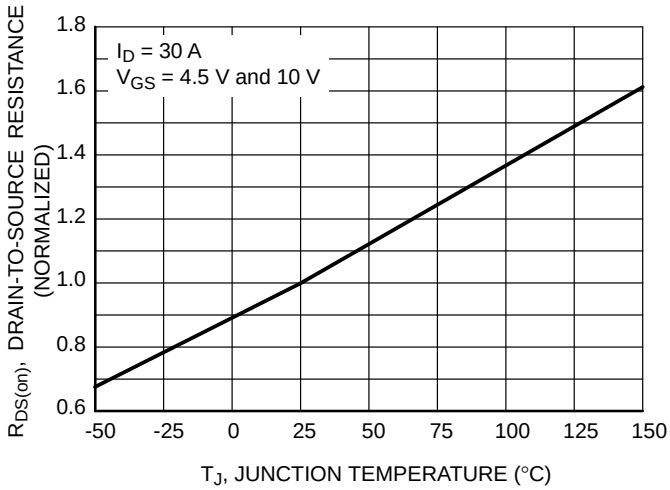


Figure 5. On-Resistance Variation with Temperature

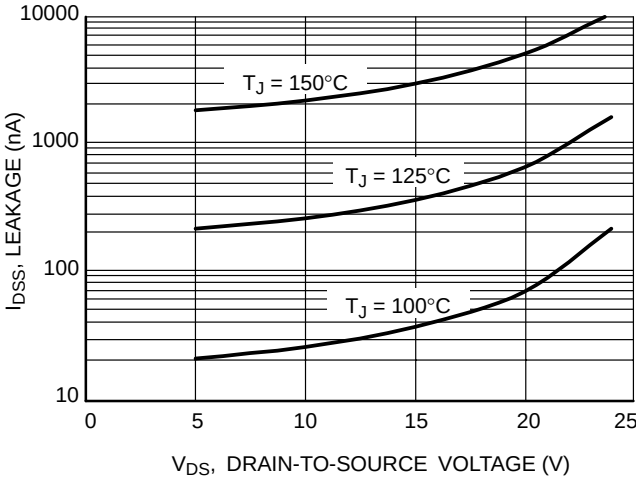


Figure 6. Drain-to-Source Leakage Current versus Voltage

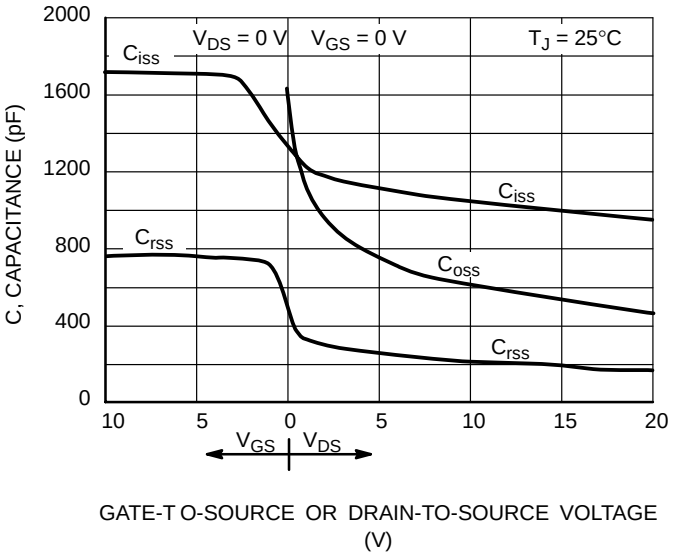


Figure 7. Capacitance Variation

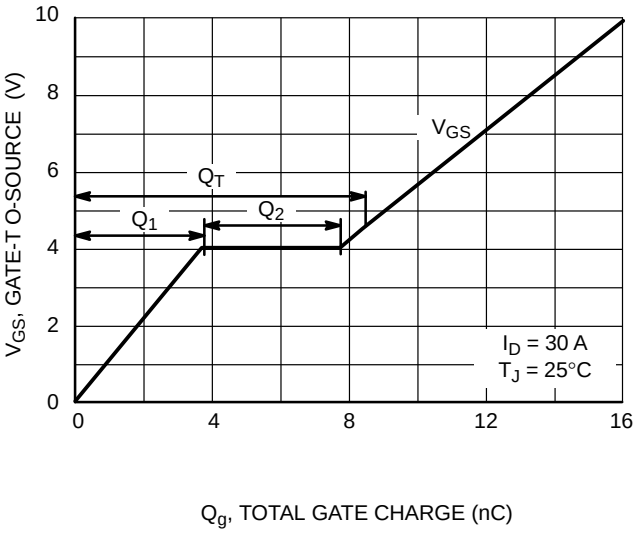


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

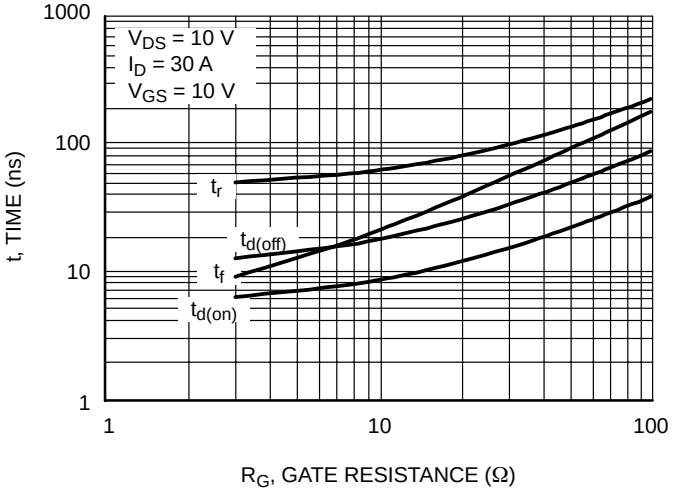


Figure 9. Resistive Switching Time Variation versus Gate Resistance

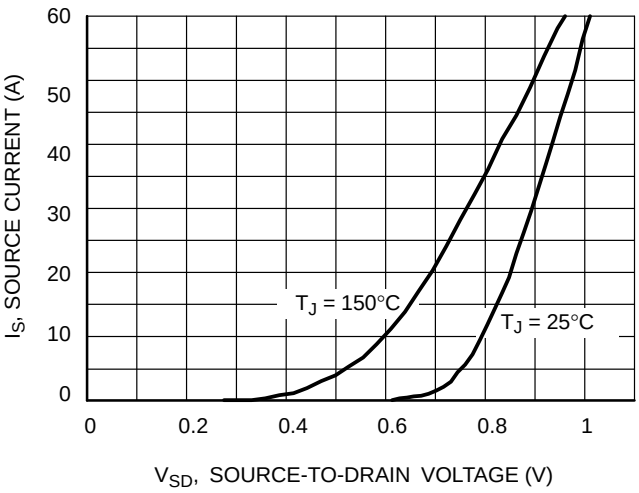


Figure 10. Diode Forward Voltage versus Current

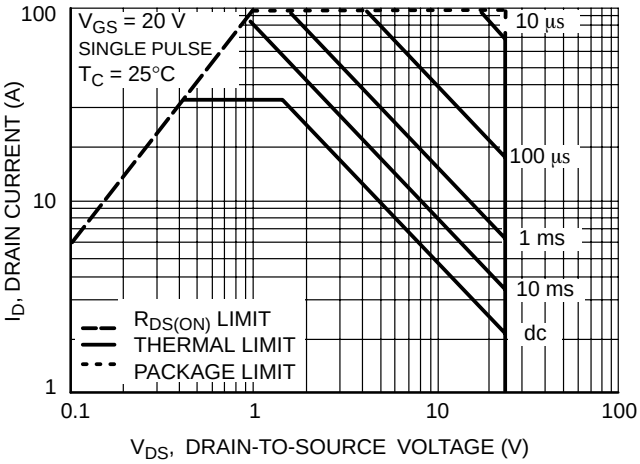


Figure 11. Maximum Rated Forward Biased Safe Operating Area

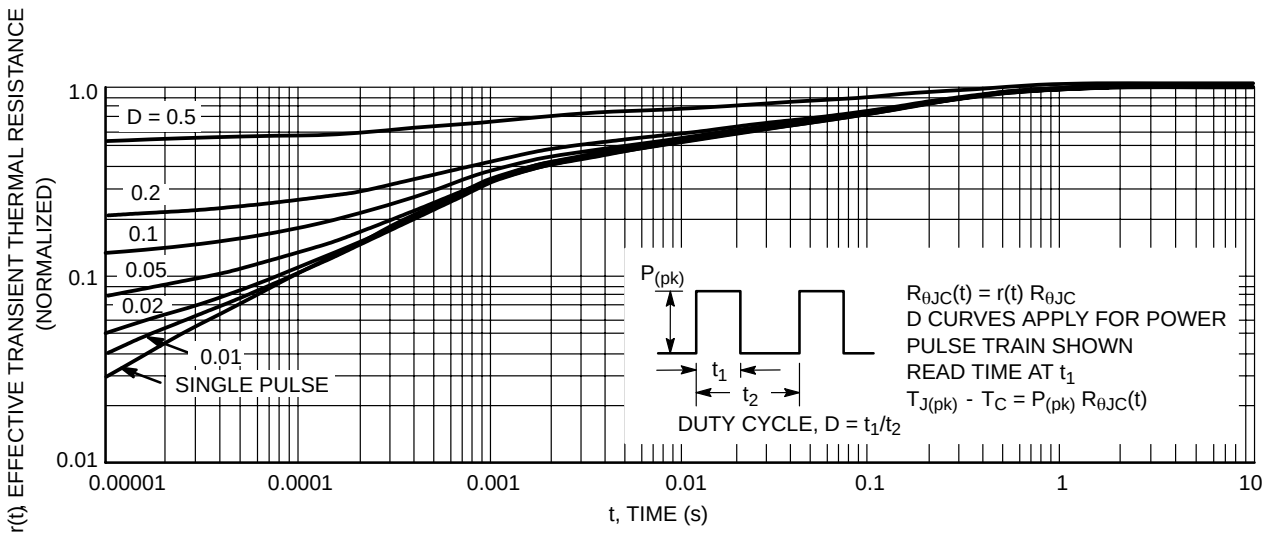
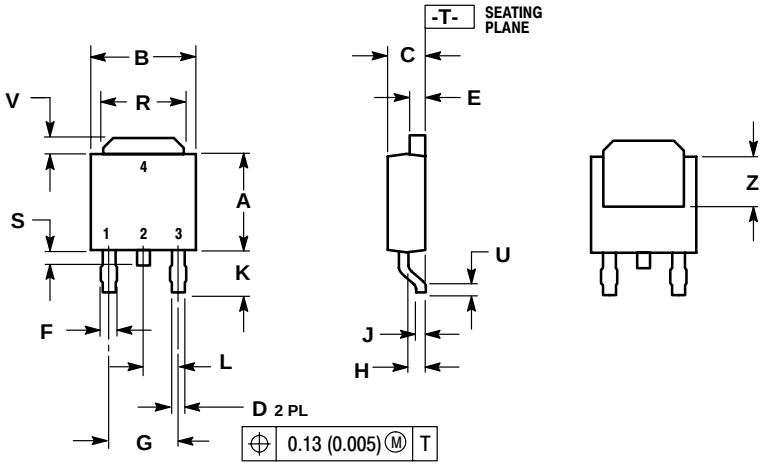


Figure 12. Thermal Response

PACKAGE DIMENSIONS

DPAK
CASE 369A-13
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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