MC14557B

1-to-64 Bit Variable Length Shift Register

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers.

- 1–64 Bit Programmable Length
- Q and $\overline{Q}$ Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or one Low–power Schottky TTL Load Over the Rated Temperature Range

ON Semiconductor

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MARKING DIAGRAMS

PDIP–16
P SUFFIX
CASE 648

16
MC14557BCP
AWLYYWW
1

SOIC–16
DW SUFFIX
CASE 751G

16
14557B
AWLYYWW
1

SOEIAJ–16
F SUFFIX
CASE 966

16
MC14557B
ALYW
1
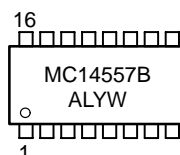
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
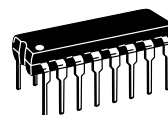
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
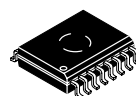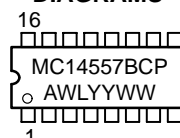
ORDERING INFORMATION
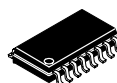
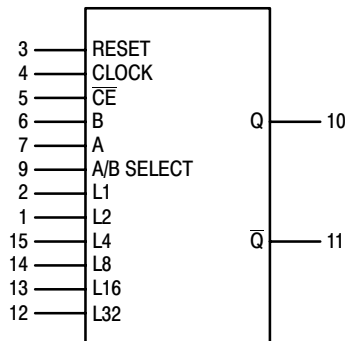| Device	Package	Shipping
MC14557BCP	PDIP–16	2000/Box
MC14557BDW	SOIC–16	47/Rail
MC14557BDWR2	SOIC–16	1000/Tape & Reel
MC14557BF	SOEIAJ–16	See Note 1.
MC14557BFEL	SOEIAJ–16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC14557B

PIN ASSIGNMENT

L2	1 ●		16	V_{DD}
L1	2		15	L4
RESET	3		14	L8
CLOCK	4		13	L16
$\overline{CE}$	5		12	L32
B	6		11	$\overline{Q}$
A	7		10	Q
V_{SS}	8		9	A/B SEL

BLOCK DIAGRAM

```
3 ——— RESET
4 ——— CLOCK
5 ——— CE
6 ——— B          Q ——— 10
7 ——— A
9 ——— A/B SELECT
2 ——— L1
1 ——— L2
15 —— L4
14 —— L8         Q ——— 11
13 —— L16
12 —— L32
```
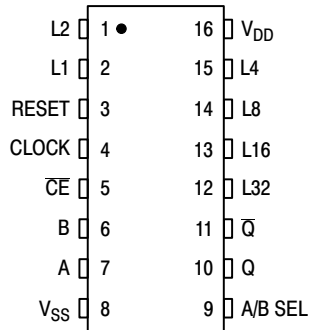
V_{DD} = PIN 16
V_{SS} = PIN 8

TRUTH TABLE

Inputs				Output
Rst	A/B	Clock	$\overline{CE}$	Q
0	0	⟋	0	B
0	1	⟋	0	A
0	0	1	⟍	B
0	1	1	⟍	A
1	X	X	X	0

Q is the output of the first selected shift
register stage.

X = Don't Care

LENGTH SELECT TRUTH TABLE

L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1 Bit
0	0	0	0	0	1	2 Bits
0	0	0	0	1	0	3 Bits
0	0	0	0	1	1	4 Bits
0	0	0	1	0	0	5 Bits
0	0	0	1	0	1	6 Bits
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	0	0	0	0	0	33 Bits
1	0	0	0	0	1	34 Bits
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	1	1	1	0	0	61 Bits
1	1	1	1	1	1	62 Bits
1	1	1	1	1	0	63 Bits
1	1	1	1	0	1	64 Bits

NOTE: Length equals the sum of the binary length control
subscripts plus one.

MC14557B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ [4.]	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	− 3.0 − 0.64 − 1.6 − 4.2	— — — —	− 2.4 − 0.51 − 1.3 − 3.4	− 4.2 − 0.88 − 2.25 − 8.8	— — — —	− 1.7 − 0.36 − 0.9 − 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.010 0.020 0.030	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current [5.] [6.] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15				I_T = (1.75 µA/kHz) f + I_{DD} I_T = (3.50 µA/kHz) f + I_{DD} I_T = (5.25 µA/kHz) f + I_{DD}				µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ [8.]	Max	Unit
Rise and Fall Time, Q or $\overline{Q}$ Output t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay, Clock or $\overline{CE}$ to Q or $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns	t_{PLH}, t_{PHL}	5 10 15	— — —	300 130 90	600 260 180	ns
Propagation Delay, Reset to Q or $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 70 ns	t_{PLH}, t_{PHL}	5 10 15	— — —	300 130 95	600 260 190	ns
Pulse Width, Clock	$t_{WH(cl)}$	5 10 15	200 100 75	95 45 35	— — —	ns
Pulse Width, Reset	$t_{WH(rst)}$	5 10 15	300 140 100	150 70 50	— — —	ns
Clock Frequency (50% Duty Cycle)	f_{cl}	5 10 15	— — —	3.0 7.5 13.0	1.7 5.0 6.7	MHz

Setup Time, A or B to Clock or $\overline{CE}$
   Worst case condition: L1 = L2 = L4 = L8 =
   L16 = L32 = V_{SS} (Register Length = 1)
	t_{su}	5
		 10
		 15
			700
			 290
			 145
				350
				 130
				 85
					—
					 —
					 —
						ns

Best case condition: L32 = V_{DD}, L1 through L16 = Don't Care (Any register length from 33 to 64)		5 10 15	400 165 60	45 5 0	— — —	

Hold Time, Clock or $\overline{CE}$ to A or B
   Best case condition: L1 = L2 = L4 = L8 = L16 =
   L32 = V_{SS} (Register Length = 1)
	t_h	5
		 10
		 15
			200
			 100
			 10
				− 150
				 − 60
				 − 50
					—
					 —
					 —
						ns

Worst case condition: L32 = V_{DD}, L1 through L16 = Don't Care (Any register length from 33 to 64)		5 10 15	400 185 85	50 25 22	— — —	
Rise and Fall Time, Clock	t_r, t_f	5 10 15		No Limit		—
Rise and Fall Time, Reset or $\overline{CE}$	t_r, t_f	5 10 15	— — —	— — —	15 5 4	μs
Removal Time, Reset to Clock or $\overline{CE}$	t_{rem}	5 10 15	160 80 70	80 40 35	— — —	ns

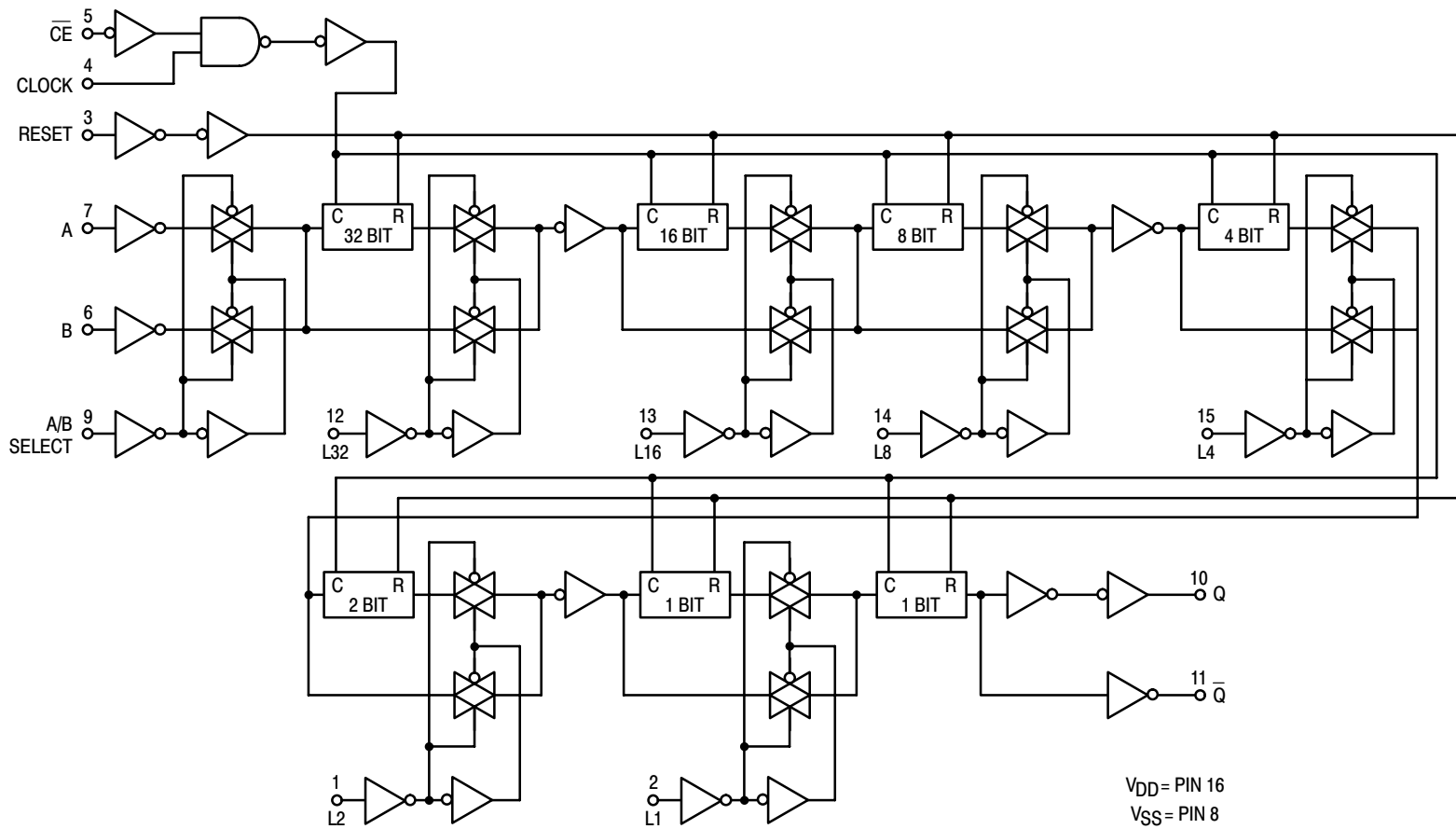7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
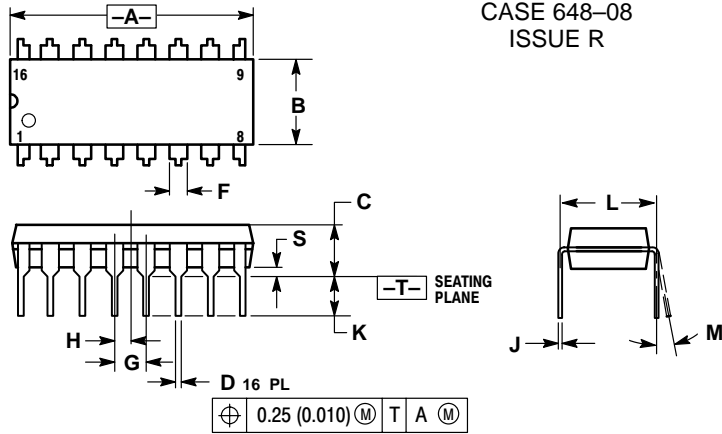
MC14557B

TIMING DIAGRAM

1–bit length:
$\overline{CE} = 0$
A/B = 1
L1 = L2 = L4 = L8 = L16 = L32 = 0
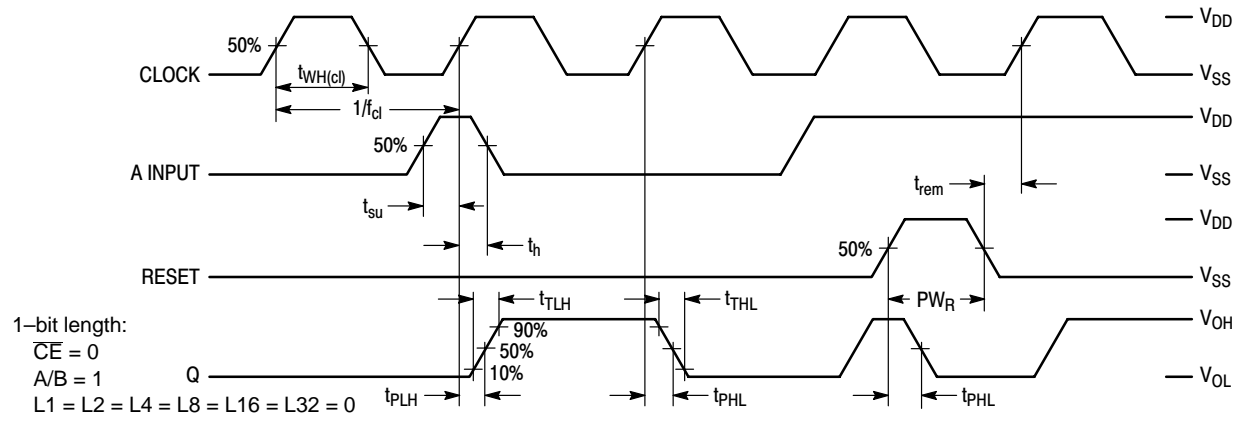
MC14557B

LOGIC DIAGRAM

V_{DD} = PIN 16

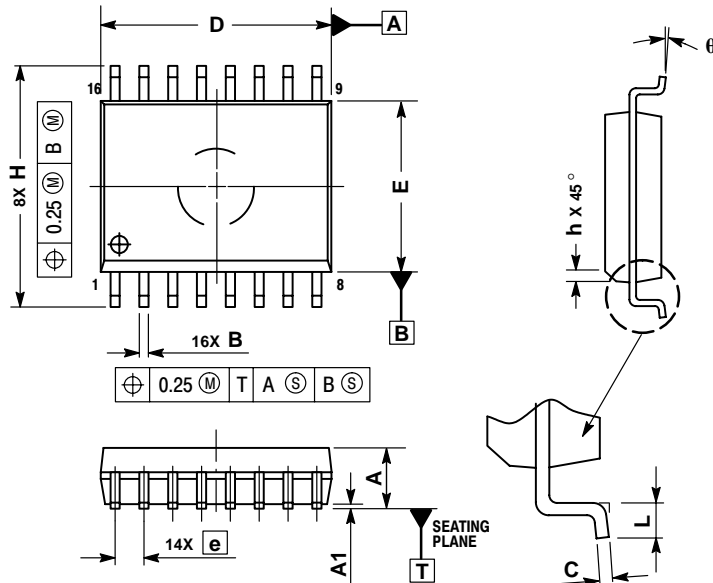V_{SS} = PIN 8

MC14557B

PACKAGE DIMENSIONS

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC–16
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–03
ISSUE B

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

PACKAGE DIMENSIONS

SOEIAJ–16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966–01
ISSUE O
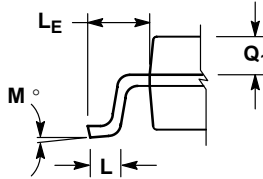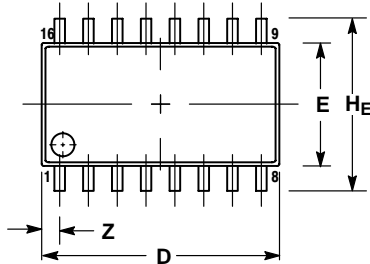
DETAIL P
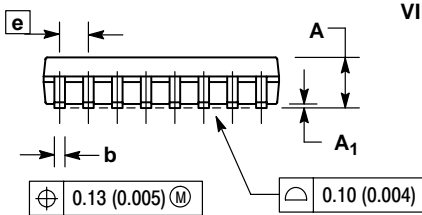
VIEW P
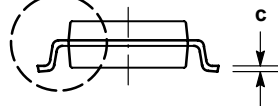
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031