NL27WZ00

Dual 2-Input NAND Gate

The NL27WZ00 is a high performance dual 2–input NAND Gate operating from a 2.3 V to 5.5 V supply.

- Extremely High Speed: t_{PD} 2.4 ns (typical) at V_{CC} = 5 V
- Designed for 2.3 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs
- LVTTL Compatible – Interface Capability With 5 V TTL Logic with V_{CC} = 3 V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Replacement for NC7WZ00
- Chip Complexity: FET = 112

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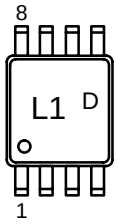
MARKING DIAGRAM

US8
US SUFFIX
CASE 493–01



D = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

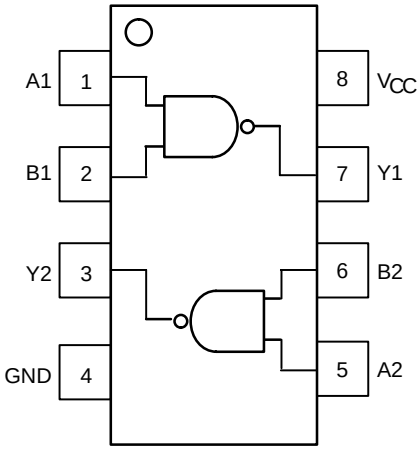


Figure 1. Pinout

Figure 2. Logic Symbol

PIN ASSIGNMENT

Pin	Function
1	A1
2	B1
3	Y2
4	GND
5	A2
6	B2
7	Y1
8	V_{CC}

FUNCTION TABLE

Y = $\overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to +7.0	V
V_O	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
I_O	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	(Note 1)	250	°C/W
P_D	Power Dissipation in Still Air at 85°C		250	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{Latch–Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 85°C (Note 5)	±500	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm–by–1 inch, 2–ounce copper trace with no air flow.
2. Tested to EIA/JESD22–A114–A.
3. Tested to EIA/JESD22–A115–A.
4. Tested to JESD22–C101–A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.3 1.5	5.5 5.5	V
V_I	Input Voltage	(Note 6)	0	5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0	V_{CC}	V
T_A	Operating Free–Air Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 2.5 V ±0.2 V V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	0 0 0	20 10 5	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high– or low–logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}		V
V_{IL}	Low–Level Input Voltage		2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}	V
V_{OH}	High–Level Output Voltage V_{IN} = V_{IL} or V_{IL}	I_{OH} = 100 μA	2.3 to 5.5	V_{CC} − 0.1	V_{CC}		V_{CC} − 0.1		V
		I_{OH} = −8 mA	2.3	1.9	2.1		1.9		
		I_{OH} = −12 mA	2.7	2.2	2.4		2.2		
		I_{OH} = −16 mA	3.0	2.4	2.7		2.4		
		I_{OH} = −24 mA	3.0	2.3	2.5		2.3		
		I_{OH} = −32 mA	4.5	3.8	4.0		3.8		
V_{OL}	Low–Level Output Voltage V_{IN} = V_{IH}	I_{OL} = 100 μA	2.3 to 5.5			0.1		0.1	V
		I_{OL} = 8 mA	2.3		0.20	0.3		0.3	
		I_{OL} = 12 mA	2.7		0.22	0.4		0.4	
		I_{OL} = 16 mA	3.0		0.28	0.4		0.4	
		I_{OL} = 24 mA	3.0		0.38	0.55		0.55	
		I_{OL} = 32 mA	4.5		0.42	0.55		0.55	
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 3.0 ns

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure 3 and 4)	R_L = 1 MΩ, C_L = 15 pF	2.5 ± 0.2	1.2	3.2	5.3	1.2	5.7	ns
		R_L = 1 MΩ, C_L = 15 pF	3.3 ± 0.3	0.8	2.4	3.7	0.8	4.0	
		R_L = 500 Ω, C_L = 50 pF		1.2	3.0	4.6	1.2	4.9	
		R_L = 1 MΩ, C_L = 15 pF	5.0 ± 0.5	0.5	1.9	2.9	0.5	3.2	
		R_L = 500 Ω, C_L = 50 pF		0.8	2.4	3.6	0.8	3.9	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 7)	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	9	pF
		10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	11	

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

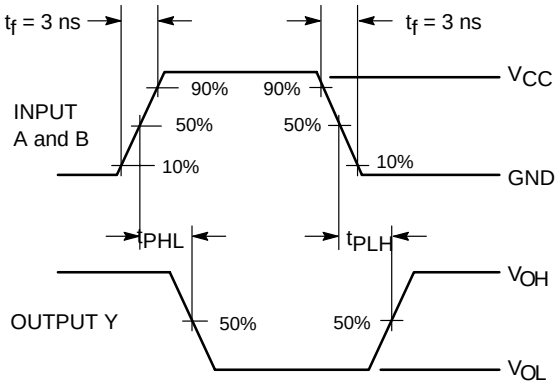
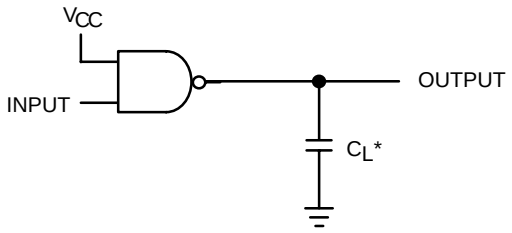


Figure 3. Switching Waveform



*C_L includes all probe and jig capacitances.
A 1–MHz square input wave is recommended
for propagation delay tests.

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix		
NL27WZ00US	NL	2	7	WZ	00	US	US8	178 mm, 3000 Unit

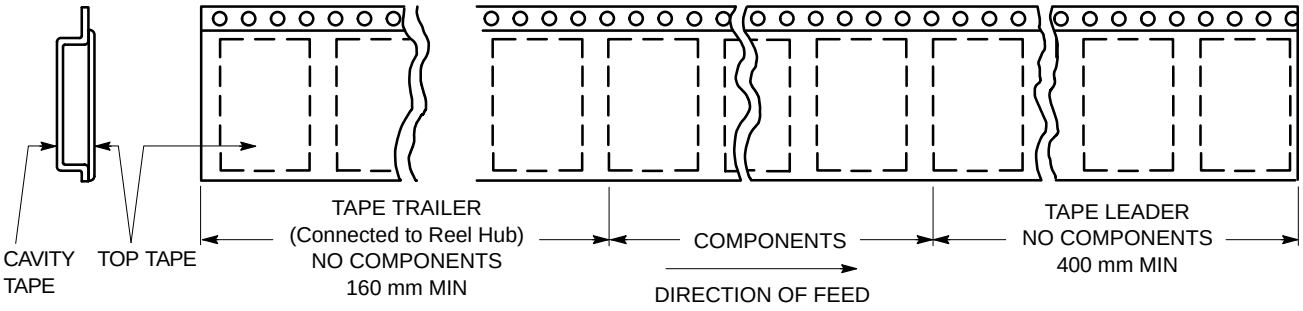


Figure 5. Tape Ends for Finished Goods

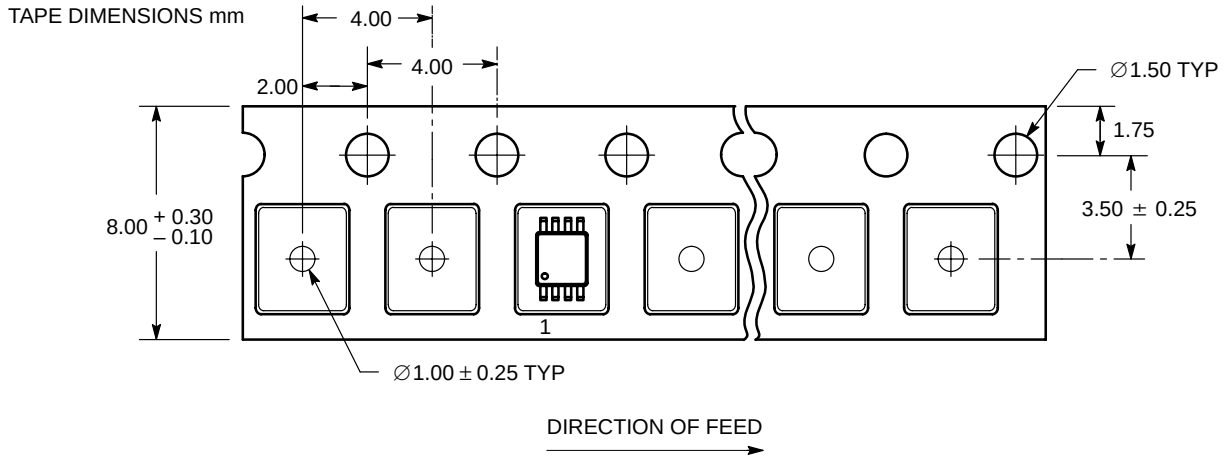


Figure 6. US8 Reel Configuration/Orientation

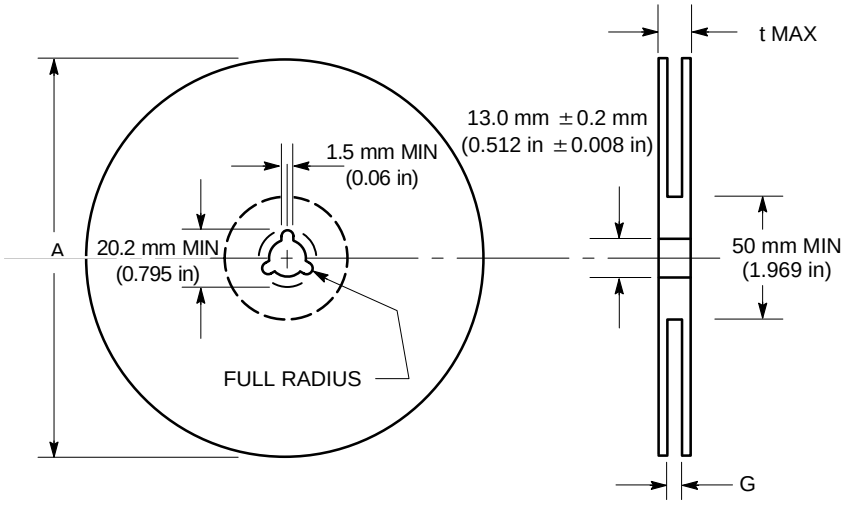


Figure 7. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	US	178 mm (7 in)	8.4 mm, + 1.5 mm, –0.0 (0.33 in + 0.059 in, –0.00)	14.4 mm (0.56 in)

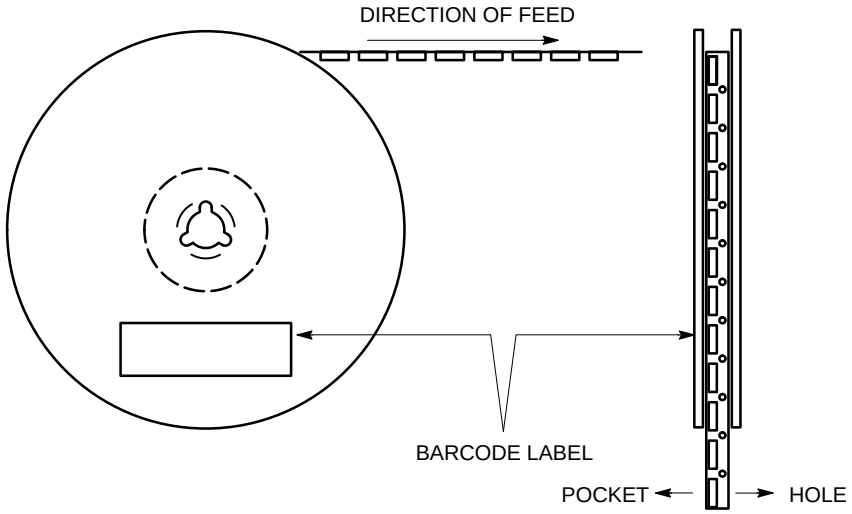
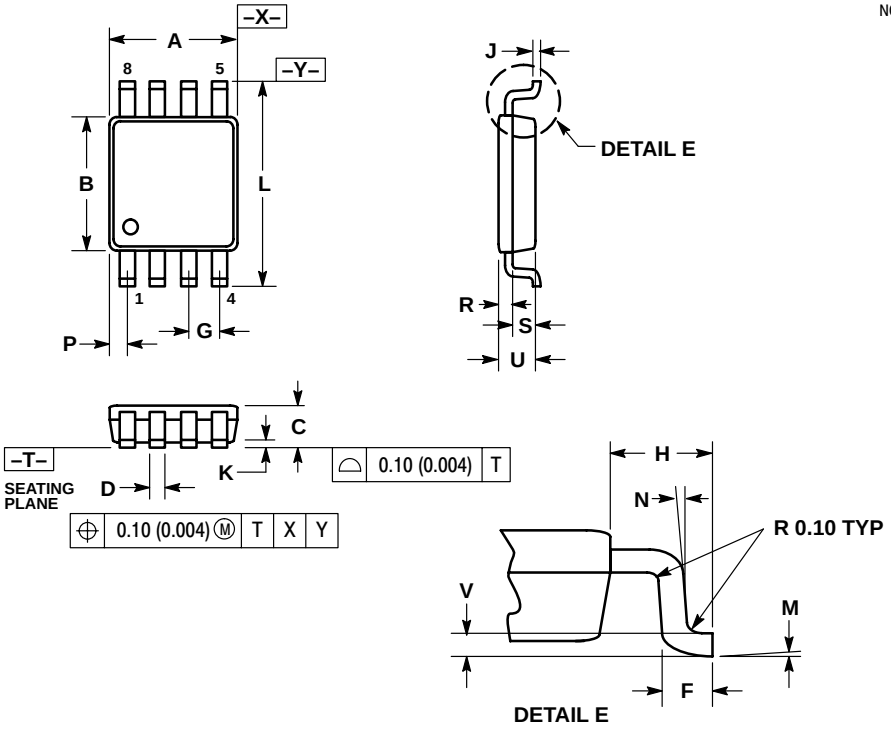


Figure 8. Reel Winding Direction

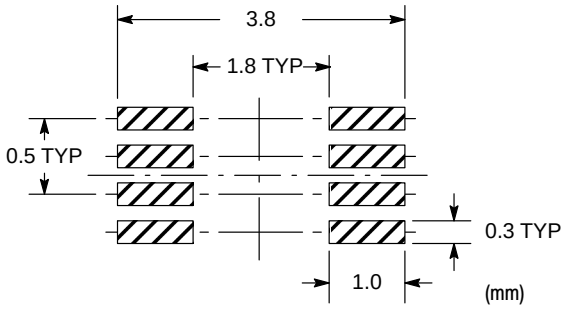
PACKAGE DIMENSIONS

US8
US SUFFIX
CASE 493–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSION. INTER–LEAD FLASH AND PROTRUSION SHALL NOT E3XCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076–0. 0203 MM. (300–800 INCH).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002").

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
P	0.28	0.44	0.011	0.017
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	



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