

MC100LVEL51

3.3V ECL Differential Clock D Flip-Flop

The MC100LVEL51 is a differential clock D flip-flop with reset. The device is functionally equivalent to the EL51 device, but operates from a 3.3 V supply. With propagation delays and output transition times essentially equal to the EL51, the LVEL51 is ideally suited for those applications which require the ultimate in AC performance at 3.3 V V_{CC} .

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the LVEL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to V_{EE} and the \overline{CLK} input will be biased at $V_{CC}/2$.

- 475 ps Propagation Delay
- 2.8 GHz Toggle Frequency
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC}= 3.0\text{ V to }3.8\text{ V}$ with $V_{EE}= 0\text{ V}$
- NECL Mode Operating Range: $V_{CC}= 0\text{ V}$ with $V_{EE}= -3.0\text{ V to }-3.8\text{ V}$
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 114 devices



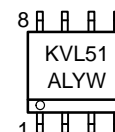
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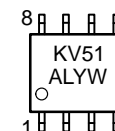
MARKING DIAGRAMS*



SO-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

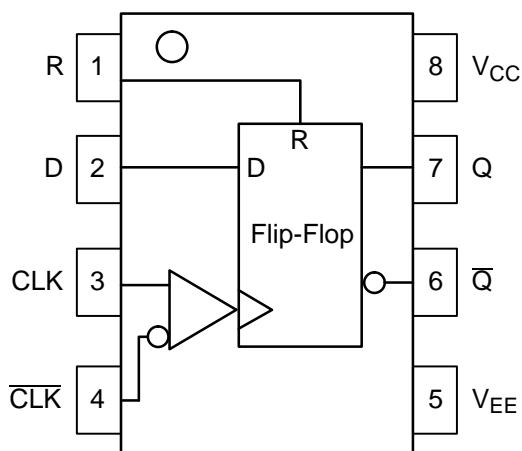
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

| Device | Package | Shipping |
|-----------------|---------|-----------------|
| MC100LVEL51D | SO-8 | 98 Units / Rail |
| MC100LVEL51DR2 | SO-8 | 2500 / Reel |
| MC100LVEL51DT | TSSOP-8 | 98 Units / Rail |
| MC100LVEL51DTR2 | TSSOP-8 | 2500 / Reel |

MC100LVEL51

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

| PIN | FUNCTION |
|------------------------------|------------------------------|
| CLK, $\overline{\text{CLK}}$ | ECL Differential Clock Input |
| Q, $\overline{\text{Q}}$ | ECL Differential Output |
| D | ECL D Input |
| R | ECL Reset Input |
| V _{CC} | Positive Supply |
| V _{EE} | Negative Supply |

TRUTH TABLE

| D | R | CLK | Q |
|---|---|-----|---|
| L | L | Z | L |
| H | L | Z | H |
| X | H | X | L |

Z = LOW to HIGH Transition
X = Don't Care

MAXIMUM RATINGS (Note 1.)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|------------------|--|-----------------------|----------------------------------|---------------|--------------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 8 to 0 | V |
| V _{EE} | NECL Mode Power Supply | V _{CC} = 0 V | | -8 to 0 | V |
| V _I | PECL Mode Input Voltage | V _{EE} = 0 V | V _I ≤ V _{CC} | 6 to 0 | V |
| | NECL Mode Input Voltage | V _{CC} = 0 V | V _I ≥ V _{EE} | -6 to 0 | V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction to Ambient) | 0 LFPM 500 LFPM | 8 SOIC 8 SOIC | 190 130 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction to Case) | std bd | 8 SOIC | 41 to 44 ± 5% | °C/W |
| θ _{JA} | Thermal Resistance (Junction to Ambient) | 0 LFPM 500 LFPM | 8 TSSOP 8 TSSOP | 185 140 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction to Case) | std bd | 8 TSSOP | 41 to 44 ± 5% | °C/W |
| T _{sol} | Wave Solder | <2 to 3 sec @ 248°C | | 265 | °C |

1. Maximum Ratings are those values beyond which device damage may occur.

MC100LVEL51

LVPECL DC CHARACTERISTICS $V_{CC}=3.3\text{ V}$; $V_{EE}=0.0\text{ V}$ (Note 1)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 30 | 35 | | 30 | 35 | | 32 | 37 | mA |
| V_{OH} | Output HIGH Voltage (Note 2.) | 2215 | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| V_{OL} | Output LOW Voltage (Note 2.) | 1470 | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| V_{IH} | Input HIGH Voltage (Single Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 3.) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$ | 1.2 | | 3.0 | 1.1 | | 3.0 | 1.1 | | 3.0 | V |
| | | 1.4 | | 3.0 | 1.3 | | 3.0 | 1.3 | | 3.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current Others CLK | 0.5 | | | 0.5 | | | 0.5 | | | μA |
| | | -600 | | | -600 | | | -600 | | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2$ volts.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1 V.

LVNECL DC CHARACTERISTICS $V_{CC}=0.0\text{ V}$; $V_{EE}=-3.3\text{ V}$ (Note 1.)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 30 | 35 | | 30 | 35 | | 32 | 37 | mA |
| V_{OH} | Output HIGH Voltage (Note 2.) | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 2.) | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single Ended) | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 3.) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$ | -2.1 | | -0.3 | -2.2 | | -0.3 | -2.2 | | -0.3 | V |
| | | -1.9 | | -0.3 | -2.0 | | -0.3 | -2.0 | | -0.3 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current Others CLK | 0.5 | | | 0.5 | | | 0.5 | | | μA |
| | | -600 | | | -600 | | | -600 | | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2$ volts.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1 V.

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AC CHARACTERISTICS $V_{CC}= 3.3\text{ V}$; $V_{EE}= 0.0\text{ V}$ or $V_{CC}= 0.0\text{ V}$; $V_{EE}= -3.3\text{ V}$ (Note 1.)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------------------|---|------------|------------|------------|------------|------------|------------|------------|------------|------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{\max} | Maximum Toggle Frequency | 2.7 | | | 2.8 | | | 2.9 | | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay to Output CLK R | 330 340 | 465 455 | 510 540 | 340 350 | 475 765 | 520 550 | 370 390 | 530 510 | 550 590 | ps |
| t_{S} | Setup Time | 150 | 0 | | 150 | 0 | | 150 | 0 | | ps |
| t_{H} | Hold Time | 200 | 100 | | 200 | 100 | | 200 | 100 | | ps |
| t_{RR} | Reset Recovery | 350 | 200 | | 350 | 200 | | 350 | 200 | | ps |
| t_{PW} | Minimum Pulse Width CLK Reset | 400 500 | | | 400 500 | | | 400 500 | | | ps |
| t_{JITTER} | Cycle-to-Cycle Jitter | | TBD | | | TBD | | | TBD | | ps |
| V_{PP} | Input Swing (Note 2.) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| t_{r} t_{f} | Output Rise/Fall Times Q (20% – 80%) | 120 | | 320 | 120 | | 320 | 120 | | 320 | ps |

- V_{EE} can vary $\pm 0.3\text{ V}$.
- $V_{\text{PP}}(\text{min})$ is minimum input swing for which AC parameters are guaranteed.

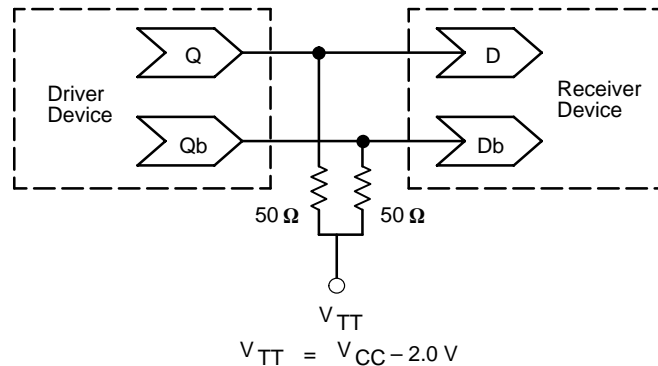


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

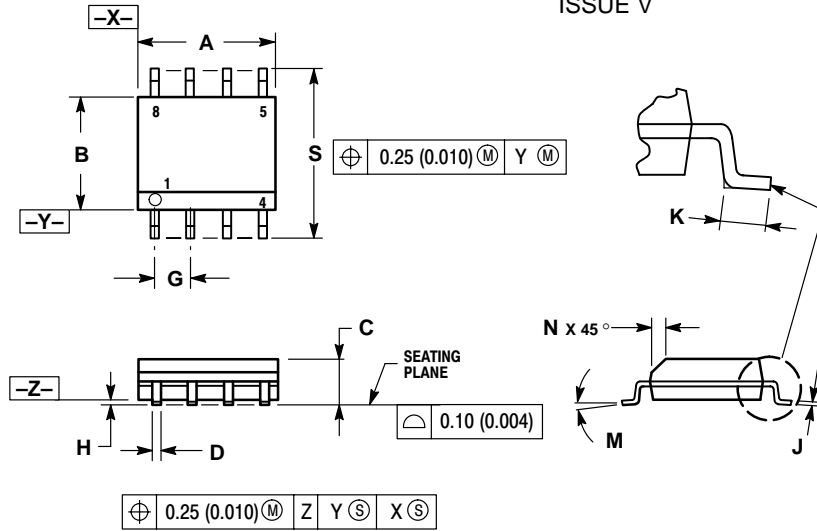
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire–OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

MC100LVEL51

PACKAGE DIMENSIONS

SO-8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-07
ISSUE V



NOTES:

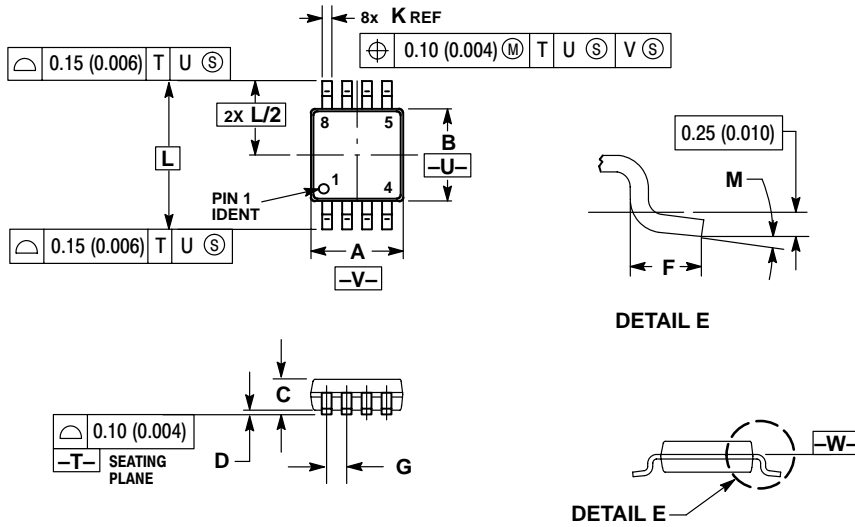
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

MC100LVEL51

PACKAGE DIMENSIONS


TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 BSC | | 0.193 BSC | |
| M | 0° | 6° | 0° | 6° |

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