

# NTMD6P02R2

Preferred Device

## Power MOSFET 6 Amps, 20 Volts P-Channel SO-8, Dual

### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual SO-8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SO-8 Mounting Information Provided

### Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	-20	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 12$	V
Thermal Resistance – Junction-to-Ambient (Note 1.)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	2.0	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	-7.8	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	-5.7	A
Maximum Operating Power Dissipation	$P_D$	0.5	W
Maximum Operating Drain Current	$I_D$	-3.89	A
Pulsed Drain Current (Note 4.)	$I_{DM}$	-40	A
Thermal Resistance – Junction-to-Ambient (Note 2.)	$R_{\theta JA}$	98	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.28	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	-6.2	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	-4.6	A
Maximum Operating Power Dissipation	$P_D$	0.3	W
Maximum Operating Drain Current	$I_D$	-3.01	A
Pulsed Drain Current (Note 4.)	$I_{DM}$	-35	A
Thermal Resistance – Junction-to-Ambient (Note 3.)	$R_{\theta JA}$	166	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	0.75	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	-4.8	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	-3.5	A
Maximum Operating Power Dissipation	$P_D$	0.2	W
Maximum Operating Drain Current	$I_D$	-2.48	A
Pulsed Drain Current (Note 4.)	$I_{DM}$	-30	A

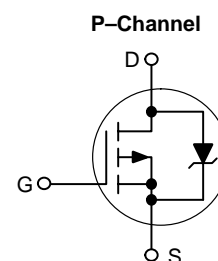
1. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz. Cu 0.06" thick single sided),  $t = 10$  seconds.
2. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz. Cu 0.06" thick single sided),  $t =$  steady state.
3. Minimum FR-4 or G-10 PCB,  $t =$  steady state.
4. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2%.



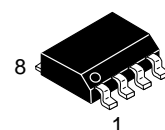
ON Semiconductor™

<http://onsemi.com>

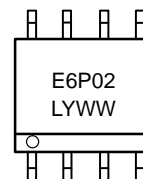
**6 AMPERES  
20 VOLTS  
 $R_{DS(on)} = 33 \text{ m}\Omega$**



### MARKING DIAGRAM

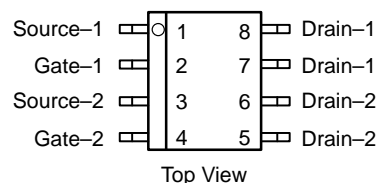


SO-8, Dual  
CASE 751  
STYLE 11



L = Location Code  
Y = Year  
WW = Work Week

### PIN ASSIGNMENT



Top View

### ORDERING INFORMATION

Device	Package	Shipping
NTMD6P02R2	SO-8	2500 Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

# NTMD6P02R2

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Rating	Symbol	Value	Unit
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = -20\text{ Vdc}$ , $V_{GS} = -5.0\text{ Vdc}$ , Peak $I_L = -5.0\text{ Apk}$ , $L = 40\text{ mH}$ , $R_G = 25\ \Omega$ )	$E_{AS}$	500	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	$T_L$	260	$^\circ\text{C}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted) \*

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = -250\ \mu\text{Adc}$ ) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	-20 –	– -11.6	– –	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ( $V_{DS} = -20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 25^\circ\text{C}$ ) ( $V_{DS} = -20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 70^\circ\text{C}$ )	$I_{DSS}$	– –	– –	-1.0 -5.0	$\mu\text{Adc}$
Gate-Body Leakage Current ( $V_{GS} = -12\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	–	–	-100	nAdc
Gate-Body Leakage Current ( $V_{GS} = +12\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	–	–	100	nAdc

### ON CHARACTERISTICS

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = -250\ \mu\text{Adc}$ ) Temperature Coefficient (Negative)	$V_{GS(th)}$	-0.6 –	-0.88 2.6	-1.20 –	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-State Resistance ( $V_{GS} = -4.5\text{ Vdc}$ , $I_D = -6.2\text{ Adc}$ ) ( $V_{GS} = -2.5\text{ Vdc}$ , $I_D = -5.0\text{ Adc}$ ) ( $V_{GS} = -2.5\text{ Vdc}$ , $I_D = -3.1\text{ Adc}$ )	$R_{DS(on)}$	– – –	0.027 0.038 0.038	0.033 0.050 –	$\Omega$
Forward Transconductance ( $V_{DS} = -10\text{ Vdc}$ , $I_D = -6.2\text{ Adc}$ )	$g_{FS}$	–	15	–	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = -16\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$C_{iss}$	–	1380	1700	pF
Output Capacitance		$C_{oss}$	–	515	775	
Reverse Transfer Capacitance		$C_{rss}$	–	250	450	

### SWITCHING CHARACTERISTICS (Notes 5. and 6.)

Turn-On Delay Time	$(V_{DD} = -10\text{ Vdc}$ , $I_D = -1.0\text{ Adc}$ , $V_{GS} = -10\text{ Vdc}$ , $R_G = 6.0\ \Omega$ )	$t_{d(on)}$	–	15	25	ns
Rise Time		$t_r$	–	20	50	
Turn-Off Delay Time		$t_{d(off)}$	–	85	125	
Fall Time		$t_f$	–	50	110	
Turn-On Delay Time	$(V_{DD} = -16\text{ Vdc}$ , $I_D = -6.2\text{ Adc}$ , $V_{GS} = -4.5\text{ Vdc}$ , $R_G = 6.0\ \Omega$ )	$t_{d(on)}$	–	17	–	ns
Rise Time		$t_r$	–	65	–	
Turn-Off Delay Time		$t_{d(off)}$	–	50	–	
Fall Time		$t_f$	–	80	–	
Total Gate Charge	$(V_{DS} = -16\text{ Vdc}$ , $V_{GS} = -4.5\text{ Vdc}$ , $I_D = -6.2\text{ Adc}$ )	$Q_{tot}$	–	20	35	nC
Gate-Source Charge		$Q_{gs}$	–	4.0	–	
Gate-Drain Charge		$Q_{gd}$	–	8.0	–	

5. Indicates Pulse Test: Pulse Width = 300  $\mu\text{s}$  max, Duty Cycle = 2%.

6. Switching characteristics are independent of operating junction temperature.

\* Handling precautions to protect against electrostatic discharge is mandatory.

# NTMD6P02R2

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted) (continued) \*

Characteristic		Symbol	Min	Typ	Max	Unit
<b>BODY-DRAIN DIODE RATINGS</b> (Note 5.)						
Diode Forward On-Voltage	( $I_S = -1.7 \text{ Adc}$ , $V_{GS} = 0 \text{ Vdc}$ ) ( $I_S = -1.7 \text{ Adc}$ , $V_{GS} = 0 \text{ Vdc}$ , $T_J = 125^\circ\text{C}$ )	$V_{SD}$	—	-0.80 -0.65	-1.2 —	Vdc
Diode Forward On-Voltage	( $I_S = -6.2 \text{ Adc}$ , $V_{GS} = 0 \text{ Vdc}$ ) ( $I_S = -6.2 \text{ Adc}$ , $V_{GS} = 0 \text{ Vdc}$ , $T_J = 125^\circ\text{C}$ )	$V_{SD}$	—	-0.95 -0.80	— —	Vdc
Reverse Recovery Time	( $I_S = -1.7 \text{ Adc}$ , $V_{GS} = 0 \text{ Vdc}$ , $dI_S/dt = 100 \text{ A}/\mu\text{s}$ )	$t_{rr}$	—	50	80	ns
		$t_a$	—	20	—	
		$t_r$	—	30	—	
Reverse Recovery Stored Charge		$Q_{RR}$	—	0.04	—	$\mu\text{C}$

5. Indicates Pulse Test: Pulse Width = 300  $\mu\text{s}$  max, Duty Cycle = 2%.

\* Handling precautions to protect against electrostatic discharge is mandatory.

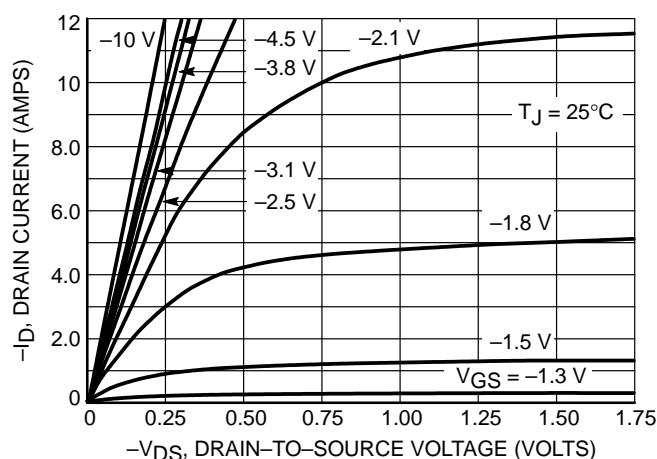


Figure 1. On-Region Characteristics

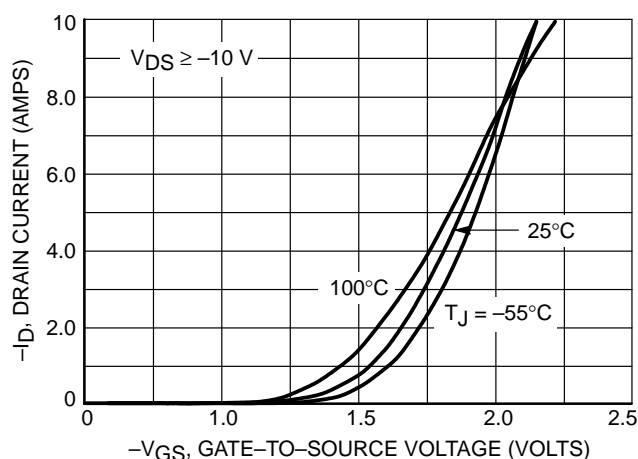


Figure 2. Transfer Characteristics

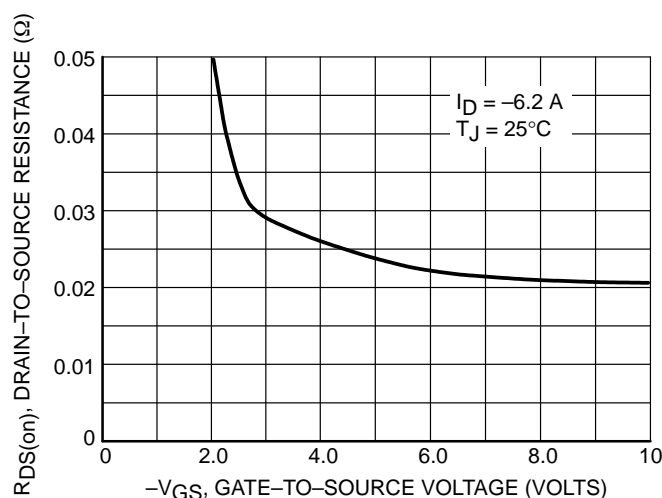


Figure 3. On-Resistance versus Gate-To-Source Voltage

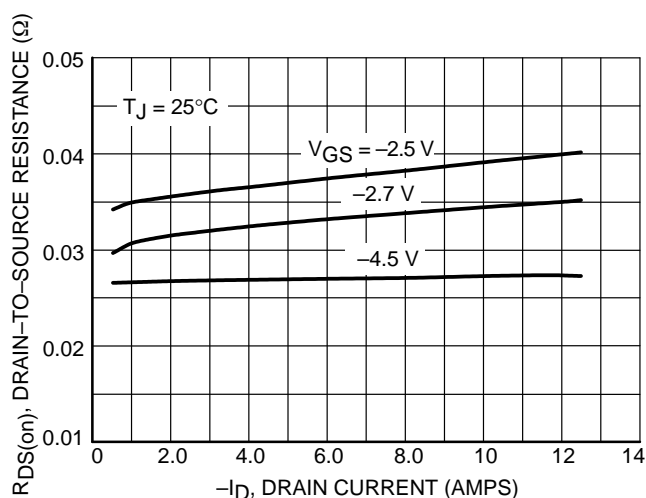


Figure 4. On-Resistance versus Drain Current and Gate Voltage

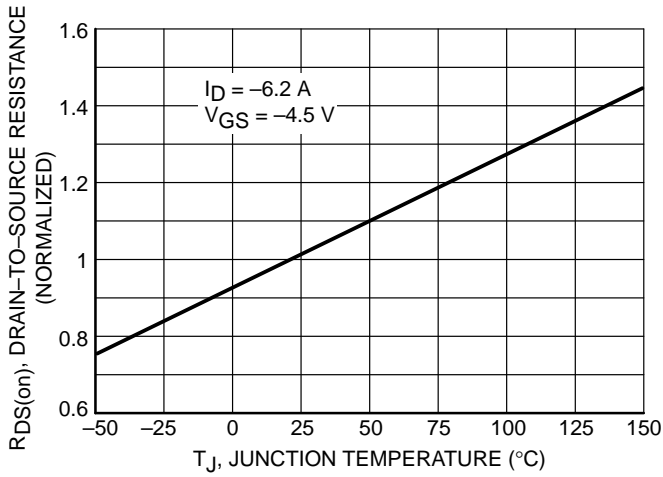


Figure 5. On-Resistance Variation with Temperature

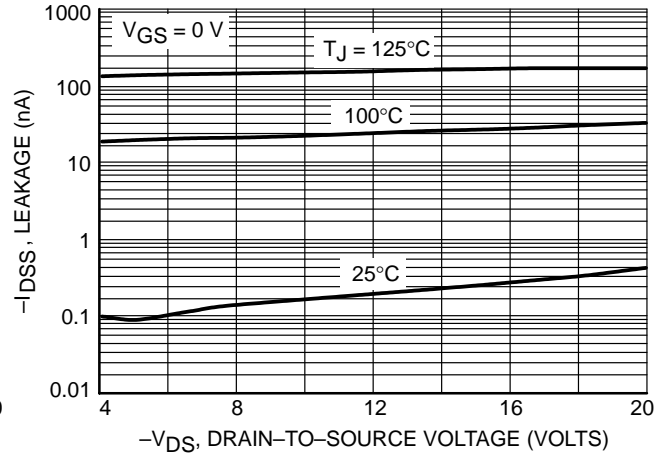


Figure 6. Drain-To-Source Leakage Current versus Voltage

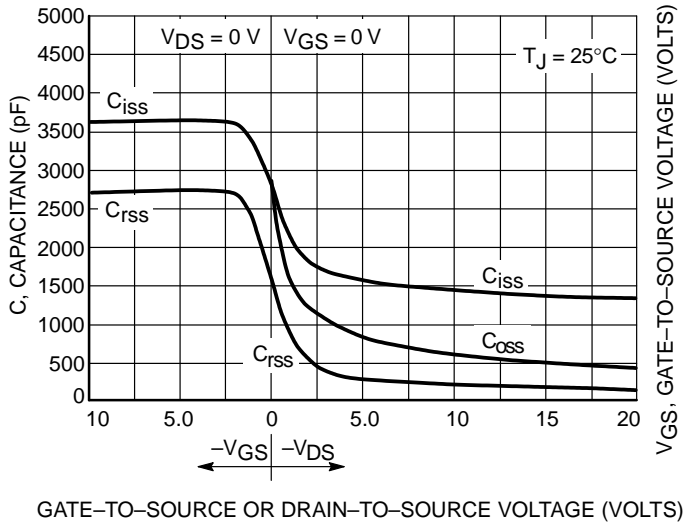


Figure 7. Capacitance Variation

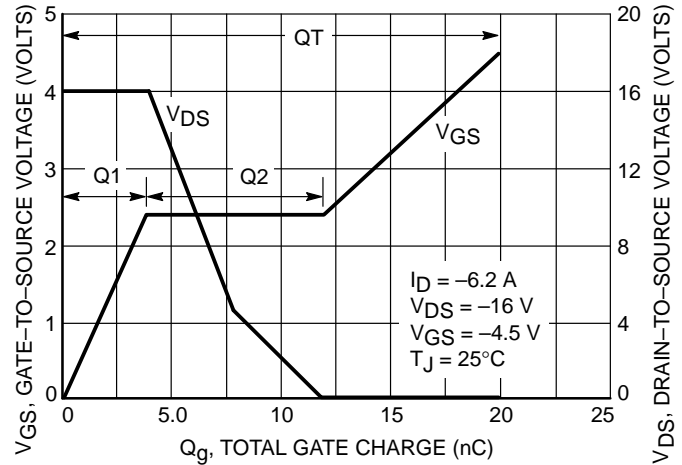


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

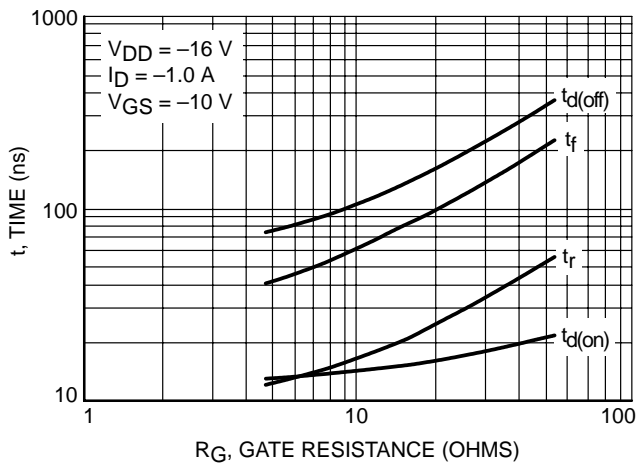


Figure 9. Resistive Switching Time Variation versus Gate Resistance

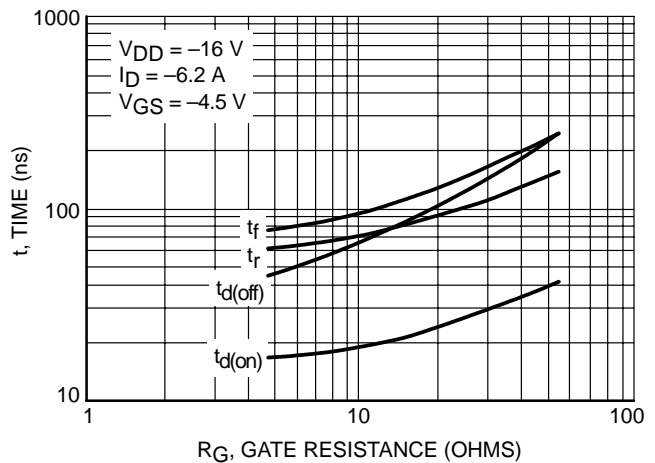


Figure 10. Resistive Switching Time Variation versus Gate Resistance

# NTMD6P02R2

## DRAIN-TO-SOURCE DIODE CHARACTERISTICS

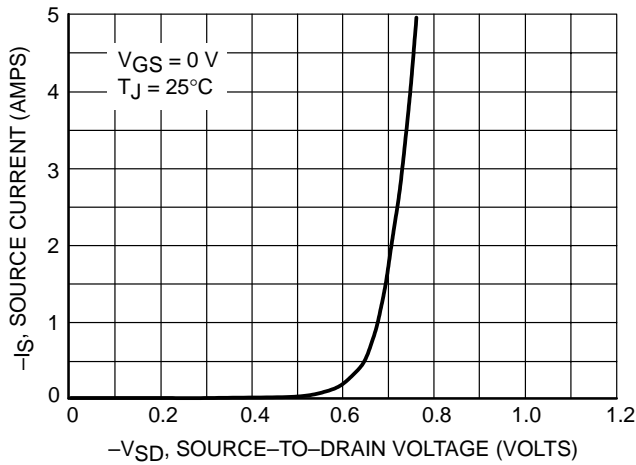


Figure 11. Diode Forward Voltage versus Current

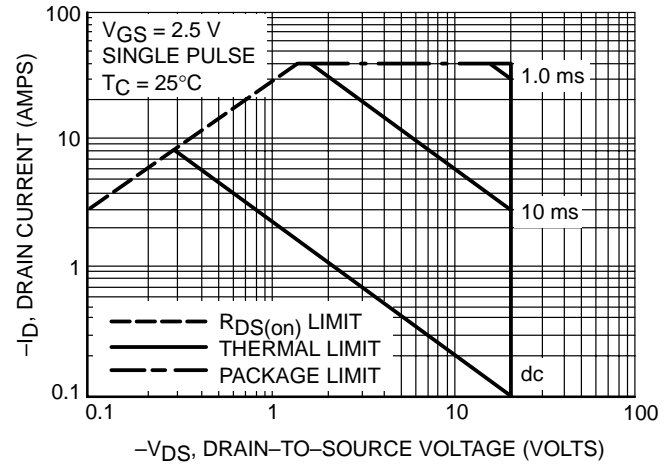


Figure 12. Maximum Rated Forward Biased Safe Operating Area

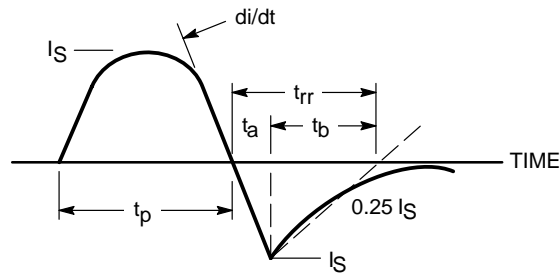


Figure 13. Diode Reverse Recovery Waveform

## TYPICAL ELECTRICAL CHARACTERISTICS

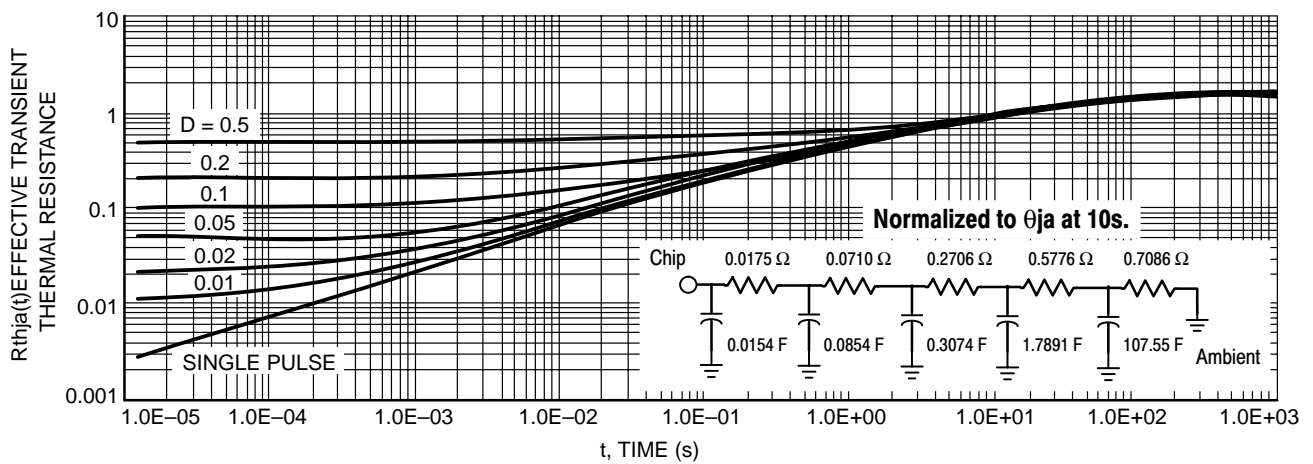


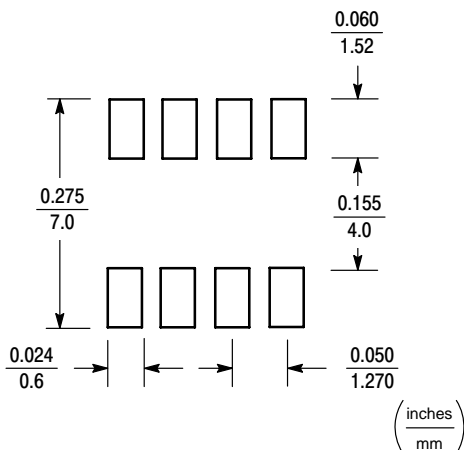
Figure 14. Thermal Response

## INFORMATION FOR USING THE SO-8 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.



### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.

- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows

temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

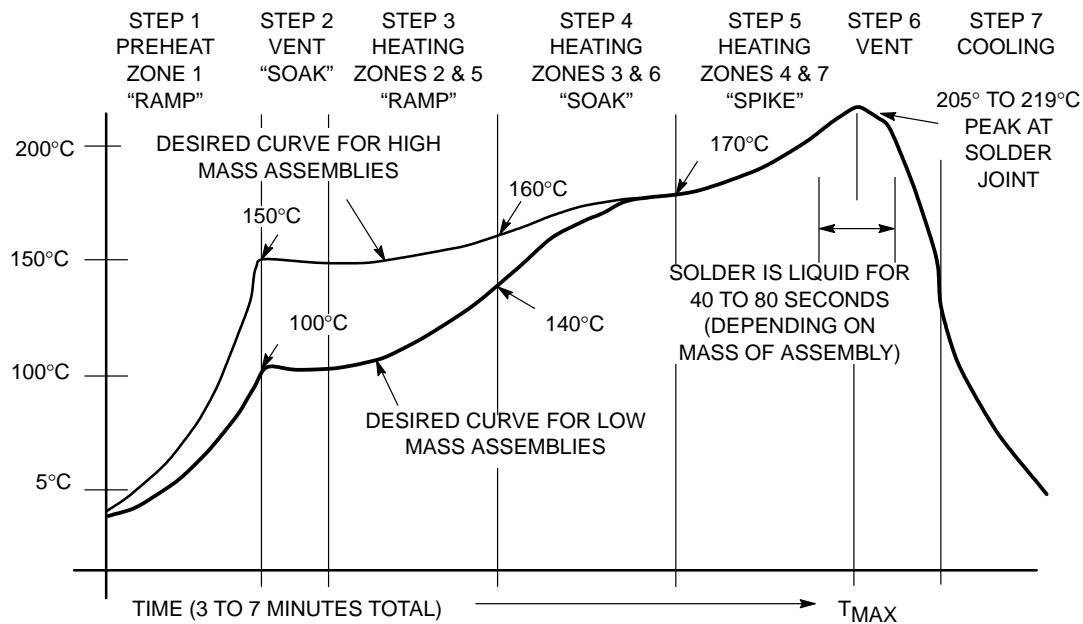
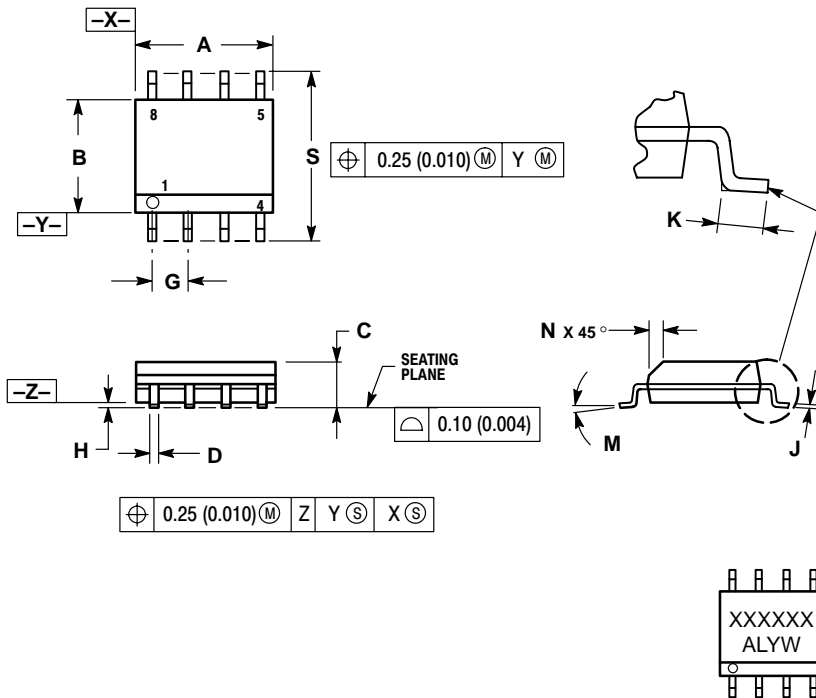


Figure 15. Typical Solder Heating Profile

# NTMD6P02R2

## PACKAGE DIMENSIONS

SO-8  
CASE 751-07  
ISSUE V



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### STYLE 11:

- PIN 1: SOURCE 1  
2. GATE 1  
3. SOURCE 2  
4. GATE 2  
5. DRAIN 2  
6. DRAIN 2  
7. DRAIN 1  
8. DRAIN 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

### N. American Technical Support: 800-282-9855 Toll Free USA/Canada

### EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)  
Email: ONlit-german@hibbertco.com  
French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)  
Email: ONlit-french@hibbertco.com  
English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)  
Email: ONlit@hibbertco.com

### EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781

\*Available from Germany, France, Italy, UK, Ireland

### CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
Email: ONlit-spanish@hibbertco.com  
Toll-Free from Mexico: Dial 01-800-288-2872 for Access –  
then Dial 866-297-9322

### ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong & Singapore:  
001-800-4422-3781  
Email: ONlit-asia@hibbertco.com

### JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
Phone: 81-3-5740-2700  
Email: r14525@onsemi.com

### ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.