

# CS8251

## 10 V/5.0 V Low Dropout Dual Regulator with Independent Output Enables

The CS8251 is a 10 V/5.0 V dual output linear regulator. The 10 V  $\pm$  5.0% output sources 1.0 A, while the 5.0 V  $\pm$  5.0% output sources 250 mA. Each output is controlled by its own ENABLE pin. Setting the ENABLE input high turns on the associated regulator output. Holding both ENABLE inputs low puts the IC into sleep mode where current consumption is less than 50  $\mu$ A.

The regulator is protected against overvoltage, short circuit and thermal runaway conditions.

The CS8251 is available in a 7 lead TO-220 package with copper tab. The tab can be connected to a heat sink if necessary.

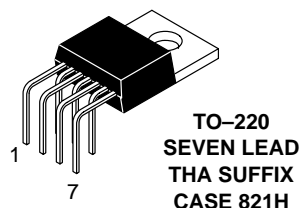
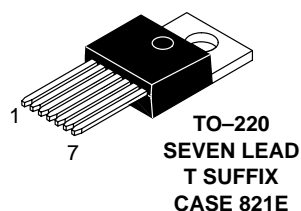
### Features

- Two Regulated Outputs
  - 10 V  $\pm$  5.0%, 1.0 A
  - 5.0 V  $\pm$  5.0%, 250 mA
- Independent ENABLE for Each Output
- Separate Sense Feedback Pin for 10 V Output
- 50  $\mu$ A Sleep Mode Current
- Fault Protection
  - Overvoltage Shutdown
  - 74 V Peak Transient
  - Short Circuit
  - Thermal Shutdown
- CMOS Compatible, Low Current ENABLE Inputs



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Tab = GND  
Pin 1. ENABLE1  
2. ENABLE2  
3. V<sub>OUT2</sub>  
4. GND  
5. Sense  
6. V<sub>CC</sub>  
7. V<sub>OUT1</sub>

### MARKING DIAGRAM



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
CS8251ET7	TO-220* STRAIGHT	50 Units/Rail
CS8251ETVA7	TO-220* VERTICAL	50 Units/Rail
CS8251ETHA7	TO-220* HORIZONTAL	50 Units/Rail

\*Seven lead.

# CS8251

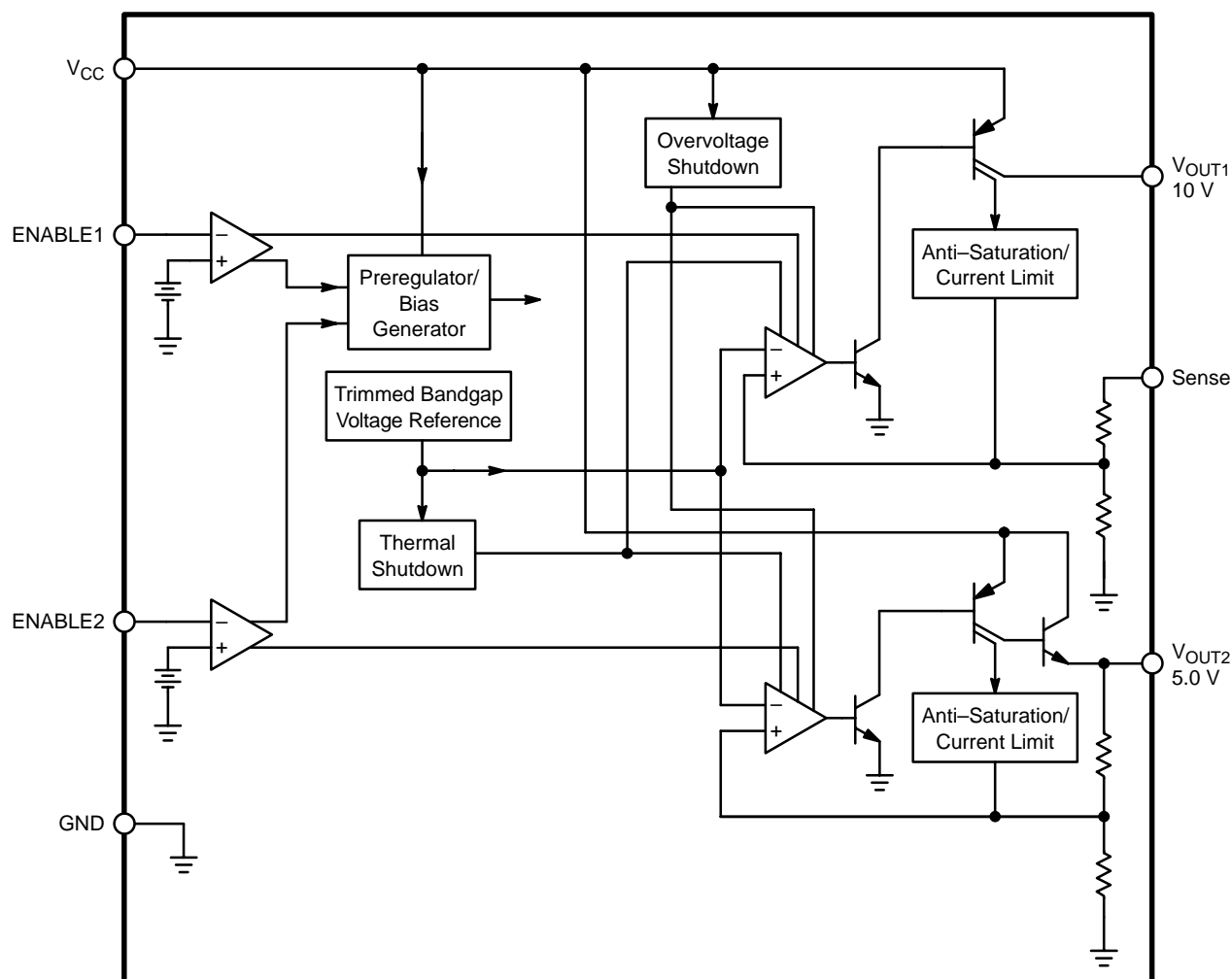


Figure 1. Block Diagram

## ABSOLUTE MAXIMUM RATINGS\*

Rating	Value	Unit	
Supply Voltage Operating Range	-0.6 to +24	V	
ENABLE Input Voltage Range	-0.6 to +10	V	
Peak Transient Voltage (60V Load Dump @ $V_{CC} = 14\text{ V}$ )	74	V	
Storage Temperature Range	-65 to +150	°C	
Junction Temperature Range	-40 to +150	°C	
ESD Susceptibility (Human Body Model)	2.0	kV	
Lead Temperature Soldering	Wave Solder (through hole styles only) Note 1.	260 peak	°C

1. 10 seconds max.

\*The maximum package power dissipation must be observed.

# CS8251

**ELECTRICAL CHARACTERISTICS** ( $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ ,  $11\text{ V} \leq V_{\text{CC}} \leq 16\text{ V}$ ,  $\text{ENABLE1} = \text{ENABLE2} = 5.0\text{ V}$ ,  $I_{\text{OUT1}} = I_{\text{OUT2}} = 5.0\text{ mA}$ ; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
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## Primary Output ( $V_{\text{OUT1}}$ )

Output Voltage	$I_{\text{OUT1}} = 1.0\text{ A}$ , $11.1\text{ V} \leq V_{\text{CC}} \leq 16\text{ V}$	9.5	10	10.5	V
Line Regulation	$11.1\text{ V} \leq V_{\text{CC}} \leq 26\text{ V}$	–	–	50	mV
Load Regulation	$5.0\text{ mA} \leq I_{\text{OUT1}} \leq 1.0\text{ A}$	–	–	150	mV
Sleep Mode Quiescent Current	$V_{\text{CC}} = 14\text{ V}$ , $\text{ENABLE1} = \text{ENABLE2} = 0\text{ V}$	–	–	50	$\mu\text{A}$
Quiescent Current	$V_{\text{CC}} = 14\text{ V}$ , $I_{\text{OUT1}} = 1.0\text{ A}$ , $I_{\text{OUT2}} = 250\text{ mA}$	–	–	208	mA
Dropout Voltage	$I_{\text{OUT1}} = 5.0\text{ mA}$	–	–	300	mV
	$I_{\text{OUT1}} = 1.0\text{ A}$	–	–	900	mV
Quiescent Bias Current	$I_{\text{OUT1}} = 5.0\text{ mA}$ , $\text{ENABLE2} = 0\text{ V}$ , $V_{\text{CC}} = 14\text{ V}$ , $I_{\text{Q}} = I_{\text{CC}} - I_{\text{OUT1}}$	–	–	10	mA
	$I_{\text{OUT1}} = 1.0\text{ A}$ , $\text{ENABLE2} = 0\text{ V}$ , $V_{\text{CC}} = 14\text{ V}$ , $I_{\text{Q}} = I_{\text{CC}} - I_{\text{OUT1}}$	–	–	200	mA
Ripple Rejection	$f = 120\text{ Hz}$ , $V_{\text{CC}} = 14\text{ V}$ with $1.0\text{ V}_{\text{P-P}}$ AC	–	54	–	dB
Current Limit	$11.1\text{ V} \leq V_{\text{CC}} \leq 26\text{ V}$	1.3	–	2.5	A

## Secondary Output ( $V_{\text{OUT2}}$ )

Output Voltage	$I_{\text{OUT2}} = 250\text{ mA}$	4.75	5.0	5.25	V
	$V_{\text{CC}} = 50\text{ V}$ transient	–	–	6.0	V
Line Regulation	$7.0\text{ V} \leq V_{\text{CC}} \leq 26\text{ V}$	–	–	40	mV
Load Regulation	$5.0\text{ mA} \leq I_{\text{OUT2}} \leq 250\text{ mA}$	–	–	100	mV
Dropout Voltage	$I_{\text{OUT2}} = 5.0\text{ mA}$	–	–	1.2	V
	$I_{\text{OUT2}} = 250\text{ mA}$	–	–	1.8	V
Quiescent Bias Current	$I_{\text{OUT2}} = 5.0\text{ mA}$ , $\text{ENABLE1} = 0\text{ V}$ , $V_{\text{CC}} = 14\text{ V}$ , $I_{\text{Q}} = I_{\text{CC}} - I_{\text{OUT2}}$	–	–	5.0	mA
	$I_{\text{OUT2}} = 250\text{ mA}$ , $\text{ENABLE1} = 0\text{ V}$ , $V_{\text{CC}} = 14\text{ V}$ , $I_{\text{Q}} = I_{\text{CC}} - I_{\text{OUT2}}$	–	–	8.0	mA
Ripple Rejection	$f = 120\text{ Hz}$ , $V_{\text{CC}} = 14\text{ V}$ with $1.0\text{ V}_{\text{P-P}}$ AC	–	54	–	dB
Current Limit	$7.0\text{ V} \leq V_{\text{CC}} \leq 26\text{ V}$	300	–	600	mA

## ENABLE Function (ENABLE)

Input Current	$V_{\text{CC}} = 14\text{ V}$ , $0\text{ V} \leq \text{ENABLE} \leq 5.5\text{ V}$	–150	–	150	$\mu\text{A}$
Input Voltage	Low	0	–	0.8	V
	High	2.0	–	5.0	V

## Protection Circuitry

Overvoltage Shutdown	–	24	–	32	V
Thermal Shutdown	–	–	180	–	$^{\circ}\text{C}$
Thermal Hysteresis	–	–	30	–	$^{\circ}\text{C}$

## PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
TO-220		
1	ENABLE1	ENABLE control for the 10 V, 1.0 A output.
2	ENABLE2	ENABLE control for the 5.0 V, 250 mA output.
3	V <sub>OUT2</sub>	5.0 V $\pm$ 5.0%, 250 mA regulated output.
4	GND	Ground.
5	Sense	Sense feedback for the primary 10 V output.
6	V <sub>CC</sub>	Supply voltage, usually from battery.
7	V <sub>OUT1</sub>	10 V $\pm$ 5.0 %, 1.0 A regulated output.

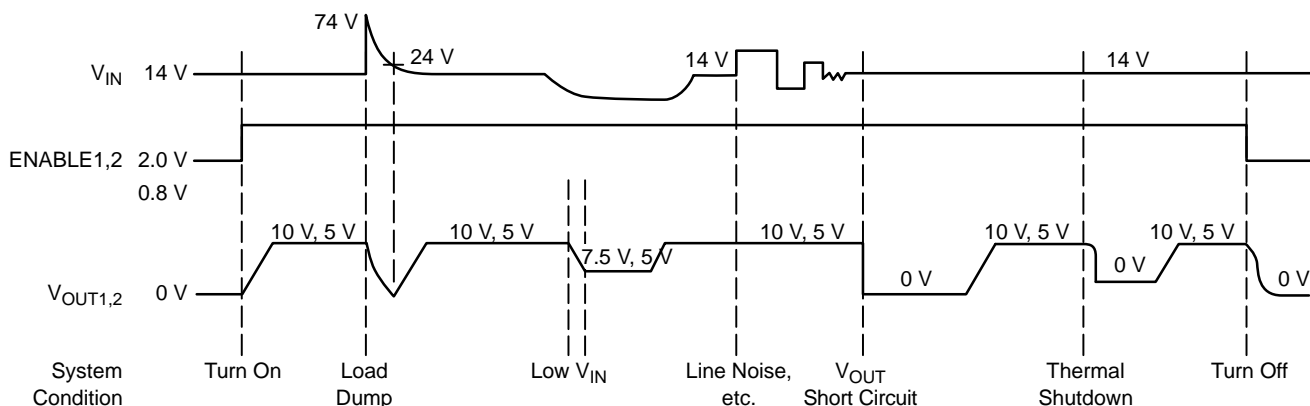


Figure 2. Typical Circuit Waveform

## DEFINITION OF TERMS

**Dropout Voltage:** The input–output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

**Current Limit:** Peak current that can be delivered to the output.

**Input Voltage:** The DC voltage applied to the input terminals with respect to ground.

**Input Output Differential:** The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation:** The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation:** The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability:** Output voltage stability under accelerated life–test conditions after 1000 hours with maximum rated voltage and junction temperature.

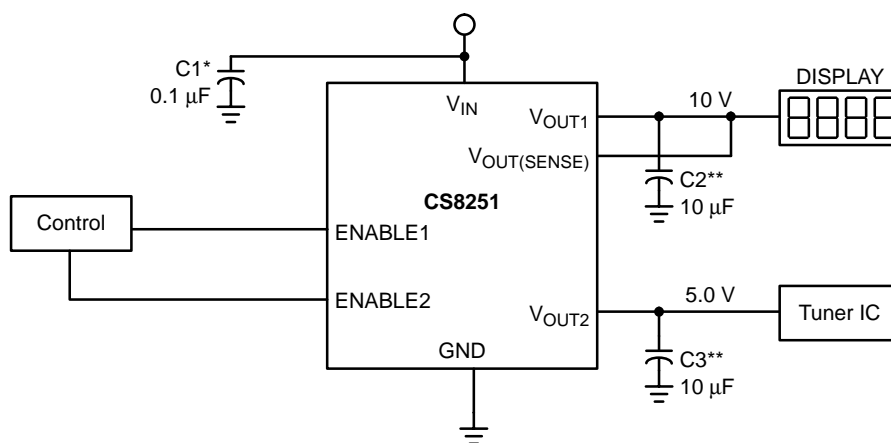
**Output Noise Voltage:** The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current:** The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

**Ripple Rejection:** The ratio of the peak–to–peak input ripple voltage to the peak–to–peak output ripple voltage.

**Temperature Stability of V<sub>OUT</sub>:** The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

## CS8251



\*C1 required if regulator is located far from power source filter.

\*\*C2 and C3 required for stability.

**Figure 3. Applications Circuit**

### APPLICATION NOTES

With separate control of each output channel, the CS8251 is ideal for applications where each load must be switched independently. In an automotive radio, the 10 V output drives the displays and tape drive motors while the 5.0 V output supplies the Tuner IC and memory.

#### Stability Considerations

The output or compensation capacitors determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor values and types should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures ( $-25^{\circ}\text{C}$  to  $-40^{\circ}\text{C}$ ), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

To determine acceptable values for the compensation capacitors in a particular application, start with tantalum capacitors of the recommended value and work towards a less expensive alternative part on each output in turn.

**Step 1:** Place the completed circuit with tantalum capacitors of the recommended values in an environmental chamber at the lowest specified operating temperature and monitor the outputs on the oscilloscope. A decade box connected in series with one of the capacitors C2 or C3 will simulate the higher ESR of an aluminum capacitor. (Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible)

**Step 2:** With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations

are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

**Step 3:** Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

**Step 4:** Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

**Step 5:** If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the circuit oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

**Step 6:** Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.

**Step 7:** Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found for each output, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of  $\pm 20\%$  so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitors should be less than 50% of the maximum allowable ESR found in step 3 above.

Repeat steps 1 through 7 with the second output leaving a large tantalum on the first output for stability.

**Calculating Power Dissipation in a Dual Output Linear Regulator**

The maximum power dissipation for a dual output regulator (Figure 4) is

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT1(min)}\}I_{OUT1(max)} + \{V_{IN(max)} - V_{OUT2(min)}\}I_{OUT2(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

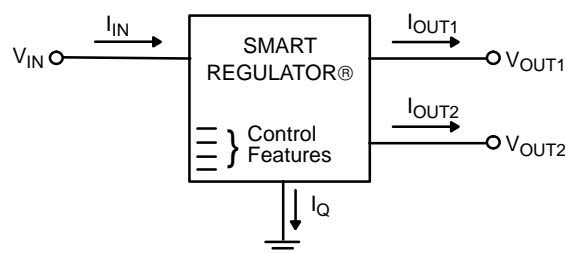
- $V_{IN(max)}$  is the maximum input voltage,
- $V_{OUT1(min)}$  is the minimum output voltage from  $V_{OUT1}$ ,
- $V_{OUT2(min)}$  is the minimum output voltage from  $V_{OUT2}$ ,
- $I_{OUT1(max)}$  is the maximum output current, for the application,
- $I_{OUT2(max)}$  is the maximum output current, for the application,
- $I_Q$  is the quiescent current the regulator consumes at  $I_{OUT(max)}$ .

Once the value of  $P_{D(max)}$  is known, the maximum permissible value of  $R_{\theta JA}$  can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}C - T_A}{P_D} \quad (2)$$

The value of  $R_{\theta JA}$  can then be compared with those in the package section of the data sheet. Those packages with  $R_{\theta JA}$ 's less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.



**Figure 4. Dual Output Regulator with Key Performance Parameters Labeled**

**Heat Sinks**

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of  $R_{\theta JA}$ .

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

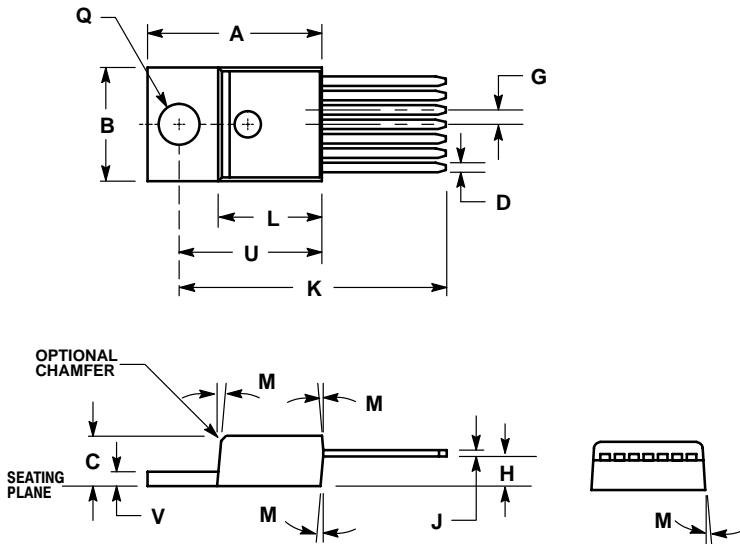
- $R_{\theta JC}$  = the junction-to-case thermal resistance,
- $R_{\theta CS}$  = the case-to-heatsink thermal resistance, and
- $R_{\theta SA}$  = the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$  appears in the package section of the data sheet. Like  $R_{\theta JA}$ , it too is a function of package type.  $R_{\theta CS}$  and  $R_{\theta SA}$  are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

# CS8251

## PACKAGE DIMENSIONS

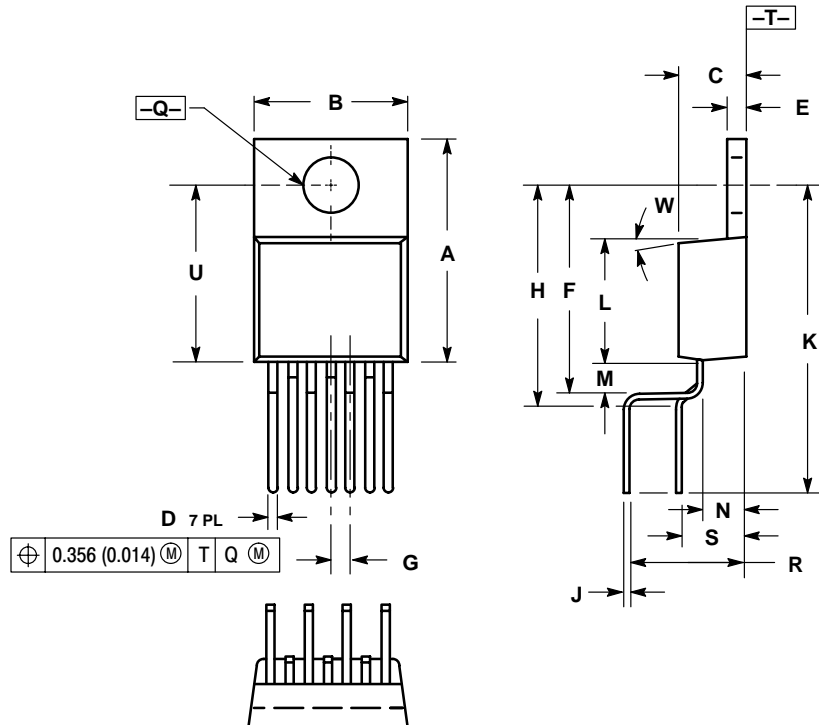
TO-220  
SEVEN LEAD  
T SUFFIX  
CASE 821E-04  
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.600	0.610	15.24	15.49
B	0.386	0.403	9.80	10.23
C	0.170	0.180	4.32	4.56
D	0.028	0.037	0.71	0.94
G	0.045	0.055	1.15	1.39
H	0.088	0.102	2.24	2.59
J	0.018	0.026	0.46	0.66
K	1.028	1.042	26.11	26.47
L	0.355	0.365	9.02	9.27
M	5° NOM		5° NOM	
Q	0.142	0.148	3.61	3.75
U	0.490	0.501	12.45	12.72
V	0.045	0.055	1.15	1.39

TO-220  
SEVEN LEAD  
TVA SUFFIX  
CASE 821J-02  
ISSUE A

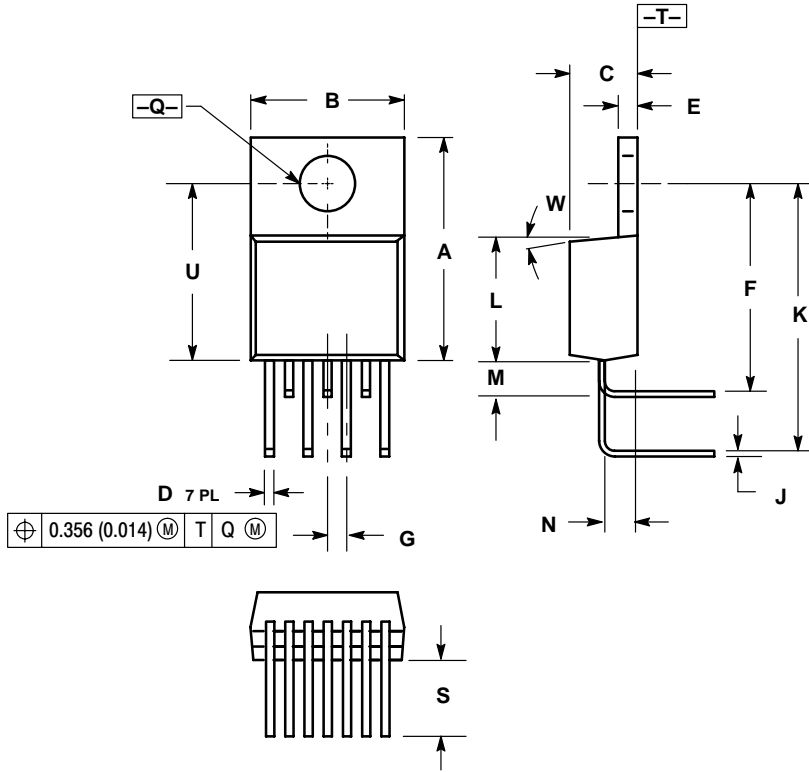


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  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.540	0.555	13.72	14.10
G	0.050 BSC		1.27 BSC	
H	0.570	0.595	14.48	15.11
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.322	0.337	8.18	8.56
M	0.073	0.088	1.85	2.24
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
R	0.289	0.304	7.34	7.72
S	0.164	0.179	4.17	4.55
U	0.460	0.475	11.68	12.07
W	3°		3°	

# CS8251

## TO-220 SEVEN LEAD THA SUFFIX CASE 821H-02 ISSUE A



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
1. LEADS MAINTAIN A RIGHT ANGLE WITH RESPECT TO THE PACKAGE BODY TO WITH  $\pm 0.020^\circ$ .

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.568	0.583	14.43	14.81
G	0.050 BSC		1.27 BSC	
J	0.015	0.022	0.38	0.56
K	0.728	0.743	18.49	18.87
L	0.322	0.337	8.18	8.56
M	0.101	0.116	2.57	2.95
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
S	0.150	0.200	3.81	5.08
U	0.460	0.475	11.68	12.07
W	3°		3°	

**PACKAGE THERMAL DATA**

Parameter		TO-220 7 LEAD	Unit
R <sub>θJC</sub>	Typical	3.5	°C/W
R <sub>θJA</sub>	Typical	50	°C/W



# Notes

# Notes

# Notes

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