Low-Voltage CMOS Octal Transceiver

With 5V–Tolerant Inputs and Outputs (3–State, Non–Inverting)

The MC74LCX2245 is a high performance, non–inverting octal transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX2245 inputs to be safely driven from 5V devices. The MC74LCX2245 is designed to reduce output overshoot and undershoot and is suitable for memory address driving and all TTL level bus oriented transceiver applications; especially those requiring the very quiet outputs.

Current drive capability is 12mA at both A and B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow through the bi–directional transceiver. Transmit (active–HIGH) enables data from A ports to B ports; Receive (active–LOW) enables data from B to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 12mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

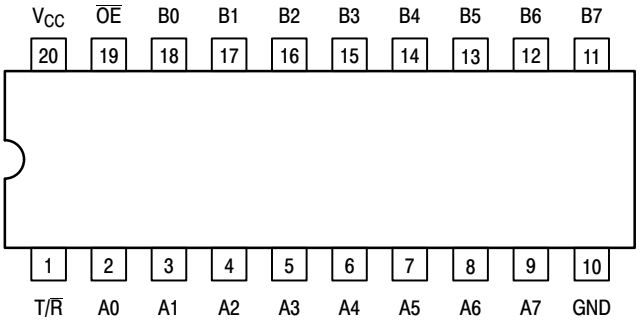


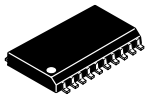
Figure 1. 20–Lead Pinout
(Top View)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

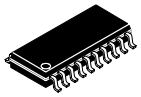
MC74LCX2245

LCX

LOW–VOLTAGE CMOS OCTAL TRANSCEIVER



DW SUFFIX
20–LEAD PLASTIC SOIC
CASE 751D–05



M SUFFIX
20–LEAD PLASTIC SOIC EIAJ
CASE 967–01

DT SUFFIX
20–LEAD PLASTIC TSSOP
CASE 948E–02

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A0–A7	Side A 3–State Inputs or 3–State Outputs
B0–B7	Side B 3–State Inputs or 3–State Outputs

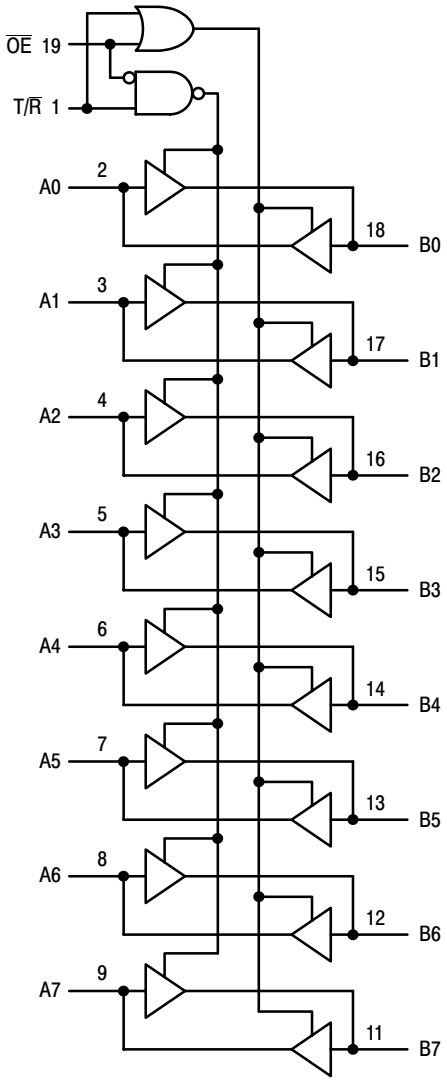


Figure 2. Logic Diagram

INPUTS		OPERATING MODE Non–Inverting
$\overline{OE}$	T/$\overline{R}$	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$–0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$–0.5 \le V_O \le +7.0$	Output in 3–State	V
		$–0.5 \le V_O \le V_{CC} + 0.5$	Note 1.	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage — Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage — (HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V			–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V			12	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7V – 3.0V			–8	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7V – 3.0V			8	mA
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	$2.7V \le V_{CC} \le 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2.)	$2.7V \le V_{CC} \le 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OH} = –100µA	V_{CC} – 0.2		V
		V_{CC} = 2.7V; I_{OH} = –4mA	2.2		
		V_{CC} = 2.7V; I_{OH} = –8mA	2.0		
		V_{CC} = 3.0V; I_{OH} = –6mA	2.4		
		V_{CC} = 3.0V; I_{OH} = –12mA	2.0		

2. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{OL}	LOW Level Output Voltage	2.7V ≤ V_{CC} ≤ 3.6V; I_{OL} = 100μA		0.2	V
		V_{CC} = 2.7V; I_{OL}= 4mA		0.4	
		V_{CC} = 2.7V; I_{OL}= 8mA		0.6	
		V_{CC} = 3.0V; I_{OL} = 6mA		0.55	
		V_{CC} = 3.0V; I_{OL} = 12mA		0.8	
I_I	Input Leakage Current	2.7V ≤ V_{CC} ≤ 3.6V; 0V ≤ V_I ≤ 5.5V		±5.0	μA
I_{OZ}	3–State Output Current	2.7 ≤ V_{CC} ≤ 3.6V; 0V ≤ V_O ≤ 5.5V; V_I = V_{IH} or V_{IL}		±5.0	μA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0V; V_I or V_O = 5.5V		10	μA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6V; V_I = GND or V_{CC}		10	μA
		2.7 ≤ V_{CC} ≤ 3.6V; 3.6 ≤ V_I or V_O ≤ 5.5V		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6V; V_{IH} = V_{CC} – 0.6V		500	μA

AC CHARACTERISTICS (Note 3., t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits			Unit
			T_A = –40°C to +85°C			
			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V	
			Min	Max	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	10.0 10.0	11.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	11.5 11.5	12.5 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.5 7.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 4.)			1.0 1.0		ns

3. These AC parameters are preliminary and may be modified prior to release.
4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 5.)	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 5.)	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.8		V

5. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF

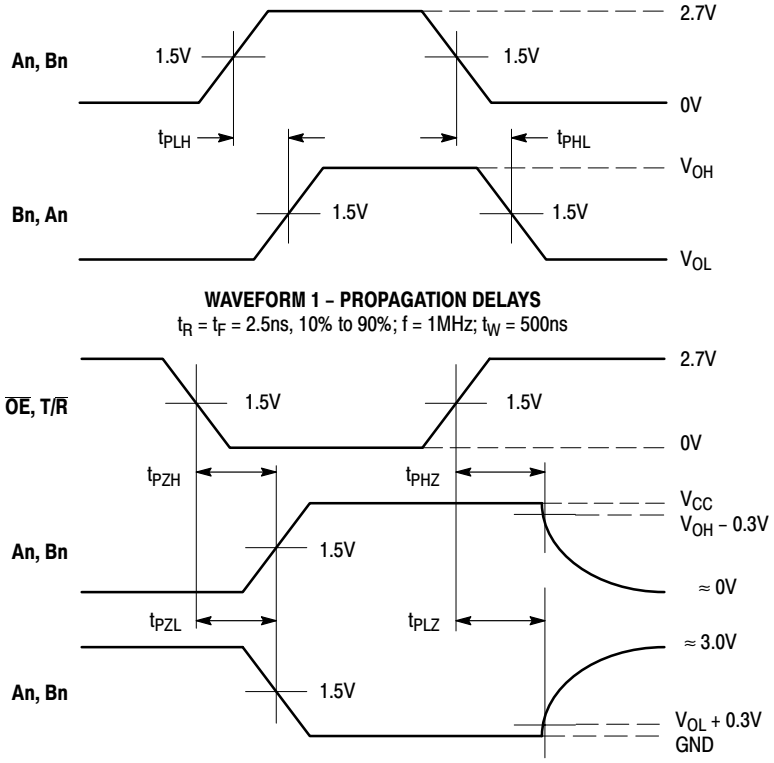
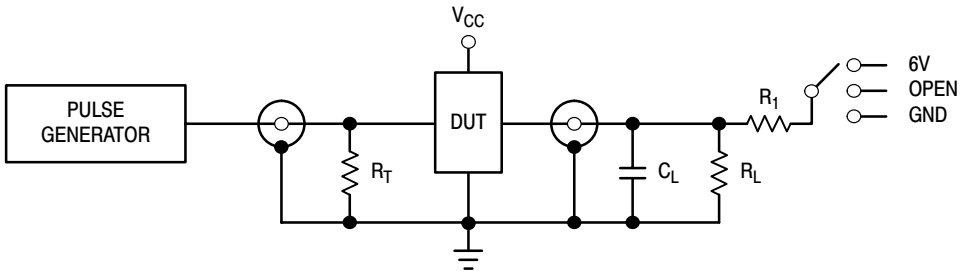


Figure 3. AC Waveforms



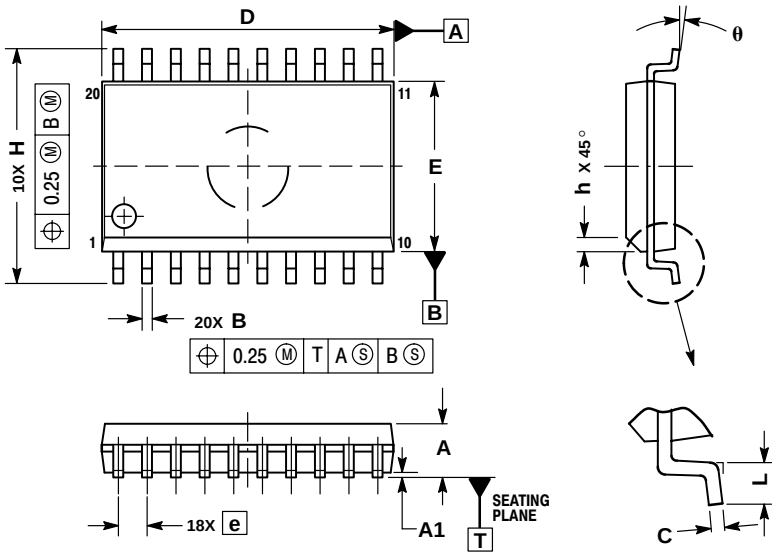
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 4. Test Circuit

OUTLINE DIMENSIONS

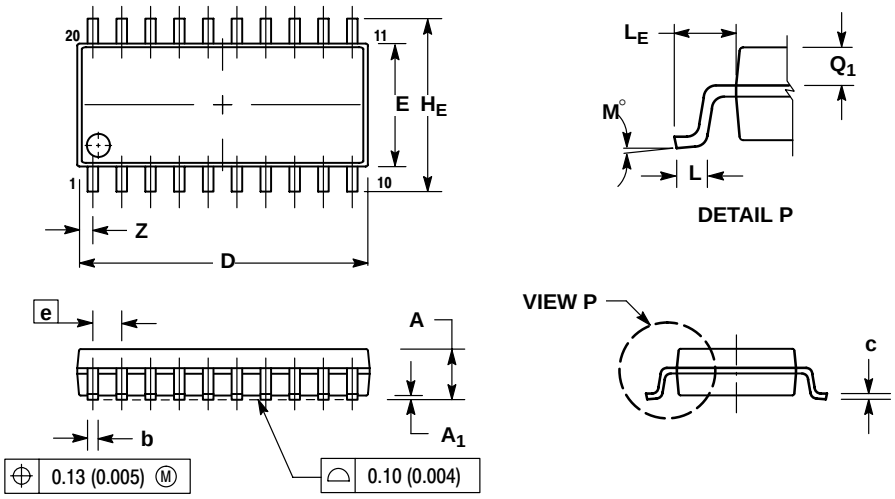
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE E



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 967–01
ISSUE O

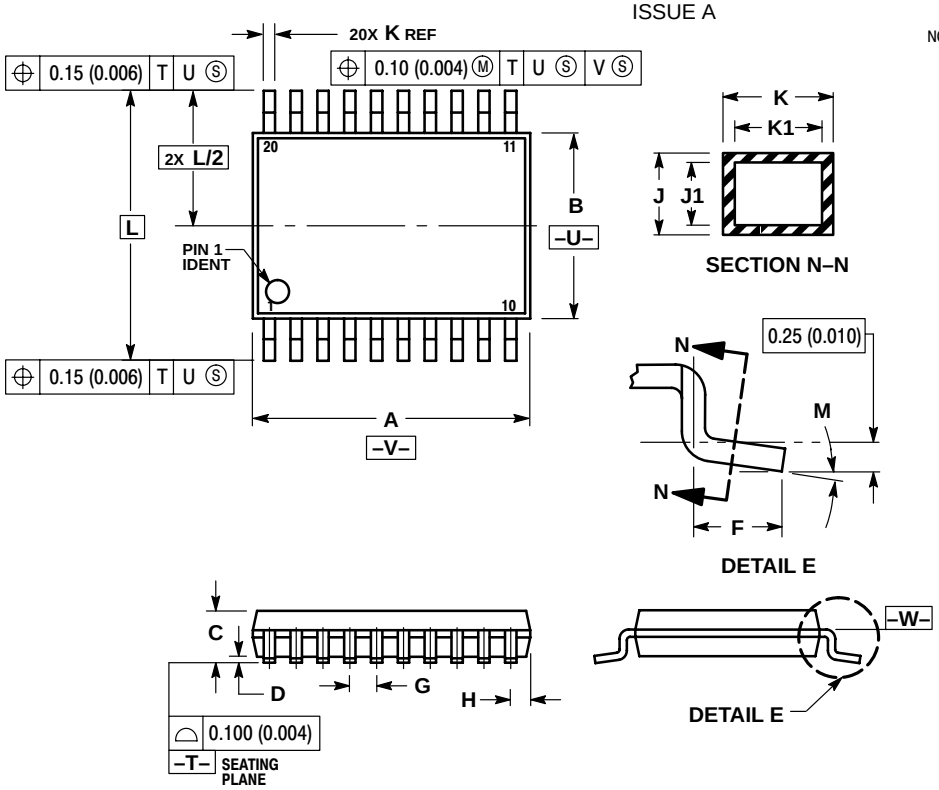


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303–675–2167 or 800–344–3810 Toll Free USA/Canada

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support
German Phone: (+1) 303–308–7140 (Mon–Fri 2:30pm to 7:00pm CET)
Email: ONlit–german@hibbertco.com
French Phone: (+1) 303–308–7141 (Mon–Fri 2:00pm to 7:00pm CET)
Email: ONlit–french@hibbertco.com
English Phone: (+1) 303–308–7142 (Mon–Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL–FREE ACCESS*: 00–800–4422–3781
*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:
Spanish Phone: 303–308–7143 (Mon–Fri 8:00am to 5:00pm MST)
Email: ONlit–spanish@hibbertco.com
Toll–Free from Mexico: Dial 01–800–288–2872 for Access – then Dial 866–297–9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001–800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.