High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

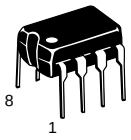
MC34080 thru MC34085

HIGH PERFORMANCE JFET INPUT OPERATIONAL AMPLIFIERS

These devices are a new generation of high speed JFET input monolithic operational amplifiers. Innovative design concepts along with JFET technology provide wide gain bandwidth product and high slew rate. Well–matched JFET input devices and advanced trim techniques ensure low input offset errors and bias currents. The all NPN output stage features large output voltage swing, no deadband crossover distortion, high capacitive drive capability, excellent phase and gain margins, low open loop output impedance, and symmetrical source/sink AC frequency response.

This series of devices is available in fully compensated or decompensated ($A_{VCL} \leq 2$) and is specified over a commercial temperature range. They are pin compatible with existing Industry standard operational amplifiers, and allow the designer to easily upgrade the performance of existing designs.

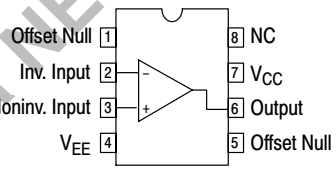
- Wide Gain Bandwidth: 8.0 MHz for Fully Compensated Devices
  16 MHz for Decompensated Devices
- High Slew Rate: 25 V/μs for Fully Compensated Devices
  50 V/μs for Decompensated Devices
- High Input Impedance: $10^{12}\Omega$
- Input Offset Voltage: 0.5 mV Maximum (Single Amplifier)
- Large Output Voltage Swing: –14.7 V to +14 V for
  $V_{CC}/V_{EE} = \pm 15$ V
- Low Open Loop Output Impedance: 30 Ω @ 1.0 MHz
- Low THD Distortion: 0.01%
- Excellent Phase/Gain Margins: 55°/7.6 dB for Fully Compensated Devices



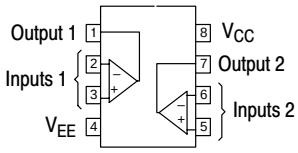
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



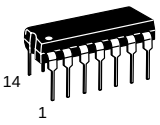
(Single, Top View)



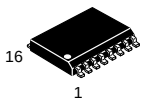
(Dual, Top View)

ORDERING INFORMATION

Op Amp Function	Fully Compensated	$A_{VCL} \geq 2$ Compensated	Operating Temperature Range	Package
Single	MC34081BD	MC34080BD	T_A = 0° to +70°C	SO–8
	MC34081BP	MC34080BP		Plastic DIP
Dual	MC34082P	MC34083BP		Plastic DIP
Quad	MC34084DW	MC34085BDW	T_A = 0° to +70°C	SO–16L
	MC34084P	MC34085BP		Plastic DIP

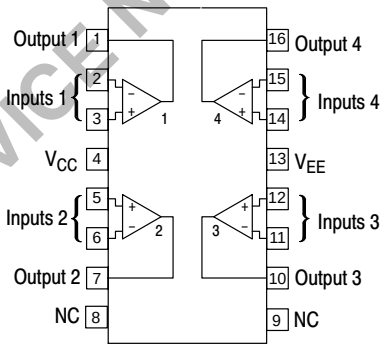


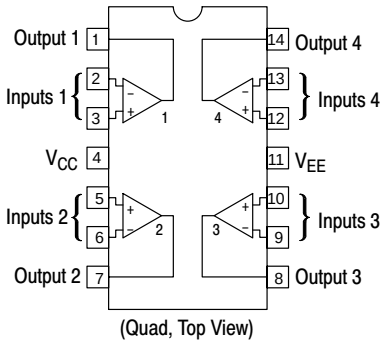
P SUFFIX
PLASTIC PACKAGE
CASE 646



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS





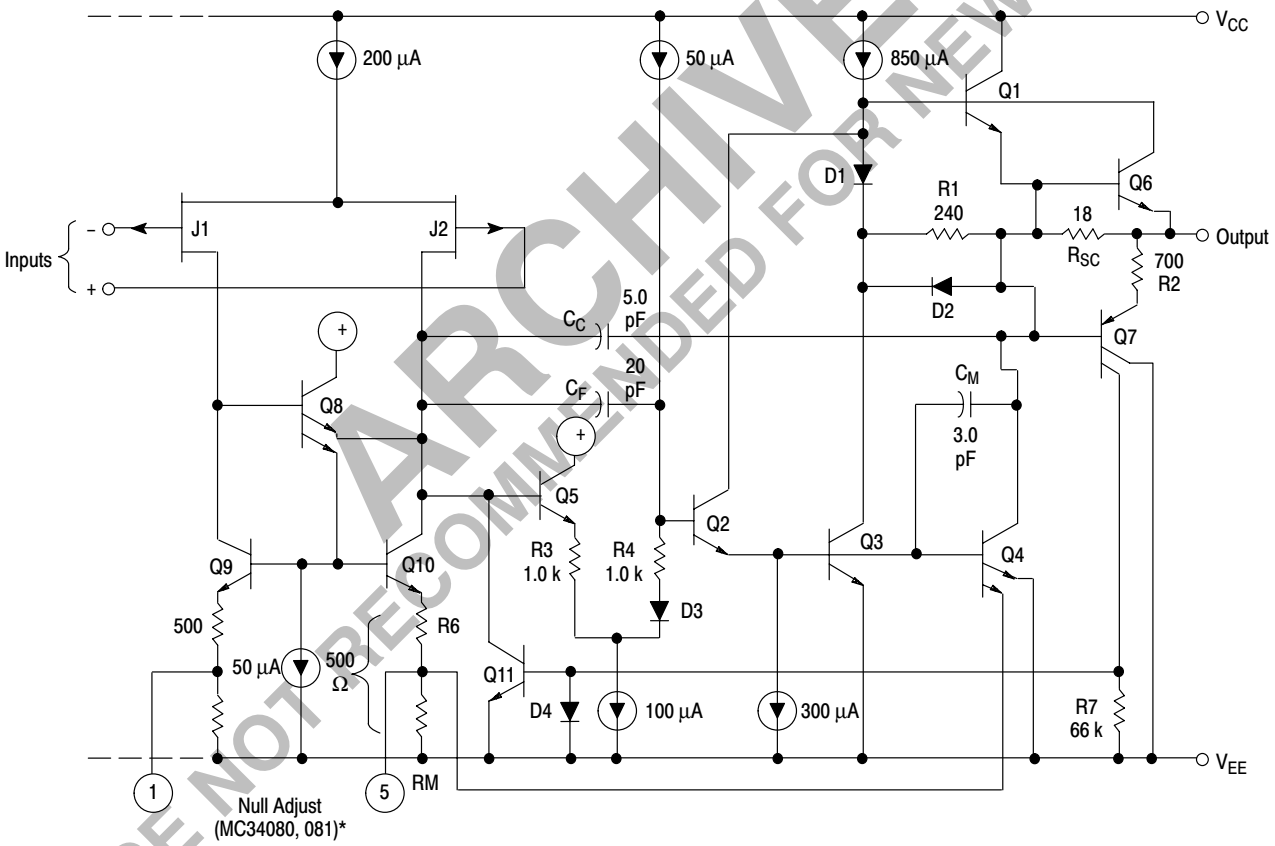
(Quad, Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	– 65 to +165	°C

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Representative Schematic Diagram
(Each Amplifier)



*Pins 1 & 5 (MC34080,081) should *not* be directly grounded or connected to V_{CC}.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (Note 4)	V_{IO}				mV
Single					
T_A = +25°C		—	0.5	2.0	
T_A = 0° to +70°C (MC34080B, MC34081B)		—	—	4.0	
Dual					
T_A = +25°C		—	1.0	3.0	
T_A = 0° to +70°C (MC34082, MC34083)		—	—	5.0	
Quad					
T_A = +25°C		—	6.0	12	
T_A = 0° to +70°C (MC34084, MC34085)		—	—	14	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0 Note 5)	I_{IB}				
T_A = +25°C		—	0.06	0.2	nA
T_A = 0° to +70°C		—	—	4.0	
Input Offset Current (V_{CM} = 0 Note 5)	I_{IO}				
T_A = +25°C		—	0.02	0.1	nA
T_A = 0° to +70°C		—	—	2.0	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}				V/mV
T_A = +25°C		25	80	—	
T_A = T_{low} to T_{high}		15	—	—	
Output Voltage Swing	V_{OH}				V
R_L = 2.0 k, T_A = +25°C		13.2	13.7	—	
R_L = 10 k, T_A = +25°C		13.4	13.9	—	
R_L = 10 k, T_A = $T_{low\ to}$ T_{high}		13.4	—	—	
R_L = 2.0 k, T_A = +25°C	V_{OL}	—	–14.1	–13.5	
R_L = 10 k, T_A = +25°C		—	–14.7	–14.1	
R_L = 10 k, T_A = $T_{low\ to}$ T_{high}		—	—	–14.0	
Output Short Circuit Current (T_A = +25°C)	I_{SC}				mA
Input Overdrive = 1.0 V, Output to Ground					
Source		20	31	—	
Sink		20	28	—	
Input Common Mode Voltage Range	V_{ICR}	(V_{EE} +4.0) to (V_{CC} – 2.0)			V
T_A = +25°C					
Common Mode Rejection Ratio (R_S ≤ 10 k, T_A = +25°C)	CMRR	70	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω, T_A = 25°C)	PSRR	70	86	—	dB
Power Supply Current	I_D				mA
Single					
T_A = +25°C		—	2.5	3.4	
T_A = T_{low} to T_{high}		—	—	4.2	
Dual					
T_A = +25°C		—	4.9	6.0	
T_A = T_{low} to T_{high}		—	—	7.5	
Quad					
T_A = +25°C		—	9.7	11	
T_A = T_{low} to T_{high}		—	—	13	

NOTES: (continued)

3. T_{low} = 0°C for MC34080B, MC34081B, MC34084, MC34085 T_{high} = +70°C for MC34080B, MC34081B, MC34084, MC34085
4. See application information for typical changes in input offset voltage due to solderability and temperature cycling.
5. Limits at T_A = +25°C are guaranteed by high temperature (T_{high}) testing.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF)	SR				V/μs
Compensated A_V = +1.0		20	25	—	
A_V = –1.0		—	30	—	
Decompensated A_V = +2.0		35	50	—	
A_V = –1.0		—	50	—	
Settling Time (10 V Step, A_V = –1.0)	t_s				μs
To 0.10% ($\pm 1/2$ LSB of 9–Bits)		—	0.72	—	
To 0.01% ($\pm 1/2$ LSB of 12–Bits)		—	1.6	—	
Gain Bandwidth Product (f = 200 kHz)	GBW				MHz
Compensated		6.0	8.0	—	
Decompensated		12	16	—	
Power Bandwidth (R_L = 2.0 k, V_O = 20 V_{pp}, THD = 5.0%)	BWp				kHz
Compensated A_V = +1.0		—	400	—	
Decompensated A_V = – 1.0		—	800	—	
Phase Margin (Compensated)	ϕ_m				De-grees
R_L = 2.0 k		—	55	—	
R_L = 2.0 k, C_L = 100 pF		—	39	—	
Gain Margin (Compensated)	A_m				dB
R_L = 2.0 k		—	7.6	—	
R_L = 2.0 k, C_L = 100 pF		—	4.5	—	
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	30	—	nV/$\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.01	—	pA/$\sqrt{Hz}$
Input Capacitance	C_i	—	5.0	—	pF
Input Resistance	r_i	—	10^{12}	—	Ω
Total Harmonic Distortion A_V = +10, R_L = 2.0 k, 2.0 ≤ V_O ≤ 20 V_{pp}, f = 10 kHz	THD	—	0.05	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	dB
Open Loop Output Impedance (f = 1.0 MHz)	Z_o	—	35	—	Ω

Figure 1. Input Common Mode Voltage Range versus Temperature

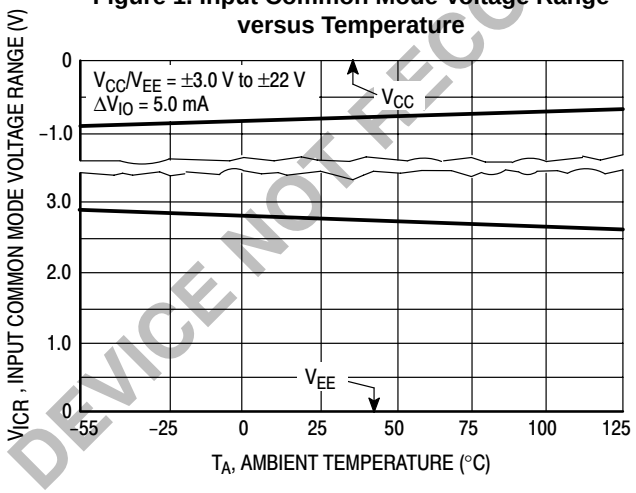


Figure 2. Input Bias Current versus Temperature

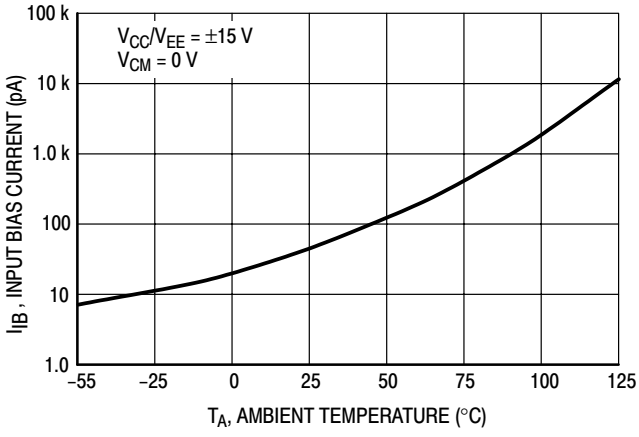


Figure 3. Input Bias Current versus Input Common Mode Voltage

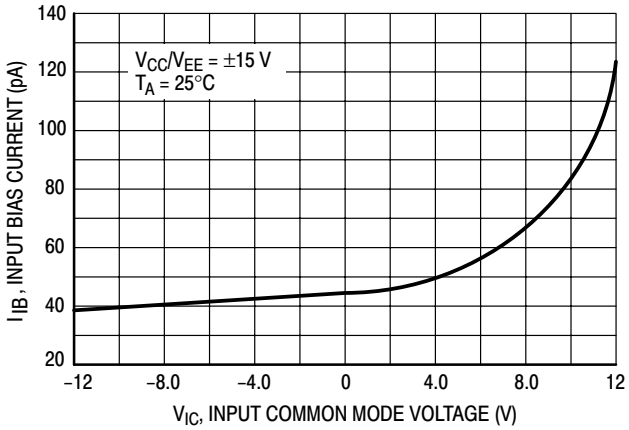


Figure 4. Output Voltage Swing versus Supply Voltage

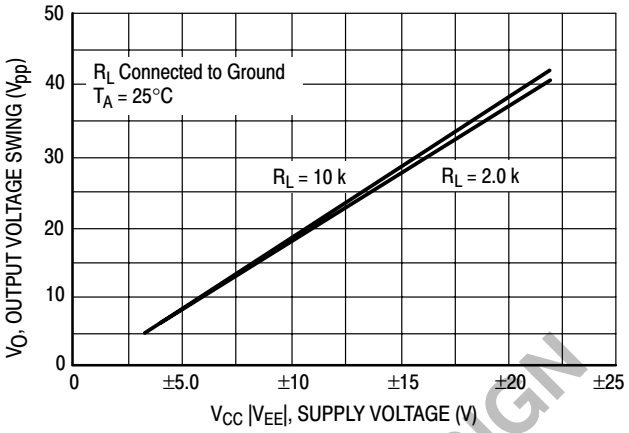


Figure 5. Output Saturation versus Load Current

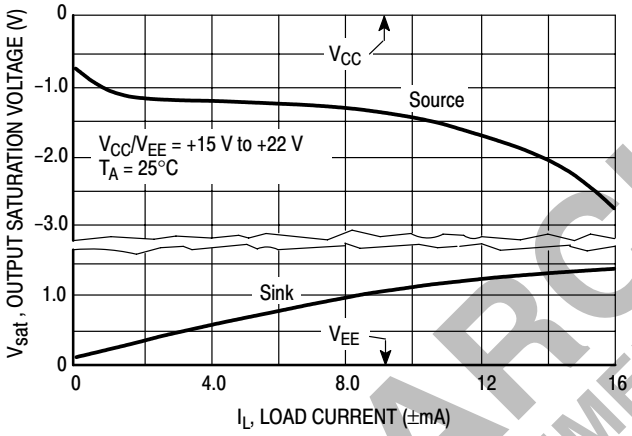


Figure 6. Output Saturation vesus Load Resistance to Ground

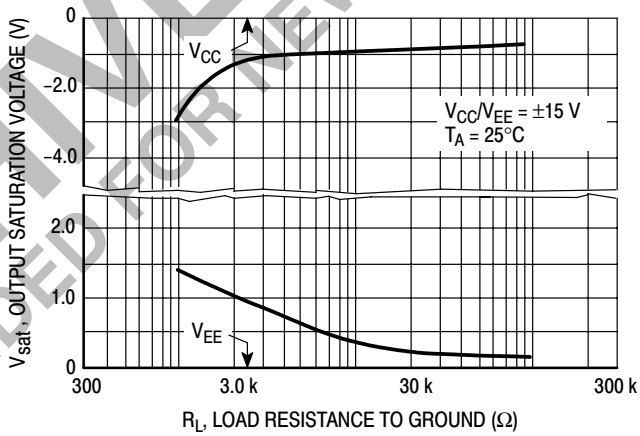


Figure 7. Output Saturation versus Load Resistance to V_{CC}

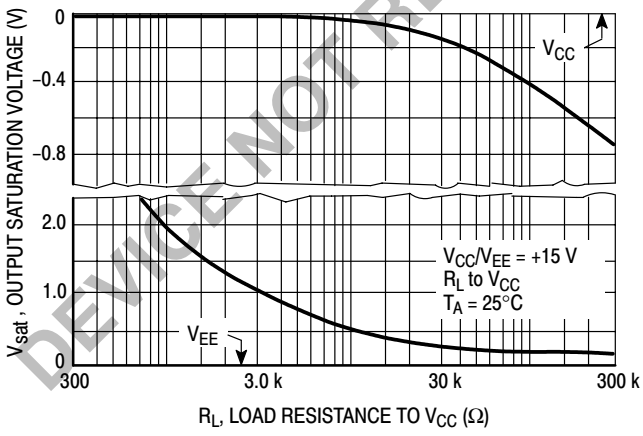


Figure 8. Output Short Circuit Current versus Temperature

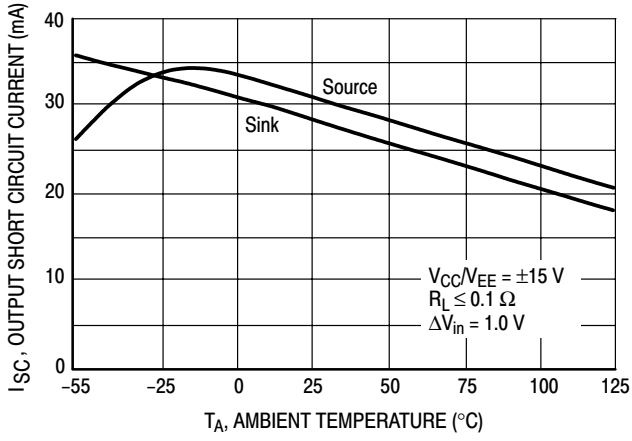


Figure 9. Output Impedance versus Frequency

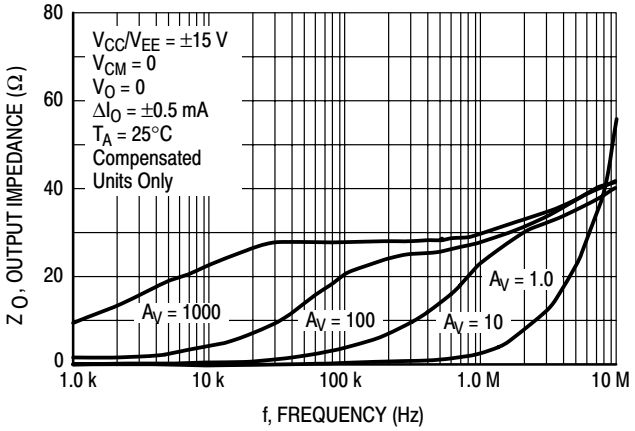


Figure 10. Output Impedance versus Frequency

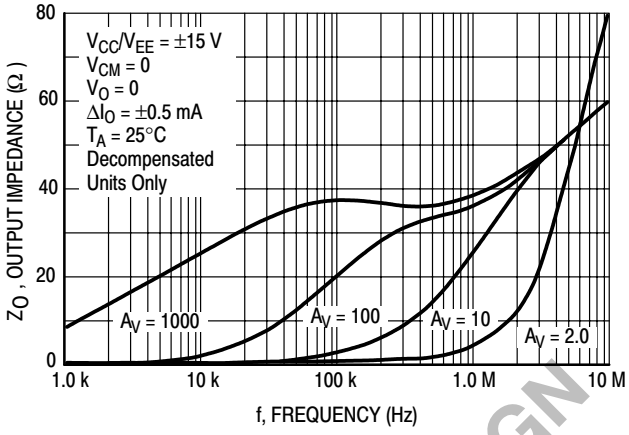


Figure 11. Output Voltage Swing versus Frequency

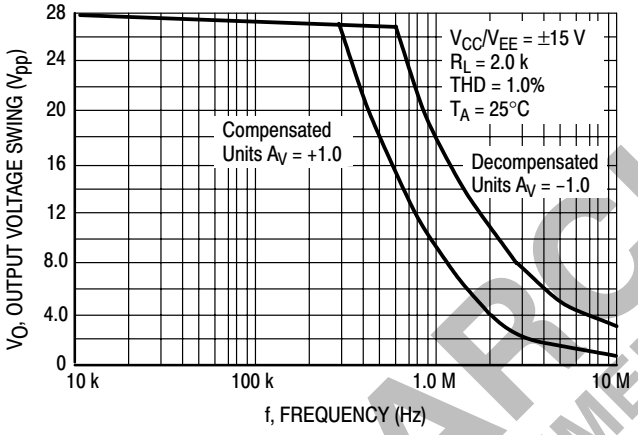


Figure 12. Output Distortion versus Frequency

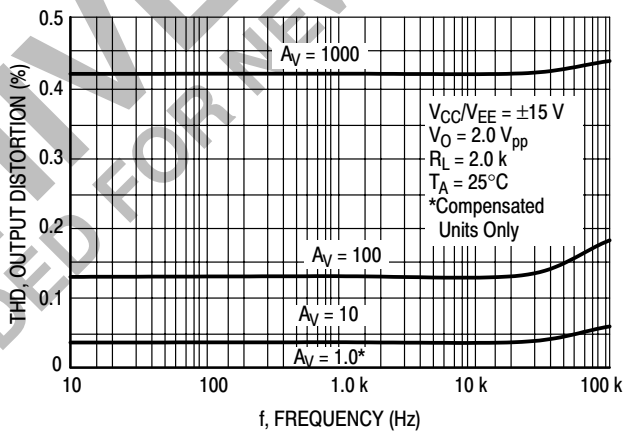


Figure 13. Open Loop Voltage Gain versus Temperature

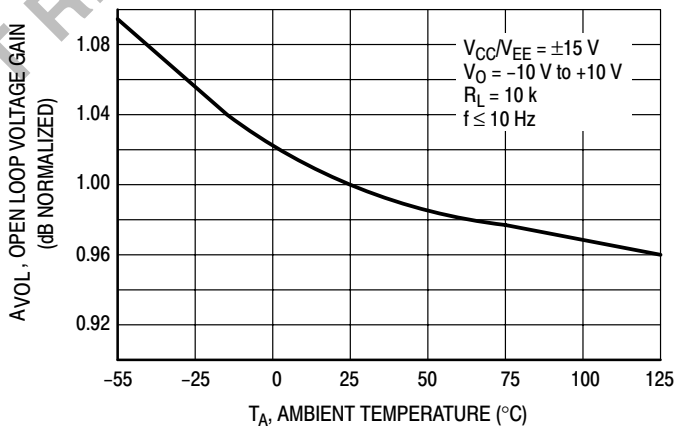


Figure 14. Open Loop Voltage Gain and Phase versus Frequency

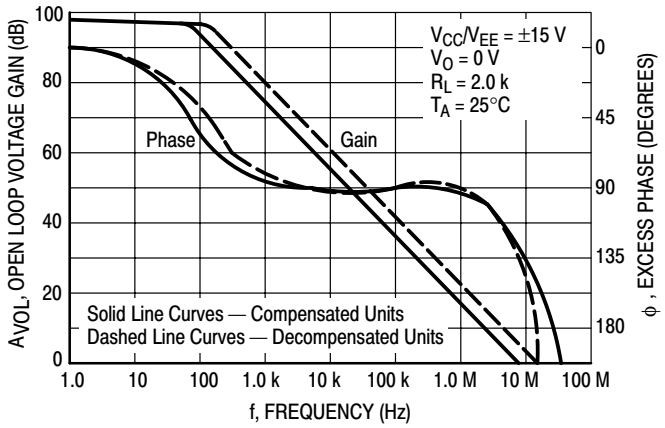


Figure 15. Open Loop Voltage Gain and Phase versus Frequency

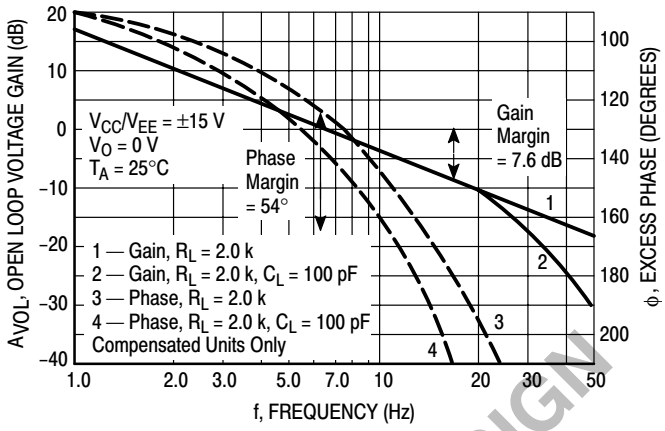


Figure 16. Open Loop Voltage Gain and Phase versus Frequency

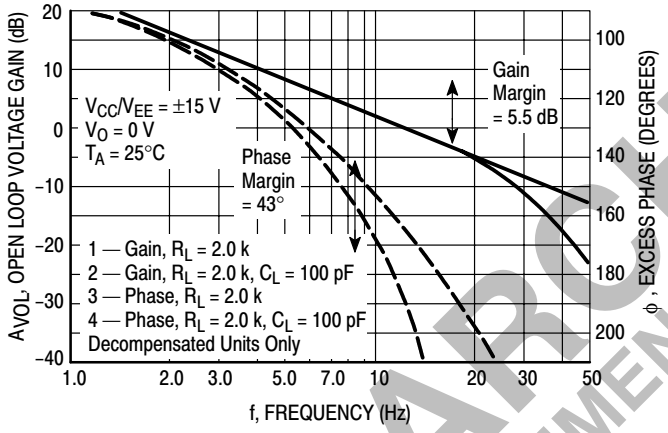


Figure 17. Normalized Gain Bandwidth Product versus Temperature

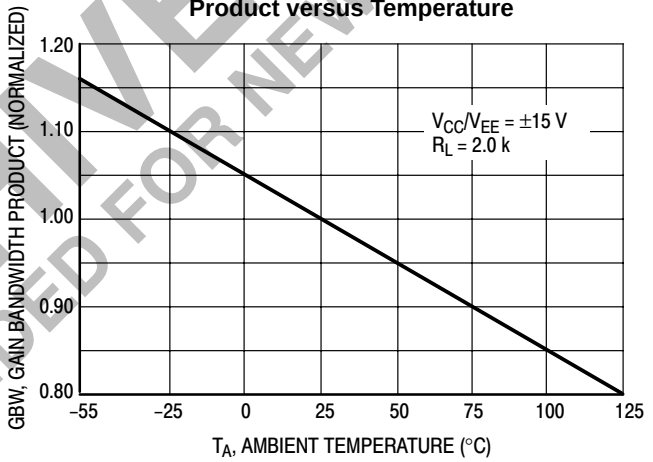


Figure 18. Percent Overshoot versus Load Capacitance

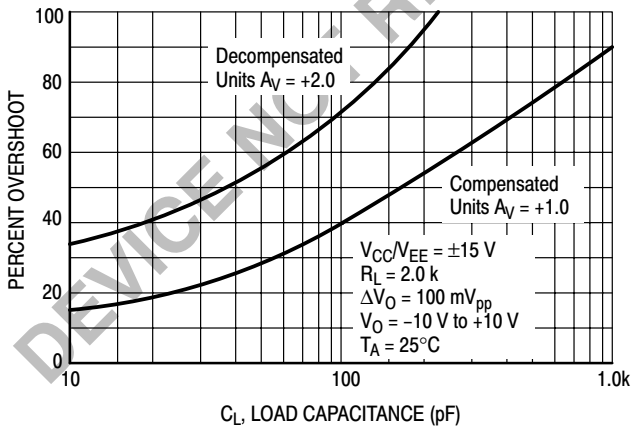


Figure 19. Phase Margin versus Load Capacitance

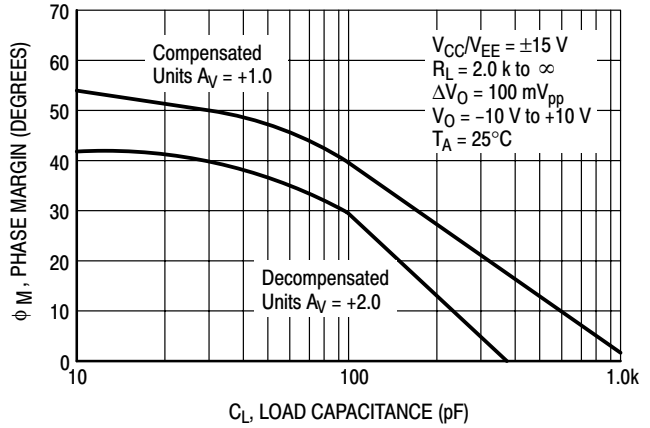


Figure 20. Gain Margin versus Load Capacitance

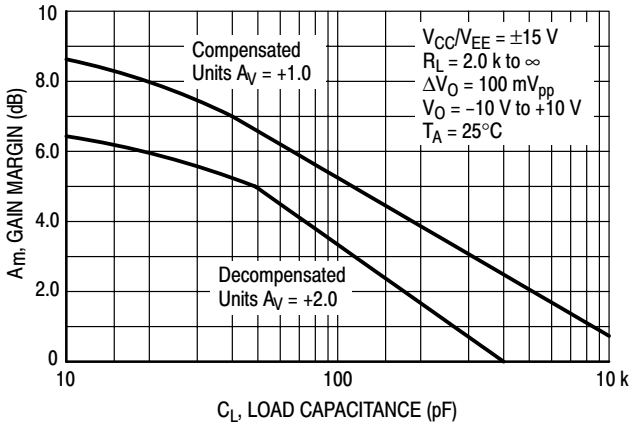


Figure 21. Phase Margin versus Temperature

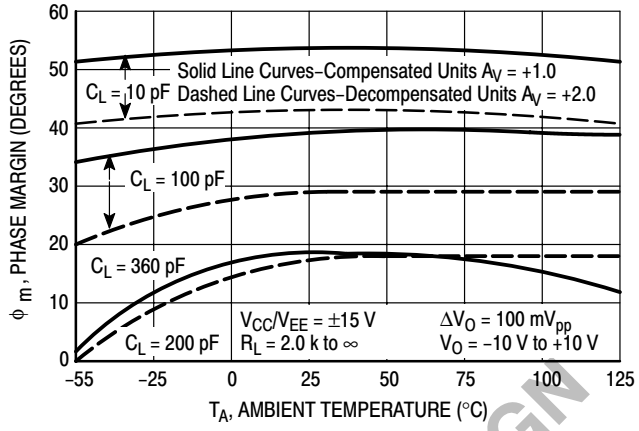


Figure 22. Gain Margin versus Temperature

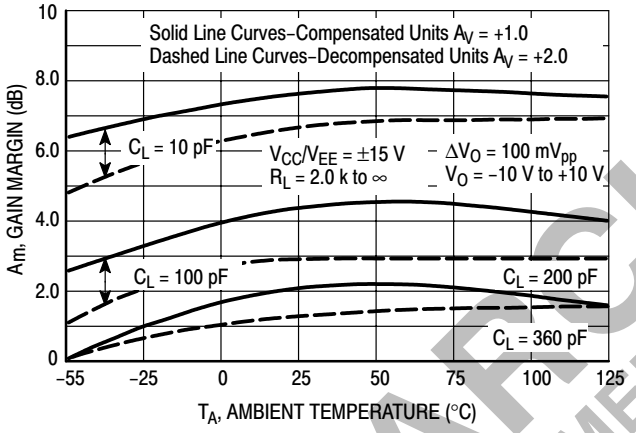
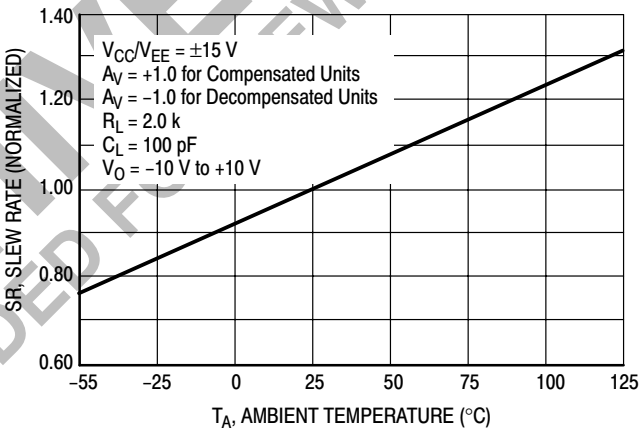


Figure 23. Normalized Slew Rate versus Temperature



MC34084 Transient Response

A_V = +1.0, R_L = 2.0 k, V_{CC}/V_{EE} = ±15 V, T_A = 25°C

Figure 24. Small Signal

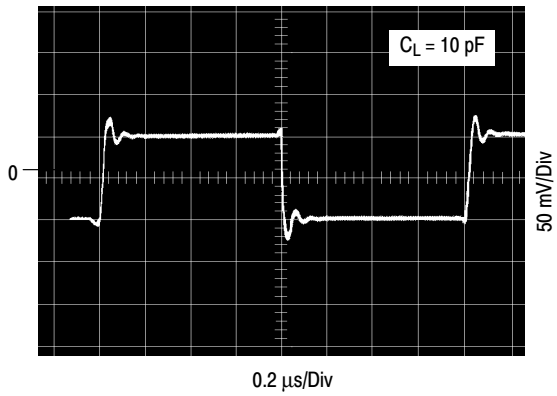
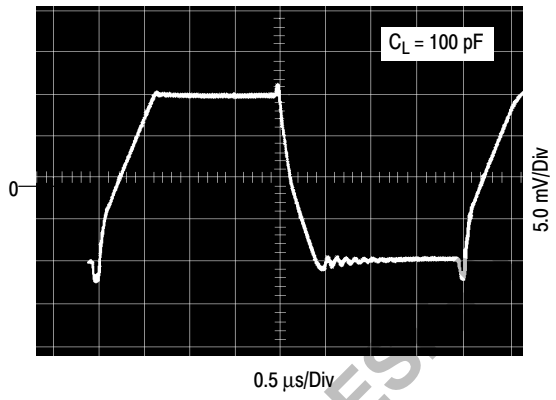


Figure 25. Large Signal



MC34085 Transient Response

A_V = +2.0, R_L = 2.0 k, V_{CC}/V_{EE} = ±15 V, T_A = 25°C

Figure 26. Small Signal

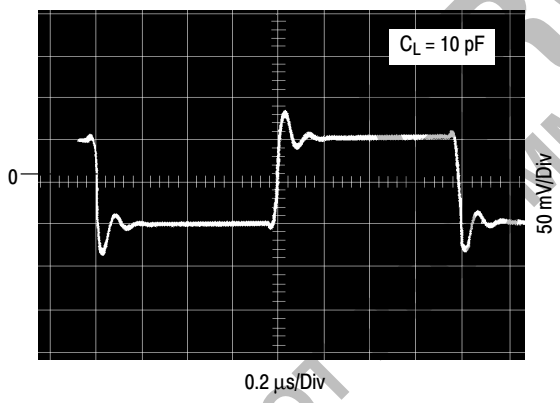


Figure 27. Large Signal

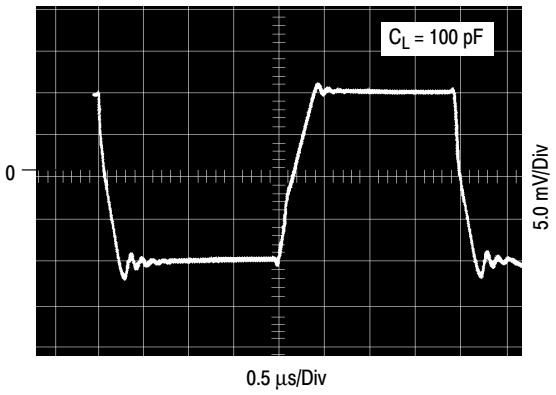


Figure 28. Common Mode Rejection Ratio versus Frequency

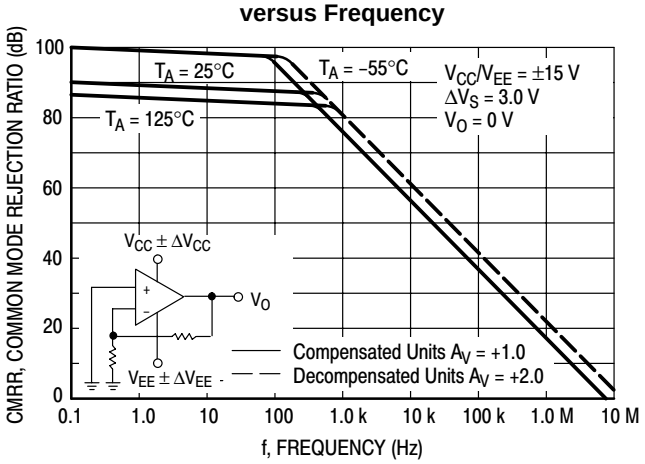


Figure 29. Power Supply Rejection Ratio versus Frequency

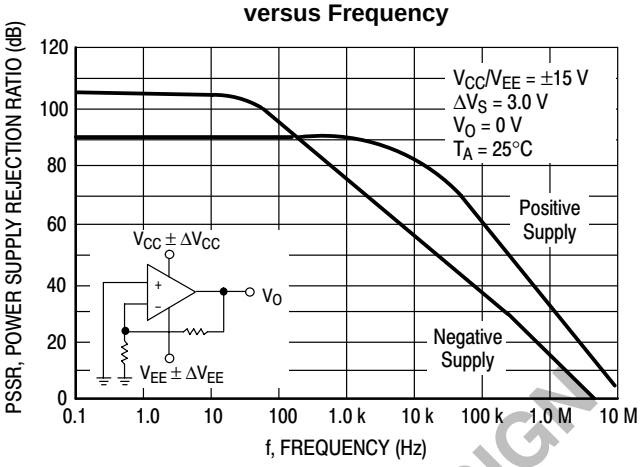


Figure 30. Power Supply Rejection Ratio versus Temperature

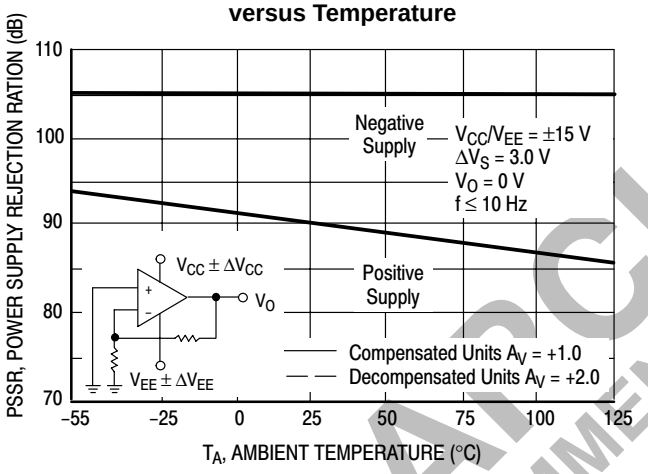


Figure 31. Normalized Supply Current versus Supply Voltage

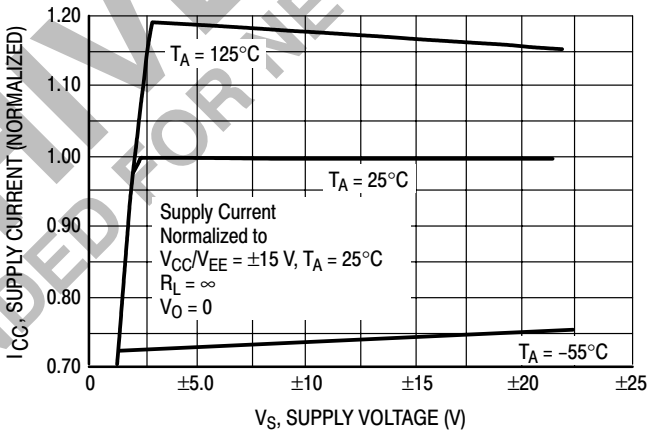


Figure 32. Channel Separation versus Frequency

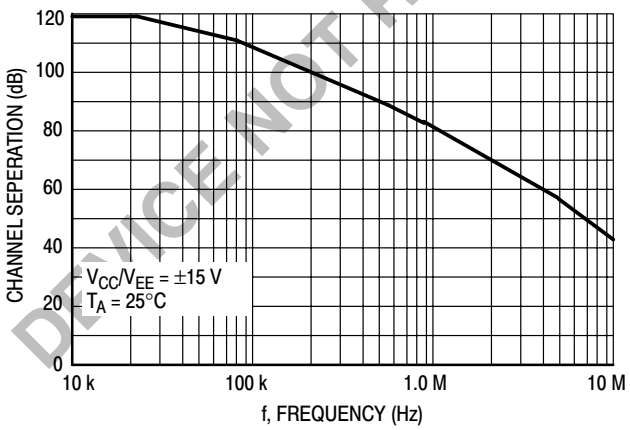
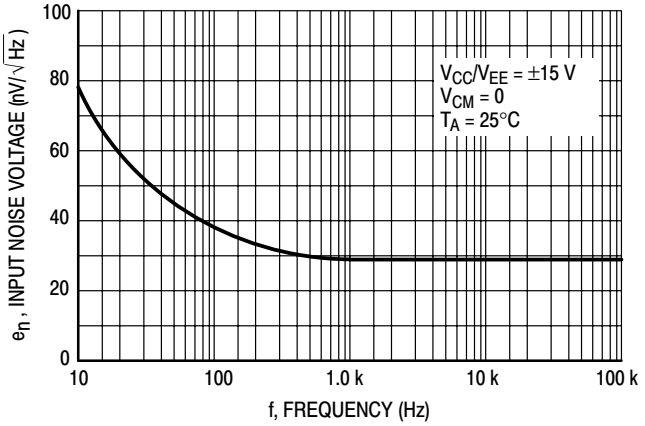


Figure 33. Spectral Noise Density



APPLICATIONS INFORMATION

The bandwidth and slew rate of the MC34080 series is nearly double that of currently available general purpose JFET op–amps. This improvement in AC performance is due to the P–channel JFET differential input stage driving a compensated miller integration amplifier in conjunction with an all NPN output stage.

The all NPN output stage offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. With a 10 k load resistance, the op amp can typically swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 p–p swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages. If the load resistance is referenced to V_{CC} instead of ground, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the NPN output transistor will pull the output very near V_{EE} during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull–up capability.

The all NPN transistor output stage is also inherently fast, contributing to the operation amplifier's high gain–bandwidth product and fast settling time. The associated high frequency output impedance is 50 Ω (typical) at 8.0 MHz. This allows driving capacitive loads from 0 pF to 300 pF without oscillations over the military temperature range, and over the full range of output swing. The 55°C phase margin and 7.6 dB gain margin as well as the general gain and phase characteristics are virtually independent of the sink/source output swing conditions. The high frequency characteristics of the MC34080 series is especially useful for active filter applications.

The common mode input range is from 2.0 V below the positive rail (V_{CC}) to 4.0 V above the negative rail (V_{EE}). The amplifier remains active if the inputs are biased at the positive rail. This may be useful for some applications in that single supply operation is possible with a single negative supply. However, a degradation of offset voltage and voltage gain may result.

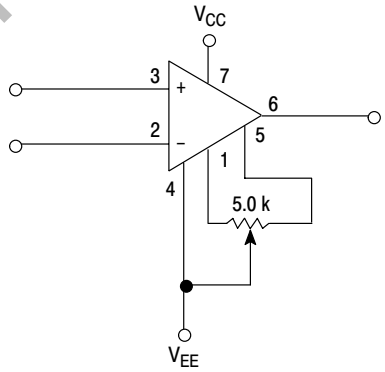
Phase reversal does not occur if either the inverting or noninverting input (or both) exceeds the positive common mode limit. If either input (or both) exceeds the negative common mode limit, the output will be in the high state. The input stage also allows a differential up to ±44 V, provided the maximum input voltage range is not exceeded. The supply voltage operating range is from ±5.0 V to ±22 V.

For optimum frequency performance and stability, careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input–output coupling. In order to reduce the input capacitance, resistors connected to the input pins should be physically close to these pins. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pickup" at this node.

Supply decoupling with adequate capacitance close to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit large impedance changes over temperature.

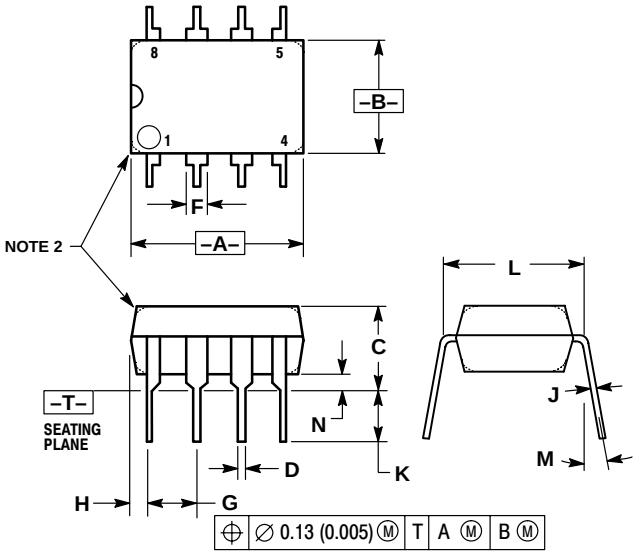
Primarily due to the JFET inputs of the op amp, the input offset voltage may change due to temperature cycling and board soldering. After 20 temperature cycles (– 55° to 165°C), the typical standard deviation for input offset voltage is 559 μV in the plastic packages. With respect to board soldering (260°C, 10 seconds), the typical standard deviation for input offset voltage is 525 μV in the plastic package. Socketed devices should be used over a minimal temperature range for optimum input offset voltage performance.

Figure 34. Offset Nulling Circuit



OUTLINE DIMENSIONS

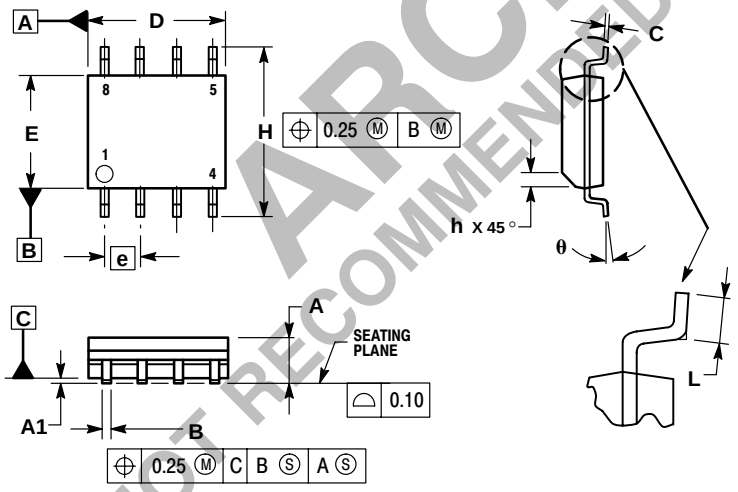
P SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10 °	---	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE R

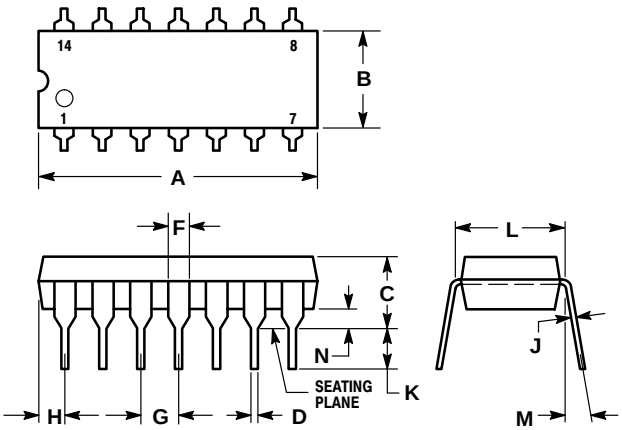


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0 °	7 °

OUTLINE DIMENSIONS

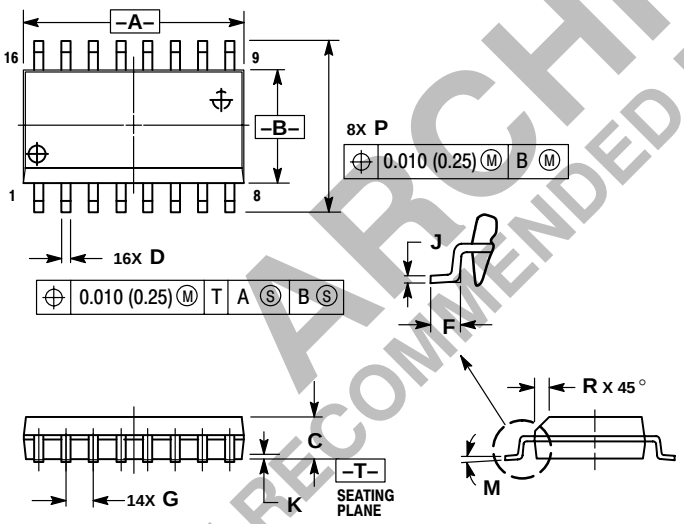
P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0 °	10°	0 °	10°
N	0.015	0.039	0.39	1.01

DW SUFFIX
PLASTIC PACKAGE
CASE 751G–02
(SO–16L)
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES

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