ANALOG DEVICES

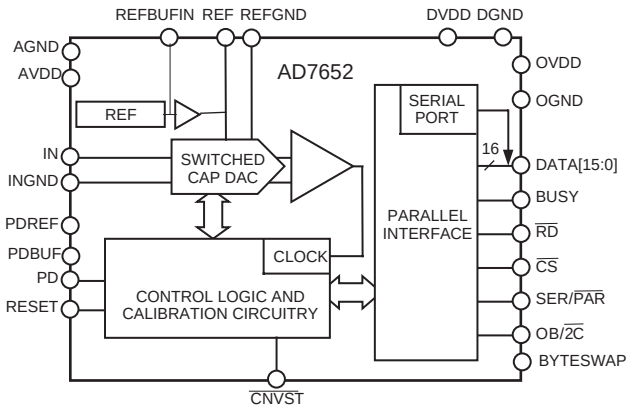
16-Bit 500 kSPS SAR Unipolar ADC with Ref

Preliminary Technical Data — AD7652*

FEATURES
Throughput: 500 kSPS
16 Bits Resolution
Analog Input Voltage Range: 0 V to 2.5 V
No Pipeline Delay
Parallel and Serial 5 V/3 V Interface
SPI™/QSPI™/MICROWIRE™/DSP Compatible
Single 5 V Supply Operation
Power Dissipation
67 mW Typ without REF, 15 μW @ 100 SPS
77 mW Typ with REF
Power-Down Mode: 7 μW Max
Package: 48-Lead Quad Flat Pack (LQFP);
48-Lead Chip Scale Package (LFCSP)
Pin-to-Pin Compatible with PulSAR ADCs

APPLICATIONS
Data Acquisition
Instrumentation
Digital Signal Processing
Spectrum Analysis
Medical Instruments
Battery-Powered Systems
Process Control

FUNCTIONAL BLOCK DIAGRAM



PulSAR Selection

Type / kSPS	100 - 250	500 - 570	1000
Pseudo Differential	AD7651 AD7660/61	AD7650/52 AD7664/66	AD7653 AD7667
True Bipolar	AD7663	AD7665	AD7671
True Differential	AD7675	AD7676	AD7677

GENERAL DESCRIPTION

The AD7652 is a 16-bit, 500 kSPS, charge redistribution SAR, analog-to-digital converter that operates from a single 5 V power supply. The part contains a high-speed 16-bit sampling ADC, an internal conversion clock, internal reference, error correction circuits, and both serial and parallel system interface ports.

It is fabricated using Analog Devices' high-performance, 0.6 micron CMOS process, with correspondingly low cost and is available in a 48-lead LQFP and a tiny 48-lead LFCSP with operation specified from –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Fast Throughput
   The AD7652 is a 500 kSPS, charge redistribution, 16-bit SAR ADC with internal error correction circuitry.
2. Internal Reference
   The AD7652 has an internal reference and allows for an external reference to be used.
3. Single-Supply Operation
   The AD7652 operates from a single 5 V supply and dissipates a typical of 67 mW. Its power dissipation decreases with throughput. It consumes 7 μW maximum when in power-down.
4. Serial or Parallel Interface
   Versatile parallel or 2-wire serial interface arrangement compatible with both 3 V or 5 V logic.

*Patent pending.
SPI and QSPI are trademarks of Motorola Inc.
MICROWIRE ia a trademark of National Semiconductor Corporation

REV. PrC

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AD7652–SPECIFICATIONS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN} - V_{INGND}$	0		V_{REF}	V
Operating Input Voltage	V_{IN}	–0.1		+3	V
	V_{INGND}	–0.1		+0.5	V
Analog Input CMRR	f_{IN} = 10 kHz		TBD		dB
Input Current	100 kSPS Throughput		TBD		µA
Input Impedance			See Analog Input Section		
THROUGHPUT SPEED					
Complete Cycle				1	µs
Throughput Rate		0		500	kSPS
DC ACCURACY					
Integral Linearity Error		–6		+6	LSB[1]
No Missing Codes		15			Bits
Transition Noise			TBD		LSB
Full-Scale Error[2]	REF = 2.5 V			±TBD	% of FSR
Unipolar Zero Error[2]			±TBD	±TBD	LSB
Power Supply Sensitivity	AVDD = 5 V ± 5%		±TBD		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 20 kHz		86		dB
Spurious Free Dynamic Range	f_{IN} = 20 kHz		98		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		-98		dB
	f_{IN} = 20 kHz		-96		dB
Signal-to-(Noise+Distortion)	f_{IN} = 20 kHz		86		dB
	–60 dB Input, f_{IN} = 10 kHz		30		dB
–3 dB Input Bandwidth			TBD		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			750	ns
REFERENCE					
Internal Reference Voltage	@ 25°C	TBD	2.5	TBD	V
Internal Reference Source Current			TBD		µA
Internal Reference Temp Drift	–40°C to +85°C		TBD		ppm/°C
Internal Reference Temp Drift	0°C to +70°C		TBD		ppm/°C
Turn-on Settling Time			TBD		
External Reference Voltage Range		2.3	2.5	AVDD – 1.85	V
External Reference Current Drain	500 kSPS Throughput		TBD		µA
Temperature Pin					
Voltage Output @ 25°C			313		mV
Temperature Sensitivity			1		mV/°C
Output Resistance			4.3		kΩ
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		2.0		DVDD + 0.3	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format			Parallel or Serial 16-Bits		
Pipeline Delay			Conversion Results Available Immediately after Completed Conversion		
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = –500 µA	OVDD – 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25[8]	V
Operating Current	500 kSPS Throughput				
AVDD			TBD		mA
DVDD[4]			TBD		mA
OVDD[4]			TBD		µA

Parameter	Conditions	Min	Typ	Max	Unit
Power Dissipation[5] without REF	500 kSPS Throughput		67		mW
	100 SPS Throughput[6]		15		µW
	In Power-Down Mode[7]			TBD	µW
Power Dissipation[5] with REF	500 kSPS Throughput		77		mW
TEMPERATURE RANGE[8]					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES
[1]LSB means Least Significant Bit. With the 0 V to 2.5 V input range, one LSB is 38.15 µV.
[2]See Definition of Specifications section. These specifications do not include the error contribution from the external reference.
[3]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.
[4]Tested in parallel reading mode using external reference.
[5]With external REF.
[6]With all digital inputs forced to DVDD or DGND respectively.
[7]Contact factory for extended temperature range.
[8]The max should be the minimum of 5.25V and DVDD+0.3 V.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

	Symbol	Min	Typ	Max	Unit
REFER TO FIGURES 11 AND 12					
Convert Pulsewidth	t_1	5			ns
Time Between Conversions	t_2	2			µs
$\overline{CNVST}$ LOW to BUSY HIGH Delay	t_3			30	ns
BUSY HIGH All Modes Except in Master Serial Read After Convert Mode	t_4			1.25	µs
Aperture Delay	t_5		2		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time	t_7			1.25	µs
Acquisition Time	t_8	750			ns
RESET Pulsewidth	t_9	10			ns
REFER TO FIGURES 13, 14, AND 15 (Parallel Interface Modes)					
$\overline{CNVST}$ LOW to DATA Valid Delay	t_{10}			1.25	µs
DATA Valid to BUSY LOW Delay	t_{11}	45			ns
Bus Access Request to DATA Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	5		15	ns
REFER TO FIGURES 16 AND 17 (Master Serial Interface Modes)[1]					
$\overline{CS}$ LOW to SYNC Valid Delay	t_{14}			10	ns
$\overline{CS}$ LOW to Internal SCLK Valid Delay[1]	t_{15}			10	ns
$\overline{CS}$ LOW to SDOUT Delay	t_{16}			10	ns
$\overline{CNVST}$ LOW to SYNC Delay	t_{17}		525		ns
SYNC Asserted to SCLK First Edge Delay	t_{18}	3			ns
Internal SCLK Period[2]	t_{19}	25		40	ns
Internal SCLK HIGH[2]	t_{20}	12			ns
Internal SCLK LOW[2]	t_{21}	7			ns
SDOUT Valid Setup Time[2]	t_{22}	4			ns
SDOUT Valid Hold Time[2]	t_{23}	2			ns
SCLK Last Edge to SYNC Delay[2]	t_{24}	3			
$\overline{CS}$ HIGH to SYNC HI-Z	t_{25}			10	ns
$\overline{CS}$ HIGH to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{CS}$ HIGH to SDOUT HI-Z	t_{27}			10	ns
BUSY HIGH in Master Serial Read after Convert[2]	t_{28}		See Table I		µs
$\overline{CNVST}$ LOW to SYNC Asserted Delay	t_{29}		1.25		µs
SYNC Deasserted to BUSY LOW Delay	t_{30}		25		ns
REFER TO FIGURES 18 AND 20 (Slave Serial Interface Modes)[1]					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	3		18	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	25			ns
External SCLK HIGH	t_{36}	10			ns
External SCLK LOW	t_{37}	10			ns

NOTES
[1]In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.
[2]In serial master read during convert mode. See Table I for serial master read after convert mode.

Specifications subject to change without notice.

Table I. Serial clock timings in Master Read after Convert

DIVSCLK[1] **DIVSCLK[0]**		**0** **0**	**0** **1**	**1** **0**	**1** **1**	**unit**
SYNC to SCLK First Edge Delay Minimum	t_{18}	3	17	17	17	ns
Internal SCLK Period minimum	t_{19}	25	50	100	200	ns
Internal SCLK Period maximum	$_{19}$ t	40	70	140	280	ns
Internal SCLK HIGH Minimum	t_{20}	12	22	50	100	ns
Internal SCLK LOW Minimum	t_{21}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{22}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{23}	2	4	30	89	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	3	60	140	300	ns
Busy High Width Maximum	t_{24}	2	2.5	3.5	5.75	µs

ABSOLUTE MAXIMUM RATINGS*

IN[2], TEMP[2],REF, REFBUFIN, INGND, REFGND to AGND . . . . . AVDD + 0.3 V to AGND – 0.3 V

Ground Voltage Differences

AGND, DGND, OGND . . . . . ±0.3 V

Supply Voltages

AVDD, DVDD, OVDD . . . . . -0.3V to +7 V

AVDD to DVDD, AVDD to OVDD . . . . . ±7 V

DVDD to OVDD . . . . . -0.3V to +7 V

Digital Inputs . . . . . –0.3 V to DVDD + 3.0 V

Internal Power Dissipation[3] . . . . . 700 mW

Internal Power Dissipation[4] . . . . . 2.5 W

Junction Temperature . . . . . 150°C

Storage Temperature Range . . . . . –65°C to +150°C

Lead Temperature Range

(Soldering 10 sec) . . . . . 300°C

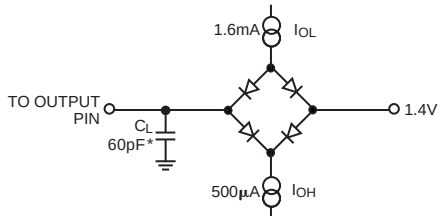
NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]See Analog Input section.

[3]Specification is for the device in free air:
48-Lead LQFP; θ_{JA} = 91°C/W, θ_{JC} = 30°C/W

[4]Specification is for the device in free air:
48-Lead LFCSP; θ_{JA} = 26°C/W



*IN SERIAL INTERFACE MODES, THE SYNC, SCLK, AND SDOUT TIMINGS ARE DEFINED WITH A MAXIMUM LOAD C_L OF 10pF; OTHERWISE, THE LOAD IS 60pF MAXIMUM.

Figure 1. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, C_L = 10 pF

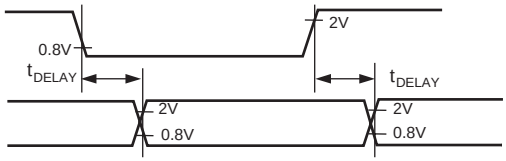


Figure 2. Voltage Reference Levels for Timing

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	
AD7652AST	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48	
AD7652ASTRL	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48	
AD7652ACP	–40°C to +85°C	Chip Scale (LFCSP)	CP-48	
AD7652ACPRL	–40°C to +85°C	Chip Scale (LFCSP)	CP-48	
EVAL-AD7652CB[1]			Evaluation Board	
EVAL-CONTROL BRD2[2]			Controller Board	

NOTES

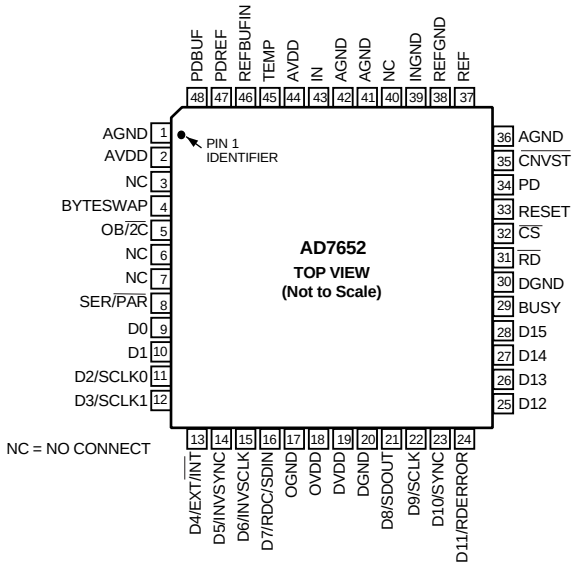
[1]This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD2 for evaluation/demonstration purposes.

[2]This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7652 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
48-Lead LQFP
(ST-48)



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
1,41,42	AGND	P	Analog Power Ground Pin
2,44	AVDD	P	Input Analog Power Pins. Nominally 5 V.
3,6,7 40–42	NC		No Connect
4	BYTESWAP	DI	Parallel Mode Selection (8/16 bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	OB/$\overline{2C}$	DI	Straight Binary/Binary Two's Complement. When OB/$\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted resulting in a two's complement output from its internal shift register.
8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface mode is selected and some bits of the DATA bus are used as a serial port.
9,10	DATA[0:1]	DI	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, these outputs are in high impedance.
11,12	DATA[2:3]or DIVSCLK[0:1]	DI/O	When SER/$\overline{PAR}$ is LOW, these outputs are used as Bit 2 and Bit 3 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, EXT/$\overline{INT}$ is LOW, and RDC/SDIN is LOW, which is serial master read after convert, these inputs, part of the serial port, are used to slow down if desired the internal serial clock which clocks the data output. In other serial moes, these pins are not used
13	DATA[4]	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 4 of the Parallel Port Data Output Bus.
	or EXT/$\overline{INT}$		When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	DATA[5]	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 5 of the Parallel Port Data Output Bus.
	or INVSYNC		When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal. It is active in both master and slave mode. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	DATA[6]	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 6 of the Parallel Port Data Out-
put			Bus.

Pin No.	Mnemonic	Type	Description
	or INVSCLK		When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave mode.
16	DATA[7]	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 7 of the Parallel Port Data Output Bus.
	or RDC/SDIN		When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/$\overline{INT}$. When EXT/$\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on DATA with a delay of 16 SCLK periods after the initiation of the read sequence. When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply than the supply of the host interface (5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 5 V.
20	DGND	P	Digital Power Ground
21	DATA[8]	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 8 of the Parallel Port Data Output Bus.
	or SDOUT		When SER/$\overline{PAR}$ is HIGH, this output, part of the serial port, is used as a serial data out put synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7652 provides the conversion result, MSB first, from its internal shift register. The DATA format is determined by the logic level of OB/$\overline{2C}$. In serial mode, when EXT/$\overline{INT}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode, when EXT/$\overline{INT}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	DATA[9]	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 9 of the Parallel Port Data Output Bus.
	or SCLK		When SER/$\overline{PAR}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, dependent upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	DATA[10]	DO	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 10 of the Parallel Port Data Output Bus.
	or SYNC		When SER/$\overline{PAR}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and remains HIGH while SDOUT output is valid. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid.
24	DATA[11]	DO	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 11 of the Parallel Port Data Output Bus.
	or RDERROR		When SER/$\overline{PAR}$ is HIGH and EXT/$\overline{INT}$ is HIGH, this output, part of the serial port, is used as a incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
25–28	DATA[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data output bus. These pins are always outputs regard less of the state of SER/$\overline{PAR}$.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started, and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The fall ing edge of BUSY could be used as a data ready clock signal.
30	DGND	P	Must Be Tied to Digital Ground
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7652. Current conversion if any is aborted. If not used, this pin could be tied to DGND.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conver sions are inhibited after the current one is completed.

Pin No.	Mnemonic	Type	Description
35	$\overline{\text{CNVST}}$	DI	Start Conversion. If $\overline{\text{CNVST}}$ is HIGH when the acquisition phase (t_8) is complete, the next falling edge on $\overline{\text{CNVST}}$ puts the internal sample/hold into the hold state and initiates a conversion started. This mode is the most appropriate if low sampling jitter is desired. If $\overline{\text{CNVST}}$ is LOW when the acquisition phase (t_8) is complete, the internal sample/hold is put into the hold state and a conversion is immediately started.
36	AGND	P	Must Be Tied to Analog Ground
37	REF	AI	Reference Input Voltage
38	REFGND	AI	Reference Input Analog Ground
39	INGND	AI	Analog Input Ground
43	IN	AI	Primart Analog Input with a Range of 0 to 2.5 V.
45	TEMP	AO	Temperature sensor voltage output.
46	REFBUFIN	AI/O	Reference Input Voltage. The reference output and the reference buffer input.
47	PDREF	DI	Allows choice of Internal or External voltage reference. When HIGH, the internal reference is switched off and an external reference must be used. When low,the on-chip reference is turned on.
48	PDBUF	DI	Allows choice of buffering an internal or external reference with the internal buffer. When LOW, the buffer is selected. When HIGH, the buffer is switched off.

NOTES
AI = Analog Input
AI/O = Bidirectional Analog
AO = Analog Output
DI = Digital Input
DI/O = Bidirectional Digital
DO = Digital Output
P = Power

DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY ERROR (INL)

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

DIFFERENTIAL NONLINEARITY ERROR (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

FULL-SCALE ERROR

The last transition (from 011 . . . 10 to 011 . . . 11 in two's complement coding) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (2.49994278 V for the 0 V–2.5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

UNIPOLAR ZERO ERROR

The first transition should occur at a level 1/2 LSB above analog ground (19.073 μV for the 0 V–2.5 V range). Unipolar zero error is the deviation of the actual transition from that point.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

EFFECTIVE NUMBER OF BITS (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula:

$$ENOB = (S/[N+D]_{dB} - 1.76)/6.02$$

and is expressed in bits.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

SIGNAL TO (NOISE + DISTORTION) RATIO (S/[N+D])

S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

APERTURE DELAY

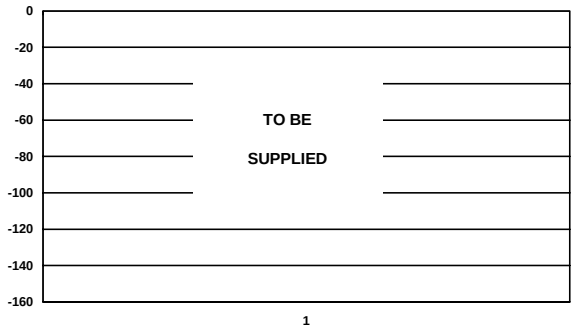
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{CNVST}$ input to when the input signal is held for a conversion.

TRANSIENT RESPONSE

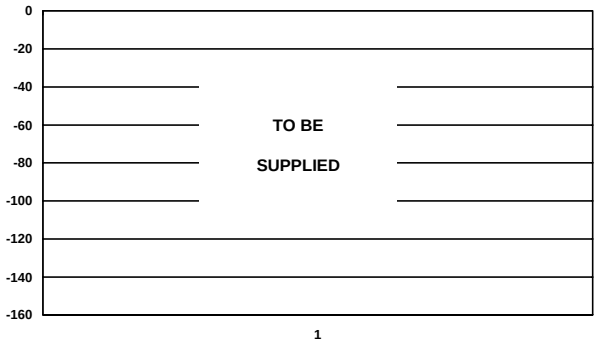
The time required for the AD7652 to achieve its rated accuracy after a full-scale step function is applied to its input.

OVERVOLTAGE RECOVERY

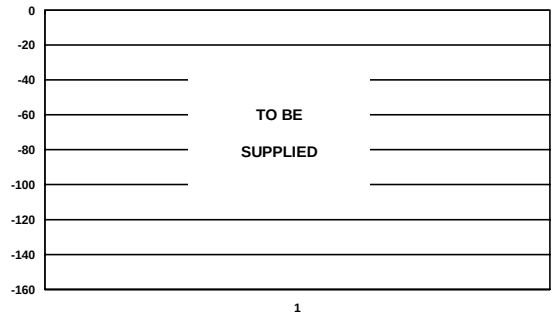
The time required for the ADC to recover to full accuracy after an analog input signal 150% of full-scale is reduced to 50% of the full-scale value.



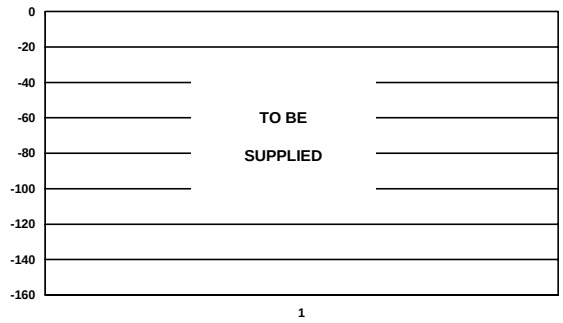
TPC 1. Integral Nonlinearity vs. Code



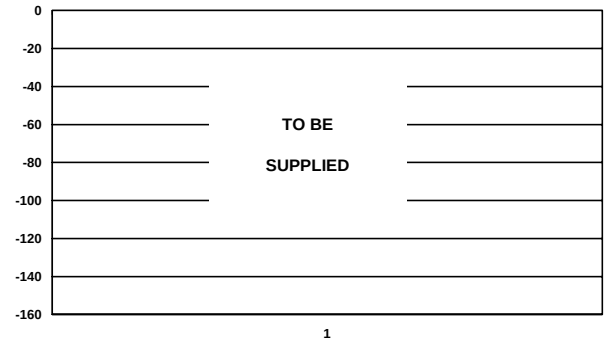
TPC 2. Histogram of 16,384 Conversions of a DC Input at the Code Transition



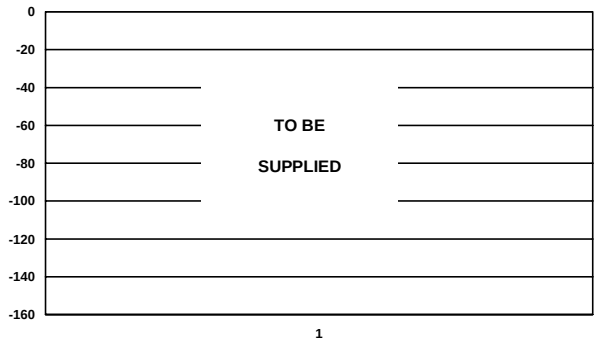
TPC 3. FFT Plot



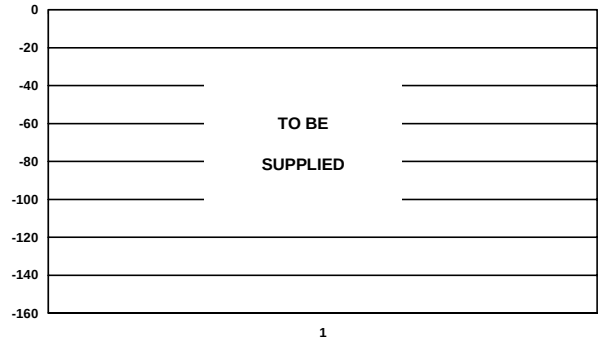
TPC 4. Differential Nonlinearity vs. Code



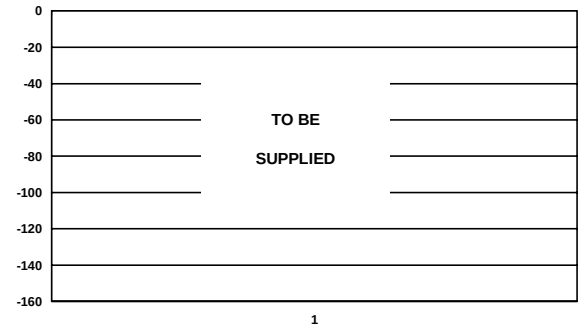
TPC 5. Histogram of 16,384 Conversions of a DC Input at the Code Center



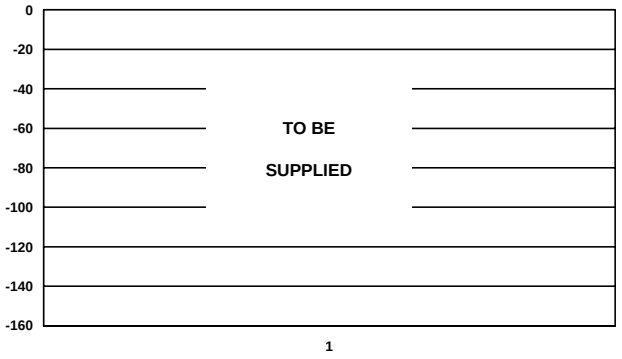
TPC 6. SNR, THD vs. Temperature



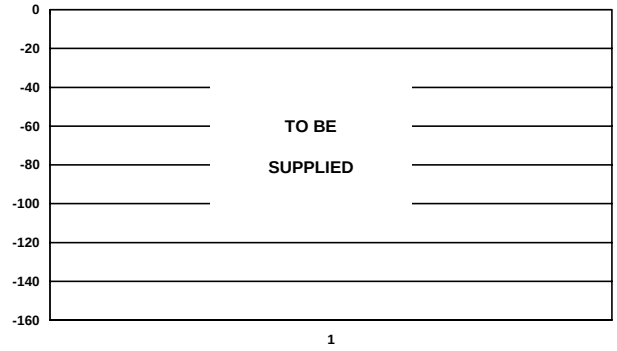
TPC 7. SNR and S/(N+D) vs. Input Level (Referred to Full Scale)



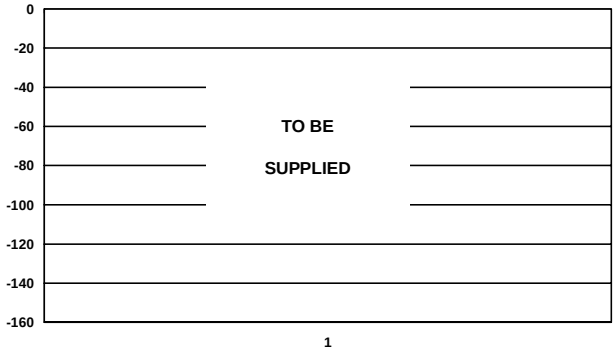
TPC 10. Typical Delay vs. Load Capacitance C_L



TPC 8. Operating Currents vs. Sample Rate



TPC 11. Power-Down Operating Currents vs. Temperature



TPC 9. THD, Harmonics, and SFDR vs. Frequency

CIRCUIT INFORMATION

The AD7652 is a very fast, low power, single supply, precise 16-bit analog-to-digital converter (ADC).

The AD7652 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7652 can be operated from a single 5 V supply and be interfaced to either 5 V or 3 V digital logic. It is housed in either a 48-lead LQFP package or a 48-lead LFCSP that saves space and allows flexible configurations as either serial or parallel interface. The AD7652 is pin-to-pin compatible with PulSAR ADC's and is an upgrade of the AD7651.

CONVERTER OPERATION

The AD7652 is a successive-approximation analog-to-digital converter based on a charge redistribution DAC. Figure 3 shows the simplified schematic of the ADC. The capacitive DAC consists of an array of 16 binary weighted capacitors and an additional "LSB" capacitor. The comparator's negative input is connected to a "dummy" capacitor of the same value as the capacitive DAC array.

During the acquisition phase, the common terminal of the array tied to the comparator's positive input is connected to AGND via SW_A. All independent switches are connected to the analog input IN. Thus, the capacitor array is used as a sampling capacitor and acquires the analog signal on IN input. Similarly, the "dummy" capacitor acquires the analog signal on INGND input.

When the $\overline{\text{CNVST}}$ input goes low, a conversion phase is initiated. When the conversion phase begins, SW_A and SW_B are opened first. The capacitor array and the "dummy" capacitor are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between IN and INGND captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND or REF, the comparator input varies by binary-weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$, . . . $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB first, to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

Transfer Functions

Using the OB/$\overline{\text{2C}}$ digital input, the AD7652 offers two output codings: straight binary and two's complement. The LSB size is $V_{REF}/65536$, which is about 38.15 µV. The ideal transfer characteristic for the AD7652 is shown in Figure 4 and Table I.

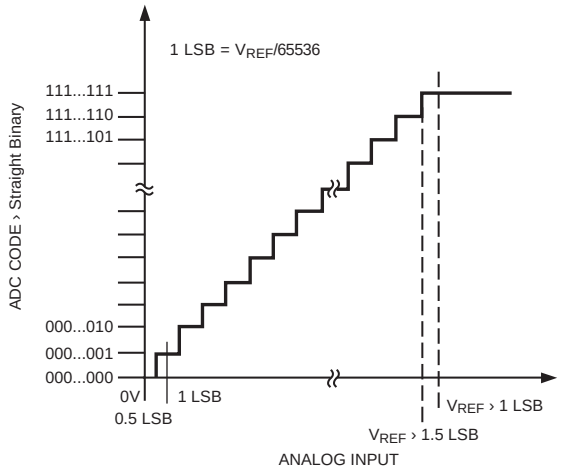


Figure 4. ADC Ideal Transfer Function

Table I. Output Codes and Ideal Input Voltages

Description	Analog Input	Digital Output Code Hexa Straight Binary	Two's Comple-
FSR –1 LSB	2.499962 V	FFFF[1]	7FFF[1]
FSR – 2 LSB	2.499923 V	FFFE	7FFE
Midscale + 1 LSB	1.250038 V	8001	0001
Midscale	1.25 V	8000	0000
Midscale – 1 LSB	1.249962 V	7FFF	FFFF
–FSR + 1 LSB	38 µV	0001	8001
–FSR	0 V	0000[2]	8000[2]

NOTES

[1]This is also the code for overrange analog input ($V_{IN} - V_{INGND}$ above $V_{REF} - V_{REFGND}$).

[2]This is also the code for underrange analog input (V_{IN} below V_{INGND}).

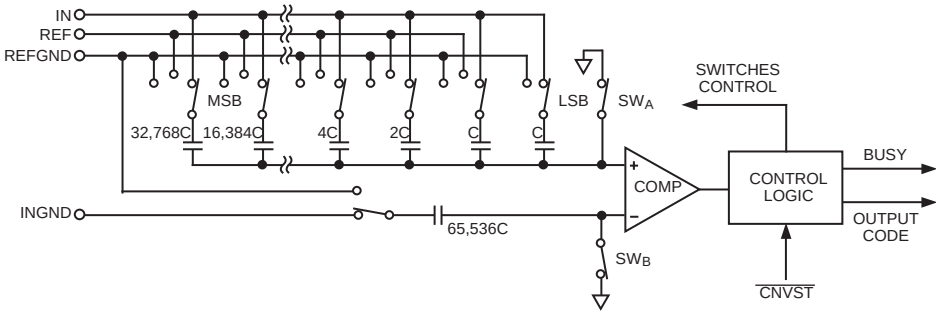


Figure 3. ADC Simplified Schematic

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7652.

Analog Input

Figure 6 shows an equivalent circuit of the input structure of the AD7652.

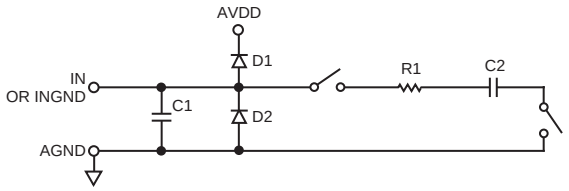


Figure 6. Equivalent Analog Input Circuit

The two diodes D1 and D2 provide ESD protection for the analog inputs IN and INGND. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 100 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from AVDD. In such case, an input buffer with a short circuit current limitation can be used to protect the part.

This analog input structure allows the sampling of the differential signal between IN and INGND. Unlike other converters, the INGND input is sampled at the same time as the IN input. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 7, which represents the typical CMRR over frequency. For instance, by using INGND to sense a remote signal ground, difference of ground potentials between the sensor and the local ADC ground are eliminated.

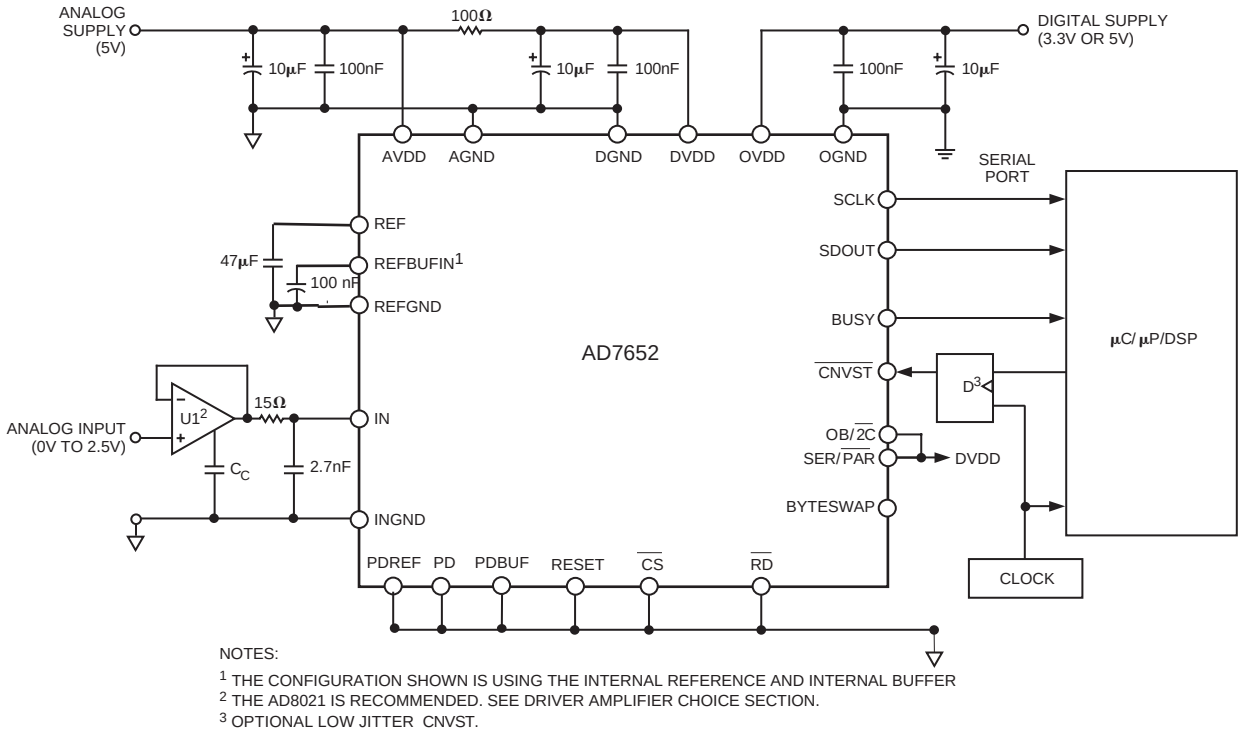


Figure 5. Typical Connection Diagram

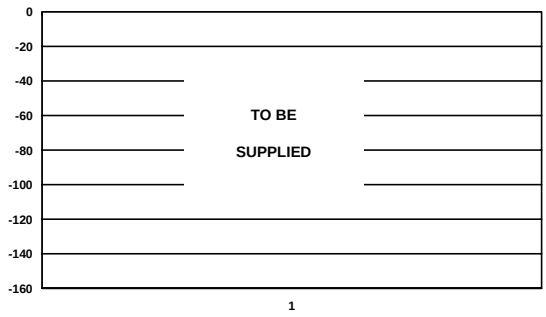


Figure 7. Analog Input CMR vs. Frequency

During the acquisition phase, the impedance of the analog input IN can be modeled as a parallel combination of capacitor C1 and the network formed by the series connection of R1 and C2. Capacitor C1 is primarily the pin capacitance. The resistor R1 is typically TBD **Ω** and is a lumped component made up of some serial resistors and the on resistance of the switches. The capacitor C2 is typically 60 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C1. The R1, C2 makes a one-pole low-pass filter that reduces undesirable aliasing effect and limits the noise.

Driver Amplifier Choice

Although the AD7652 is easy to drive, the driver amplifier needs to meet at least the following requirements:

– The driver amplifier and the AD7652 analog input circuit must be able together to settle for a full-scale step the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, the settling at 0.1% to 0.01% is more commonly specified. It could significantly differ from the settling time at 16 bit level and it should therefore be verified prior to the driver selection. The tiny op amp AD8021, which combines ultralow noise and a high-gain bandwidth, meets this settling time requirement even when used with high gain up to 13.

– The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7652. The noise coming from the driver is filtered by the AD7652 analog input circuit one-pole low-pass filter made by R1 and C2 or the external filter if any is used. The SNR degradation due to the amplifier is:

– The driver needs to have a THD performance suitable to that of the AD7652.

The AD8021 meets these requirements and is usually appropriate for almost all applications. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type.

The AD8022 could also be used where dual version is needed and gain of 1 is used.

The AD829 is another alternative where high-frequency (above 100 kHz) performance is not required. In gain of 1, it requires an 82 pF compensation capacitor.

The AD8610 is another option where low bias current is needed in low-frequency applications.

Voltage Reference Input

The AD7652 allows the choice of either an internal 2.5 V voltage reference or an external 2.5 V reference.

To use the internal reference along with the internal buffer, PDREF and PDBUF should both be LOW. This will produce a voltage on REFBUFIN of 1.25 V and the buffer's gain will be 2, resulting in a 2.5 V reference.

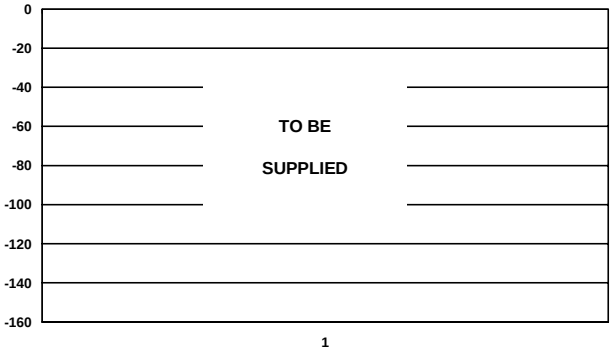
To use an external reference along with the internal buffer, PDREF should be HIGH and PDBUF should be low. This powers down the internal reference and allows for the 2.5 V reference to be applied to REFBUFIN. In this mode the buffer's gain is 1.

To use both external reference and external buffer, PDREF and PDBUF should both be HIGH. The reference input should be applied to REF.

It is useful to decouple the REFBUFIN pin with a 100 nF ceramic capacitor. The output impedance of the REFBUFIN pin is 4 k**Ω**. Thus, the 100 nF capacitor provides an RC filter for noise reduction.

It should be noted that the internal reference and internal buffer are independent of the power down (PD) pin of the part. Powering down the part does not power down the internal reference or the internal buffer. Furthermore, powering down the internal reference and internal buffer, as well as powering them up, requires time. This is due to the fact that we have charging and discharging capacitors on the REF which require some settling time. Therefore, for applications requiring low power, there will always be a typical of 10 mW of power dissipated if you decide to use the internal reference and internal buffer even during times with no conversions.

The internal reference is temperature compensated to 2.5V ± TBD mV. The reference is trimmed to provide a typical drift of TBD ppm/°C. This typical drift characteristic is shown in Figure TBD. For improved drift performance, an external reference such as the AD780 can be used.



For the external reference, the voltage reference input REF of the AD7652 has a dynamic input impedance; it should therefore be driven by a low-impedance source with an efficient decoupling between REF and REFGND inputs. This decoupling depends on the choice of the voltage reference but usually consists of a 1 µF ceramic capacitor and a low ESR tantalum capacitor connected to the REF and REFGND

inputs with minimum parasitic inductance. 47 µF is an appropriate value for the tantalum capacitor when using either the internal reference of one of the recommended reference voltages:

– The low noise, low temperature drift ADR421 and AD780 voltage references
– The low power ADR291 voltage reference
– The low cost AD1582 voltage reference

For applications using multiple AD7652s, it is more effective to buffer the reference voltage using the internal buffer. To do so, PDREF should be HIGH, and PDBUF should be low.

Care should also be taken with the reference temperature coefficient of the voltage reference which directly affects the full-scale accuracy if this parameter matters. For instance, a ±15 ppm/°C tempco of the reference changes the full scale by ±1 LSB/°C.

V_{REF} , as mentioned in the specification table, could be increased to AVDD – 1.85 V. The benefit here is the increased SNR obtained as a result of this increase. Since the input range is defined in terms of V_{REF}, this would essentially increase the range to make it a 0 to 3 V input range with an AVDD above 4.85 V. One of the benefits here is the additional SNR obtained as a result of this increase. The theoretical improvement as a result of this increase in reference is 1.58 dB (20 log [3/2.5]). Due to the theoretical quantization noise, however, the observed improvement is approximately 1 dB. The AD780 can be selected with a 3 V reference voltage.

The TEMP pin, which measures the temperature of the AD7652, can be used as follows. Refer to figure TBD to see the connectivity. The output of the TEMP pin is applied to one of the inputs of the analog switch (ADG779). The other input, as shown is the analog signal. The output of the switch is connected to the AD8021 which is configured as a follower. The output of the op-amp is applied to the IN pin. Refer to the Specification Table for the appropriate values related to the TEMP pin. This configuration could be very useful to improve the calibration accuracy over the temperature range.

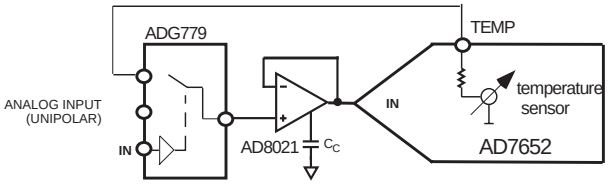


Figure TBD

Power Supply

The AD7652 uses three sets of power supply pins: an analog 5 V supply AVDD, a digital 5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.7 V and DVDD + 0.3 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 5. The AD7652 is independent of power supply sequencing, once OVDD does not exceed DVDD by more than 0.3V, and thus free from supply voltage induced latchup.

POWER DISSIPATION Vs. THROUGHPUT

Operating currents are very low during the acquisition phase, which allows a significant power saving when the conversion rate is reduced as shown in Figure 10. This power saving depends on the mode used. The AD7652 automatically reduces its power consumption at the end of each conversion phase. This feature makes the AD7652 ideal for very low power battery applications. It should be noted that the digital interface and reference remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power supply rails (i.e., DVDD or DGND) and OVDD should not exceed DVDD by more than 0.3V.

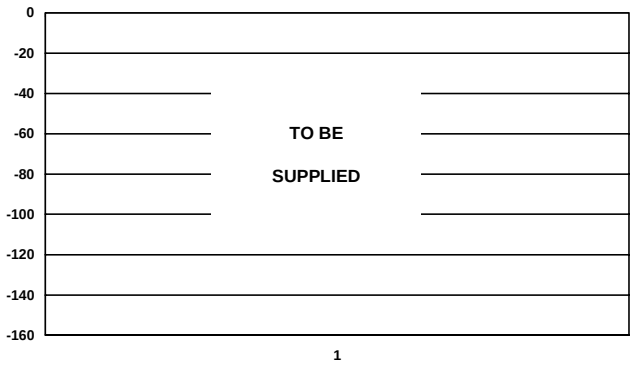


Figure 10. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 11 shows the detailed timing diagrams of the conversion process. The AD7652 is controlled by the signal $\overline{\text{CNVST}}$ which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals.

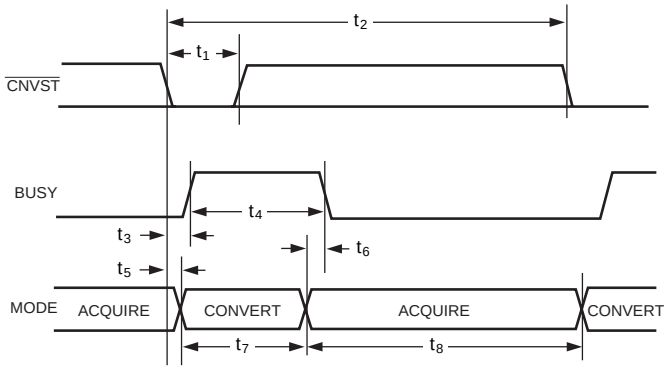


Figure 11. Basic Conversion Timing

Conversions can be automatically initiated. If $\overline{CNVST}$ is held low when BUSY is low, the AD7652 controls the acquisition phase and then automatically initiates a new conversion. By keeping $\overline{CNVST}$ low, the AD7652 keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes low. Also, at power-up, $\overline{CNVST}$ should be brought low once to initiate the conversion process. In this mode, the AD7652 could sometimes run slightly faster then the guaranteed limits of 500 kSPS.

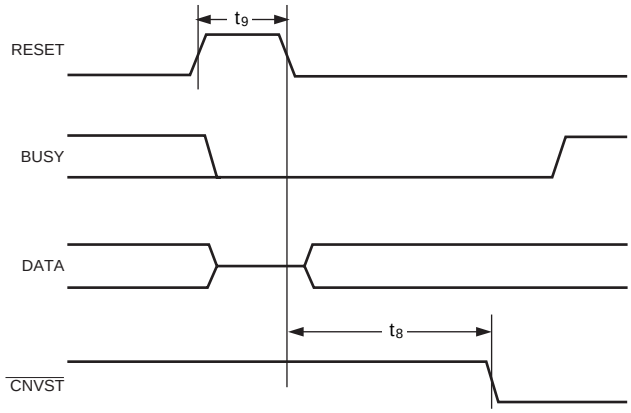


Figure 12. RESET Timing

Although $\overline{CNVST}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot and undershoot or ringing.

It is a good thing to shield the $\overline{CNVST}$ trace with ground and also to add a low value serial resistor (i.e., 50 ý) termination close to the output of the component that drives this line.

For applications where the SNR is critical, $\overline{CNVST}$ signal should have a very low jitter. Some solutions to achieve that is to use a dedicated oscillator for $\overline{CNVST}$ generation or, at least, to clock it with a high-frequency low-jitter clock as shown in Figure 5.

DIGITAL INTERFACE

The AD7652 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7652 digital interface also accommodates both 3 V or 5 V logic by simply connecting the OVDD supply pin of the AD7652 to the host system interface digital supply. Finally, by using the OB/$\overline{2C}$ input pin, both two's complement or straight binary coding can be used.

The two signals $\overline{CS}$ and $\overline{RD}$ control the interface. $\overline{CS}$ and $\overline{RD}$ have a similar effect because they are OR'd together internally. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7652 in multicircuits applications and is held low in a single AD7652 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

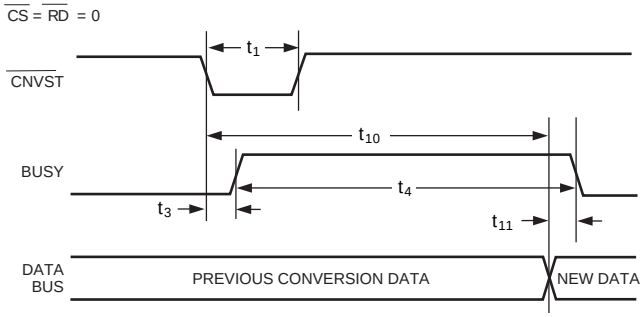


Figure 13. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The AD7652 is configured to use the parallel interface when the SER/$\overline{PAR}$ is held low. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion as shown, respectively, in Figure 14 and Figure 15. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. That avoids any potential feed-through between voltage transients on the digital interface and the most critical analog conversion circuitry.

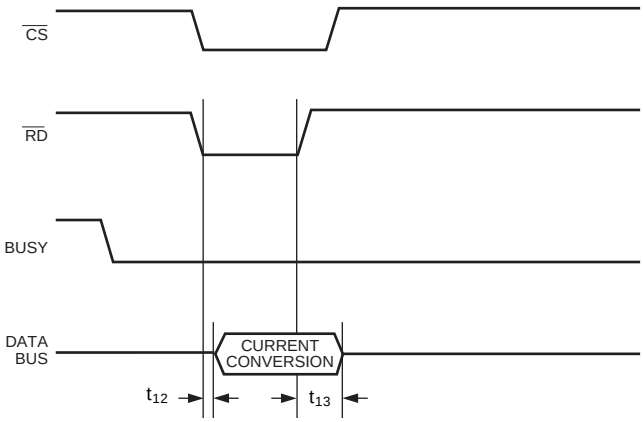


Figure 14. Slave Parallel Data Timing for Reading (Read After Convert)

The BYTESWAP pin allows a glueless interface to a 8 bits bus. As shown in Figure TBD, the LSB byte is output on D[7:0] and the MSB is output on D[15:8] when BYTESWAP is low. When BYTESWAP is high, the LSB and MSB bytes are swapped and the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16 bits data can be read in 2 bytes on either D[15:8] or D[7:0].

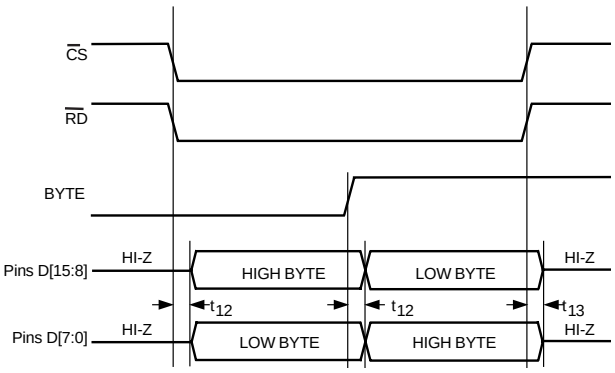


Figure TBD, 8-bit Parallel

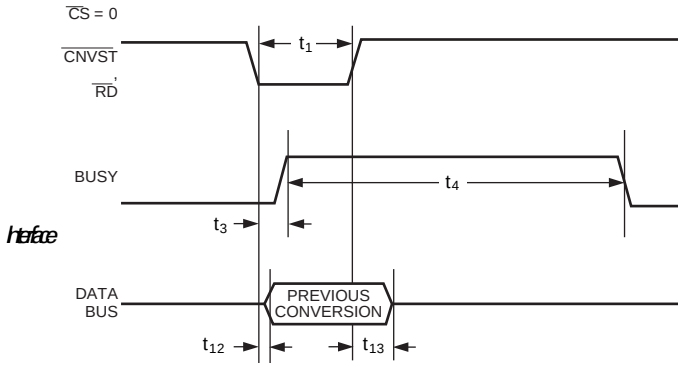


Figure 15. Slave Parallel Data Timing for Reading

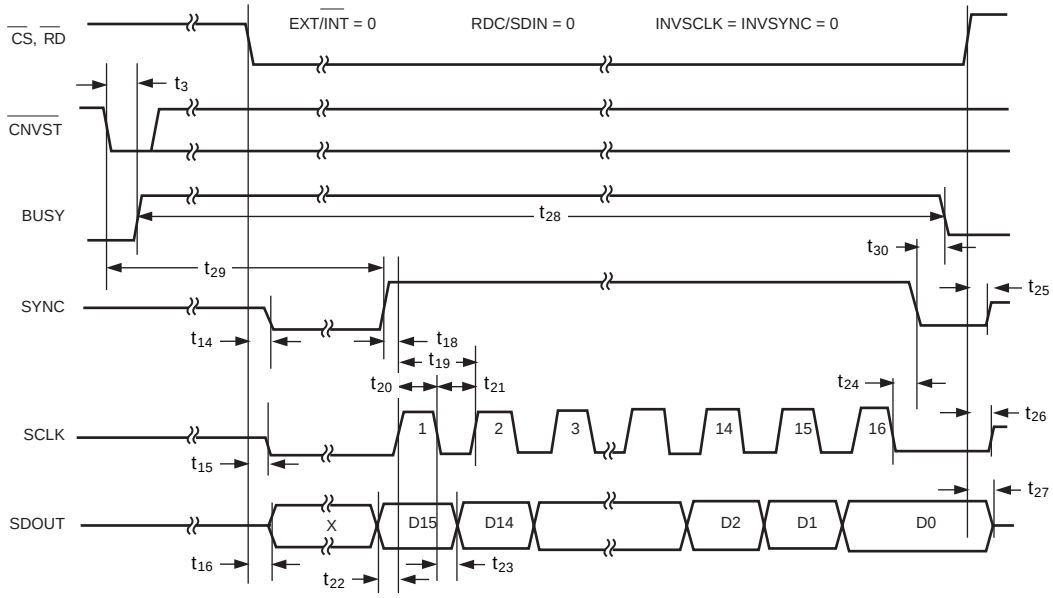


Figure 16. Master Serial Data Timing for Reading (Read After Convert)

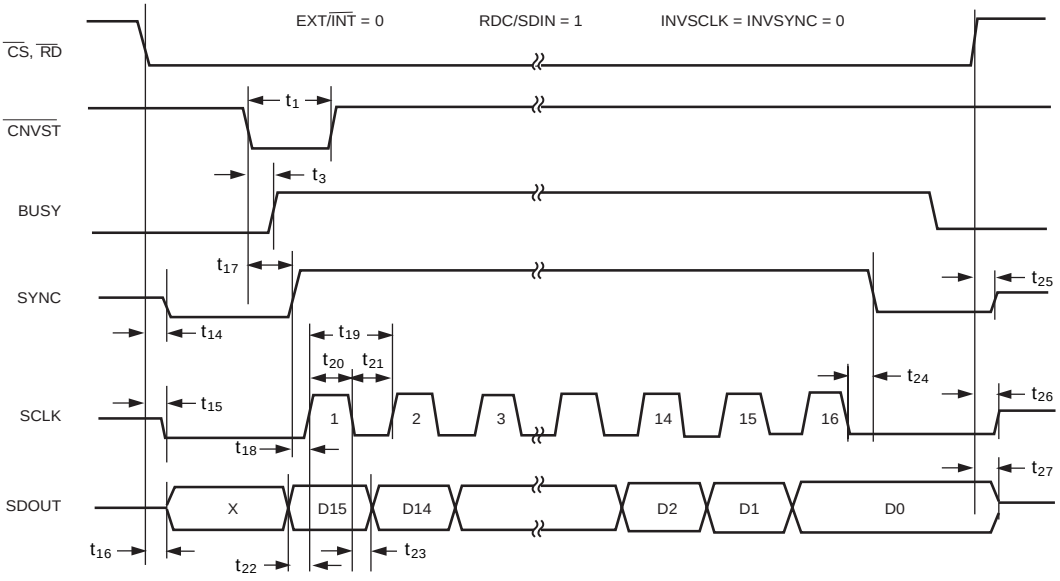


Figure 17. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

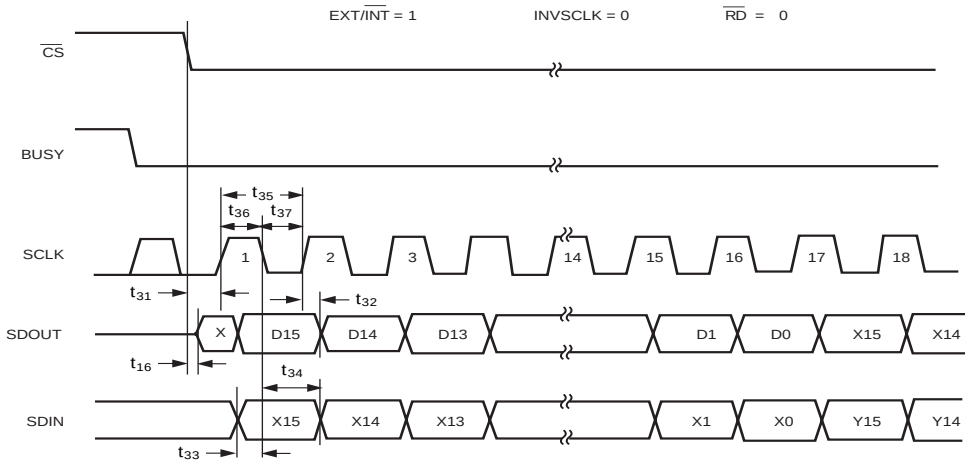


Figure 18. Slave Serial Data Timing for Reading (Read After Convert)

(Read During Convert)

SERIAL INTERFACE

The AD7652 is configured to use the serial interface when the SER/$\overline{\text{PAR}}$ is held high. The AD7652 outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on SCLK pin. The output data is valid on both the rising and falling edge of the data clock.

MASTER SERIAL INTERFACE

Internal Clock

The AD7652 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{\text{INT}}$ pin is held low. The AD7652 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. Depending on RDC/SDIN input, the data can be read after each conversion or during the following conversion. Figure 16 and Figure 17 show the detailed timing diagrams of these two modes.

Usually, because the AD7652 is used with a fast throughput, the mode master, read during conversion is the most recommended serial mode when it can be used.

In read-during-conversion mode, the serial clock and data toggle at appropriate instants which minimize potential feedthrough between digital activity and the critical conversion decisions.

In read-after-conversion mode, it should be noted that, unlike in other modes, the signal BUSY returns low after the 16 data bits are pulsed out and not at the end of the conversion phase which results in a longer BUSY width.

SLAVE SERIAL INTERFACE

External Clock

The AD7652 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{\text{INT}}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{\text{CS}}$. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 18 and Figure 20 show the detailed timing diagrams of these methods.

While the AD7652 is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7652 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 18 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the result of this conversion can be read while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. The data is shifted out, MSB first, with 16 clock pulses and is valid on both rising and falling edge of the clock.

Among the advantages of this method, the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process.

Another advantage is to be able to read the data at any speed up to 40 MHz which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7652 provides a "daisy-chain" feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 19. Simultaneous sampling is possible by using a common $\overline{\text{CNVST}}$ signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite to the one used to shift out the data on SDOUT. Hence, the MSB of the "up-

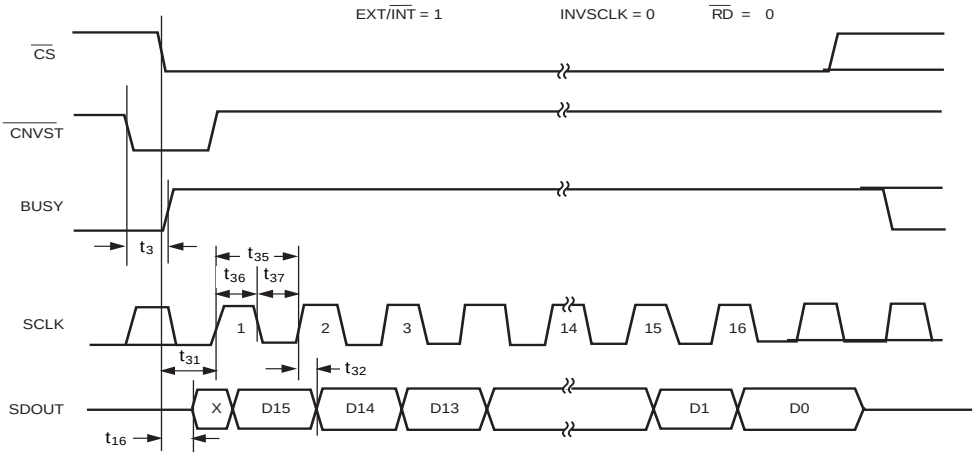


Figure 20. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

stream" converter just follows the LSB of the "downstream" converter on the next SCLK cycle.

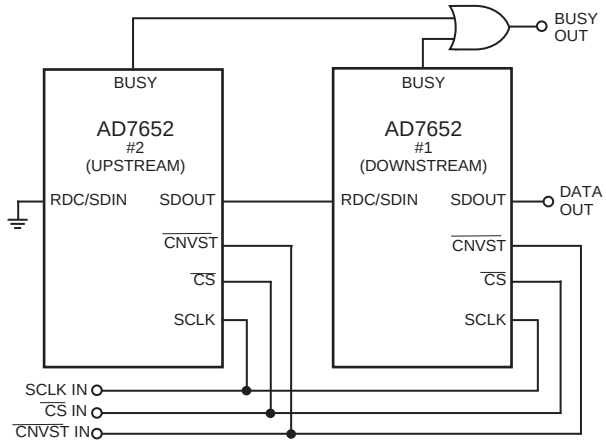


Figure 19. Two AD7652s in a "Daisy-Chain" Configuration

External Clock Data Read During Conversion

Figure 20 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are both low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 16 clock pulses and is valid on both rising and falling edge of the clock. The 16 bits have to be read before the current conversion is complete. If that is not done, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no "daisy chain" feature in this mode and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock of, at least 18 MHz, is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated. That allows the use of a slower clock speed like 14 MHz.

MICROPROCESSOR INTERFACING

The AD7652 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7652 is designed to interface either with a parallel 16-bit-wide interface or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7652 to prevent digital noise from coupling into the ADC. The following sections illustrate the use of the AD7652 with an SPI-equipped microcontroller, the ADSP-21065L and ADSP-218x signal processors.

SPI Interface (MC68HC11)

Figure 21 shows an interface diagram between the AD7652 and an SPI-equipped microcontroller like the MC68HC11. To accommodate the slower speed of the microcontroller, the AD7652 acts as a slave device and data must be read after conversion. This mode allows also the "daisy chain" feature.

The convert command could be initiated in response to an internal timer interrupt. The reading of output data, one byte at a time, if necessary, could be initiated in response to the end-of-conversion signal (BUSY going low) using to an interrupt line of the microcontroller. The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1), Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1 and SPI Interrupt Enable (SPIE = 1) by writing to the SPI Control Register (SPCR). The IRQ is configured for edge-sensitive-only operation (IRQE = 1 in OPTION register).

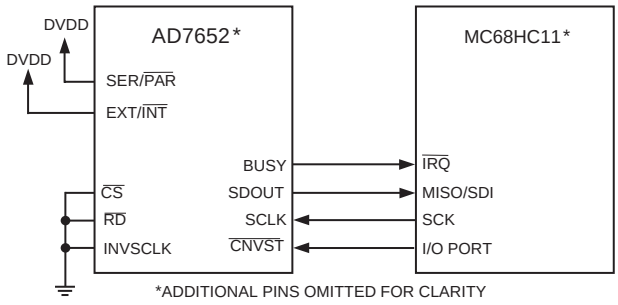


Figure 21. Interfacing the AD7652 to SPI Interface

ADSP-21065L in Master Serial Interface

As shown in Figure 22, the AD7652 can be interfaced to the ADSP-21065L using the serial interface in master mode without any glue logic required. This mode combines the advantages of reducing the number of wire connections and being able to read the data during or after conversion at user convenience.

The AD7652 is configured for the internal clock mode (EXT/$\overline{INT}$ low) and acts, therefore, as the master device. The convert command can be generated by either an external low jitter oscillator or, as shown, by a FLAG output of the ADSP-21065L or by a frame output TFS of one serial port of the ADSP-21065L which can be used as a timer. The serial port on the ADSP-21065L is configured for external clock (IRFS = 0), rising edge active (CKRE = 1), external late framed sync signals (IRFS = 0, LAFS = 1, RFSR = 1) and active high (LRFS = 0). The serial port of the ADSP-21065L is configured by writing to its receive control register (SRCTL)—see ADSP-2106x SHARC User's Manual. Because the serial port within the ADSP-21065L will be seeing a discontinuous clock, an initial word reading has to be done after the ADSP-21065L has been reset to ensure that the serial port is properly synchronized to this clock during each following data read operation.

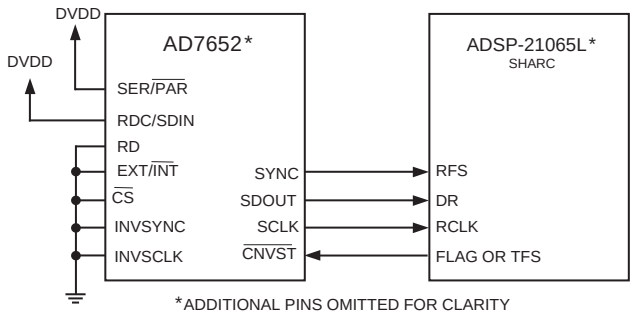


Figure 22. Interfacing to the ADSP-21065L Using the Serial Master Mode

APPLICATION HINTS

Bipolar and Wider Input Ranges

In some applications, it is desired to use a bipolar or wider analog input range like, for instance, ±10 V, ±5 V or 0 V to 5 V. Although the AD7652 has only one unipolar range, by simple modifications of the input driver circuitry, bipolar and wider input ranges can be used without any performance degradation.

Figure 23 shows a connection diagram which allows that. Components values required and resulting full-scale ranges are shown in Table II.

For applications where accurate gain and offset are desired, they can be calibrated by acquiring a ground and a voltage reference using an analog multiplexer, U2, as shown for bipolar input ranges in Figure 23.

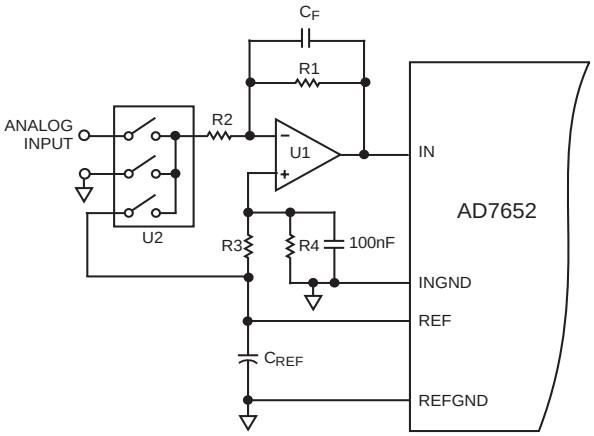


Figure 23. Using the AD7652 in 16-Bit Bipolar and/or Wider Input Ranges

Table II. Component Values and Input Ranges

Input Range	R1	R2	R3	R4
±10 V	250 Ω	2 kΩ	10 kΩ	8 kΩ
±5 V	500 Ω	2 kΩ	10 kΩ	6.67 kΩ
0 V to –5 V	1 kΩ	2 kΩ	None	0 Ω

Layout

The AD7652 has very good immunity to noise on the power supplies as can be seen in Figure 9. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7652 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7652, or, at least, as close as possible to the AD7652. If the AD7652 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7652.

It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7652 to avoid noise coupling. Fast switching signals like $\overline{CNVST}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board.

The power supplies lines to the AD7652 should use as large trace as possible to provide low impedance paths and reduce the effect of glitches on the power supplies lines. Good decoupling is also important to lower the supplies impedance

presented to the AD7652 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supplies pins AVDD, DVDD, and OVDD close to, and ideally right up against, these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7652 can be either a separate supply or come from the analog supply AVDD or the digital interface supply OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended that if no separate supply available, connect the DVDD digital supply to the analog supply, AVDD, through an RC filter as shown in Figure 5, and connect the system supply to the interface digital supply, OVDD, and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high-frequency spikes.

The AD7652 has five different ground pins: INGND, REFGND, AGND, DGND, and OGND. INGND is used to sense the analog input signal. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

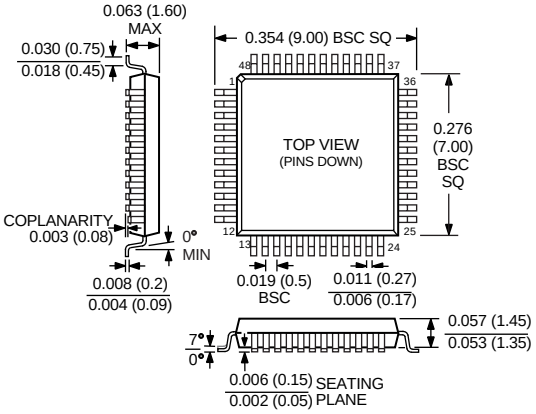
Evaluating the AD7652 Performance

A recommended layout for the AD7652 is outlined in the evaluation board for the AD7652. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Eval-Control Board.

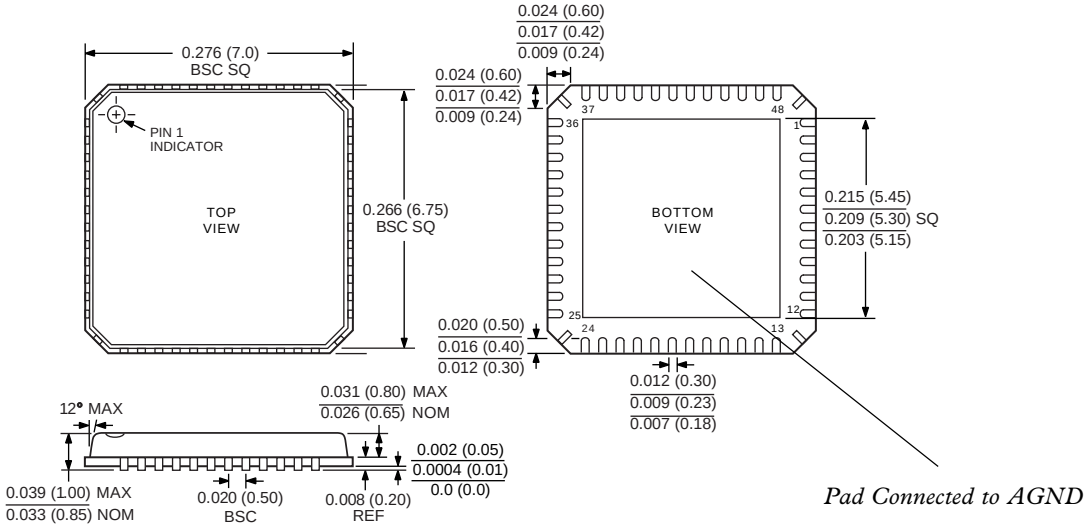
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Quad Flatpack (LQFP)
(ST-48)



48-Lead Frame Chip Scale Package (LQFP)
(CP-48)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS