Charge Pump Regulator for Color TFT Panels

ADM8839

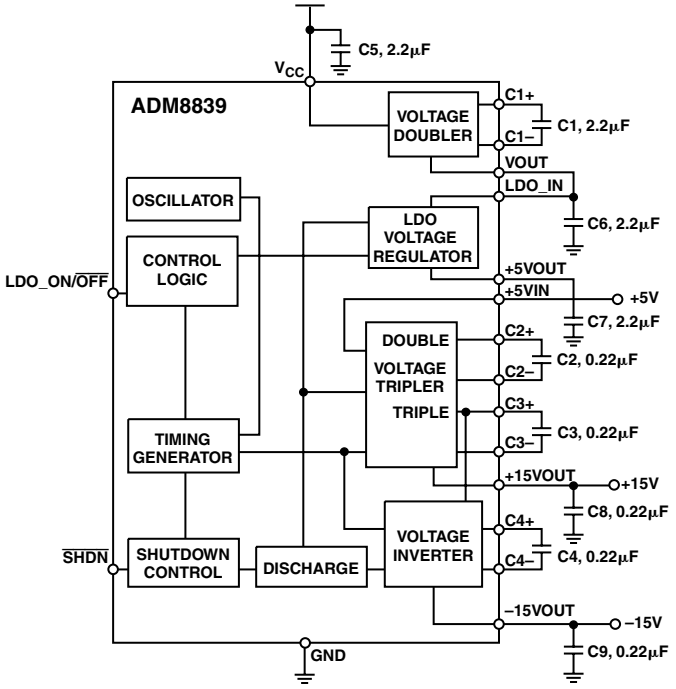
FEATURES

- 3 Voltages (+5 V, +15 V, –15 V) from a Single 3 V Supply
- Power Efficiency Optimized for Use with TFT in Mobile Phones
- Low Quiescent Current
- Low Shutdown Current (<5 μA)
- Shutdown Function
- Option to Use External LDO

APPLICATIONS

- Hand-held Instruments
- TFT LCD Panels
- Cellular Phones

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM8839 is a charge pump regulator used for color thin film transistor (TFT) liquid crystal displays (LCDs). Using charge pump technology, the device can be used to generate three voltages (+5 V ±2%, +15 V, –15 V) from a single 3 V supply. These voltages are then used to provide supplies for the LCD controller (5 V) and the gate drives for the transistors in the panel (+15 V and –15 V). Only a few external capacitors are needed for the charge pumps. An efficient low dropout (LDO) voltage regulator ensures that the power efficiency is high and provides a low ripple 5 V output. This LDO can be shut down and an external LDO can be used to regulate the 5 V doubler output and drive the input to the charge pump section that generates the +15 V and –15 V outputs, if required by the user.

The ADM8839 has a power save shutdown feature. The 5 V output consumes the most power, so power efficiency is also maximized on this output with an oscillator enabling scheme (Green Idle™). This effectively senses the load current that is flowing and turns on the charge pump only when charge needs to be delivered to the 5 V pump doubler output.

The ADM8839 is fabricated using CMOS technology for minimal power consumption. The part is packaged in a 20-lead LFCSP (lead frame chip scale package).

REV. A

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ADM8839–SPECIFICATIONS (V_{CC} = 3 V – 10%, 40%; T_A = –40°C to +85°C; C1, C5, C6, C7 = 2.2 μF; C2, C3, C4, C8, C9 = 0.22 μF; unless otherwise noted.)

Parameter	Test Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE, V_{CC}		2.7		4.2	V
SUPPLY CURRENT, I_{CC}	Unloaded		250	500	μA
	Shutdown Mode, T_A = 25°C			5	μA
+5 V OUTPUT					
Output Voltage	I_L = 10 μA to 8 mA	4.9	5.0	5.1	V
Output Current			5	8	mA
Output Ripple	8 mA Load		10		mV p-p
Transient Response	I_L Stepped from 10 μA to 8 mA		5		μs
+15 V OUTPUT					
Output Voltage	I_L = 1 μA to 150 μA	14.0	15.0	16.0	V
Output Current			1	150	μA
Output Ripple	I_L = 100 μA		50		mV p-p
–15 V OUTPUT					
Output Voltage	I_L = –1 μA to –150 μA	–16.0	–15.0	–14.0	V
Output Current		–150	–1		μA
Output Ripple	I_L = –100 μA		50		mV p-p
POWER EFFICIENCY	$R5V_{OUT}$ Load = 5 mA, ±15 V Load = ±150 μA, V_{CC} = 3.0 V		82		%
CHARGE PUMP FREQUENCY		60	100	140	kHz
CONTROL PINS, $\overline{SHDN}$					
Input Voltage, $V_{\overline{SHDN}}$	$\overline{SHDN}$ Low = Shutdown Mode			0.3 × V_{CC}	V
	$\overline{SHDN}$ High = Normal Mode	0.7 × V_{CC}			V
Digital Input Current				±1	μA
Digital Input Capacitance*				10	pF
LDO_ON/$\overline{OFF}$					
Input Voltage	Low = External LDO			0.3 × V_{CC}	V
	High = Internal LDO	0.7 × V_{CC}			V
Digital Input Current				±1	μA
Digital Input Capacitance*				10	pF

*Guaranteed by design. Not 100% production tested.

Specifications are target values and are subject to change without notice.

TIMING SPECIFICATIONS (V_{CC} = 3 V, T_A = 25°C; C1, C5, C6, C7 = 2.2 μF; C2, C3, C4, C8, C9 = 0.22 μF.)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-UP SEQUENCE					
+5 V Rise Time, t_{R5V}	10% to 90%, Figure 1		250		μs
+15 V Rise Time, t_{R15V}	10% to 90%, Figure 1		3		ms
–15 V Fall Time, t_{FM15V}	90% to 10%, Figure 1		3		ms
Delay between –15 V Fall and +15 V, t_{DELAY}	Figure 1		600		μs
POWER-DOWN SEQUENCE					
+5 V Fall Time, t_{F5V}	90% to 10%, Figure 1		35		ms
+15 V Fall Time, t_{F15V}	90% to 10%, Figure 1		10		ms
–15 V Rise Time, t_{RM15V}	10% to 90%, Figure 1		20		ms

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

Supply Voltage . . . . . –0.3 V to +6.0 V
Input Voltage on Digital Inputs . . . . . –0.3 V to +6.0 V
Output Short-Circuit Duration to GND . . . . . 10 sec
Output Voltage
  +5 V Output . . . . . 0 V to 7.0 V
  –15 V Output . . . . . –17 V to +0.3 V
  +15 V Output . . . . . –0.3 V to +17 V
Operating Temperature Range . . . . . –40°C to +85°C
Power Dissipation . . . . . 50 mW
Storage Temperature Range . . . . . –65°C to +150°C
ESD . . . . . Class I

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

20-Lead LFCSP Package:
θ_{JA} = 31°C/W

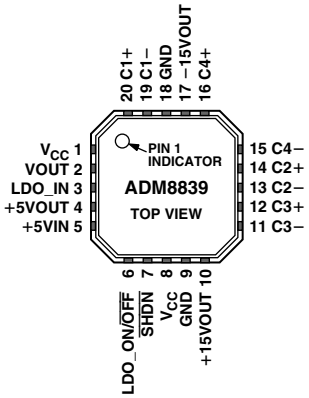
ORDERING GUIDE

Model	Temperature Range	Package Option
ADM8839ACP	–40°C to +85°C	CP-20

CAUTION

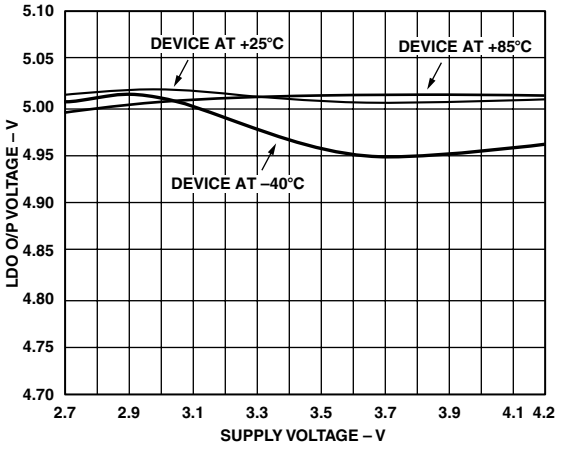
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM8839 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

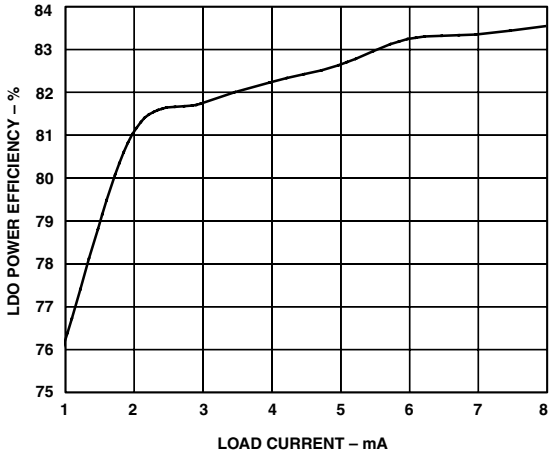


PIN FUNCTION DESCRIPTIONS

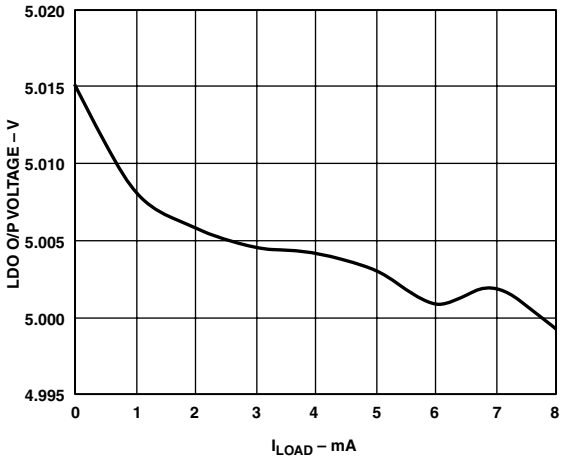
Pin No.	Mnemonic	Function
1	V_{CC}	Positive Supply Voltage Input. Connect this pin to the 3 V supply with a 2.2 μF decoupling capacitor.
2	VOUT	Voltage Doubler Output. This was derived by doubling the 3 V supply. A 2.2 μF capacitor to ground is required on this pin.
3	LDO_IN	Voltage Regulator Input. The user may bypass this circuit by using the LDO_ON/$\overline{OFF}$ pin.
4	+5VOUT	5 V Output. This was derived by doubling and regulating the 3 V supply. A 2.2 μF capacitor to ground is required on this pin to stabilize the regulator.
5	+5VIN	5 V Input. This is the input to the voltage tripler and inverter charge pump circuits.
6	LDO_ON/$\overline{OFF}$	Control Logic Input. 3 V CMOS logic. A logic high selects the internal LDO for regulation of the 5 V voltage doubler output. A logic low isolates the internal LDO from the rest of the charge pump circuits. This allows the use of an external LDO to regulate the 5 V voltage doubler output. The output of this LDO is then fed back into the voltage tripler and inverter circuits of the ADM8839.
7	$\overline{SHDN}$	Digital Input. 3 V CMOS logic. Active low shutdown control. This shuts down the timing generator and enables the discharge circuit to dissipate the charge on the voltage outputs, thus driving them to 0 V.
8	V_{CC}	Connect this pin to V_{CC}.
9	GND	Connect this pin to GND.
10	+15VOUT	15 V Output. This was derived by tripling the 5 V regulated output. A 0.22 μF capacitor is required on this pin.
11, 12	C3–, C3+	External capacitor C3 is connected between these pins. A 0.22 μF capacitor is recommended.
13, 14	C2–, C2+	External capacitor C2 is connected between these pins. A 0.22 μF capacitor is recommended.
15, 16	C4–, C4+	External capacitor C4 is connected between these pins. A 0.22 μF capacitor is recommended.
17	–15VOUT	–15 V Output. This was derived by tripling and inverting the 5 V regulated output. A 0.22 μF capacitor is required on this pin.
18	GND	Device Ground.
19, 20	C1–, C1+	External capacitor C1 is connected between these pins. A 2.2 μF capacitor is recommended.



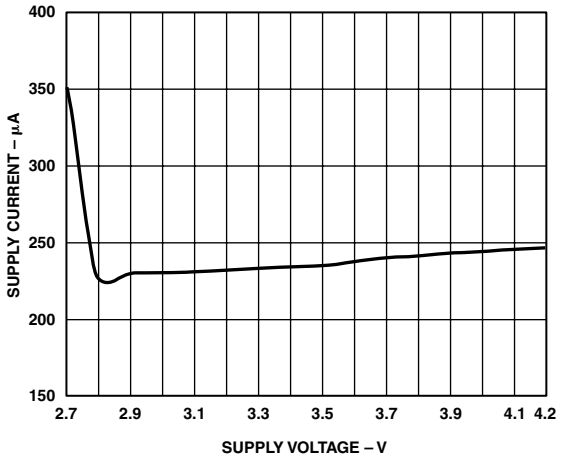
TPC 1. LDO O/P Voltage Variation over Temperature and Supply



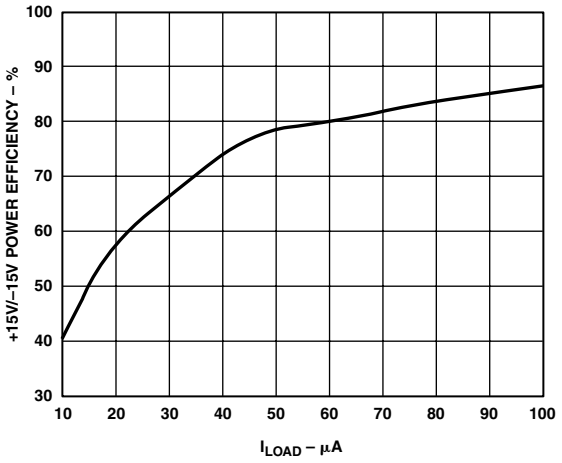
TPC 4. LDO Power Efficiency vs. Load Current, V_{CC} = 3 V



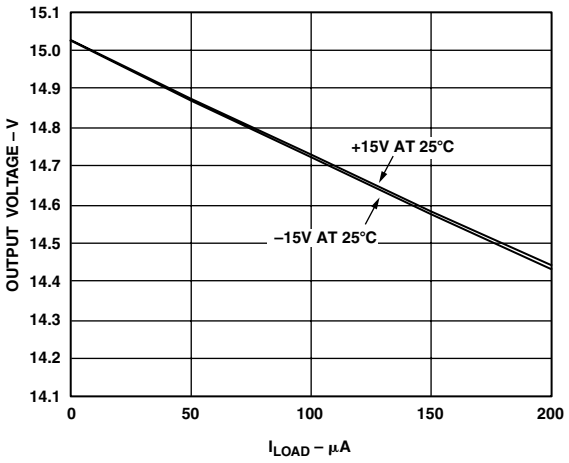
TPC 2. LDO O/P Voltage vs. Load Current



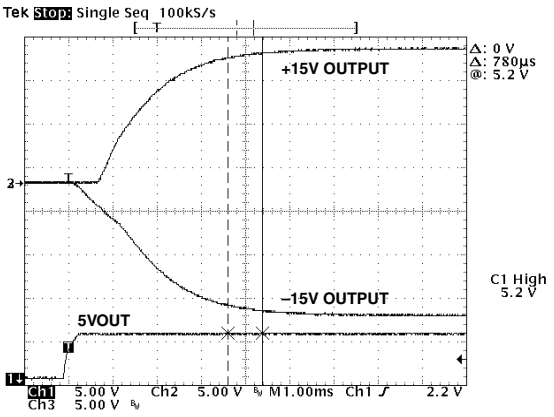
TPC 5. Supply Current vs. Supply Voltage



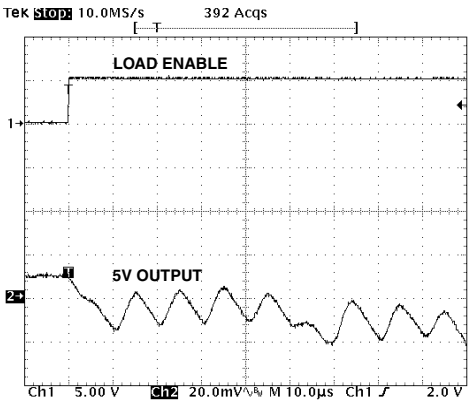
TPC 3. +15 V/–15 V Power Efficiency vs. Load Current



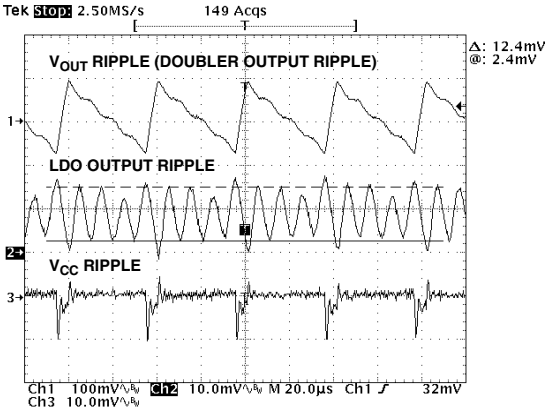
TPC 6. +15 V/–15 V Output Voltage vs. Load Current, Typical Configuration



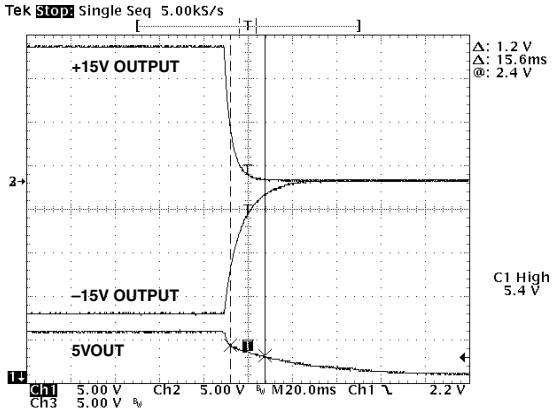
TPC 7. +15 V and –15 V Outputs at Power-Up



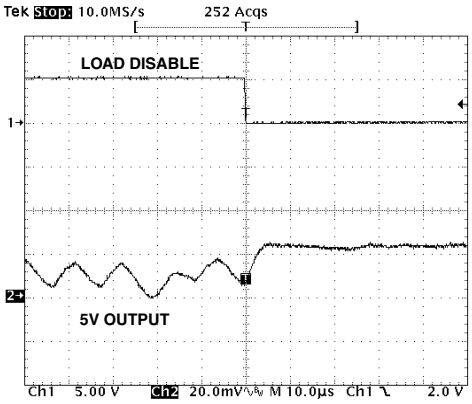
TPC 10. Output Transient Response for Maximum Load Current



TPC 8. Output Ripple on LDO (5 V Output)



TPC 11. +15 V and –15 V Outputs at Power-Down



TPC 9. 5 V Output Transient Response, Load Disconnected

POWER SEQUENCING

In order for the TFT panel to power up correctly, the gate drive supplies must be sequenced such that the –15 V supply is up before the +15 V supply. The ADM8839 controls this sequence. When the device is turned on (a logic high on $\overline{SHDN}$), the ADM8839 allows the –15 V output to ramp immediately but holds off the +15 V output. It continues to do this until the negative output has reached –3 V. At this point, the positive output is enabled and allowed to ramp to +15 V. This sequence is highlighted in Figure 1.

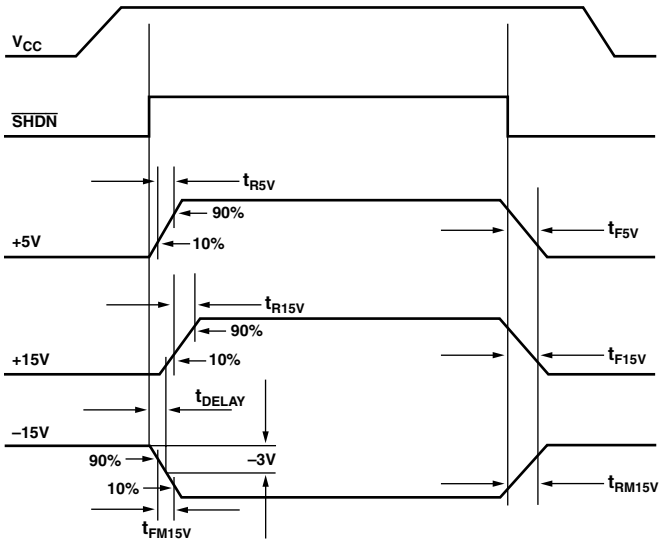


Figure 1. Power Sequence

TRANSIENT RESPONSE

The ADM8839 features extremely fast transient response, making it very suitable for fast image updates on TFT LCD panels. This means that even under changing load conditions, there is still very effective regulation of the 5 V output. TPCs 9 and 10 show how the 5 V output responds when a maximum load is dynamically connected and disconnected. Note that the output settles within 5 µs to less than 1% of the output level.

BOOSTING THE CURRENT DRIVE OF THE ±15 V SUPPLY

The ADM8839 ±15 V output can deliver 150 µA of current in the typical configuration, as shown in Figure 2. It is also possible to draw 100 µA from the +15 V output and 200 µA from the –15 V output, or vice versa. It is possible to draw only a maximum of 300 µA combined from both the +15 V and the –15 V outputs at any time (see Figure 3). In this configuration, +5VOUT (Pin 4) is connected to +5VIN (Pin 5), as shown in the Functional Block Diagram.

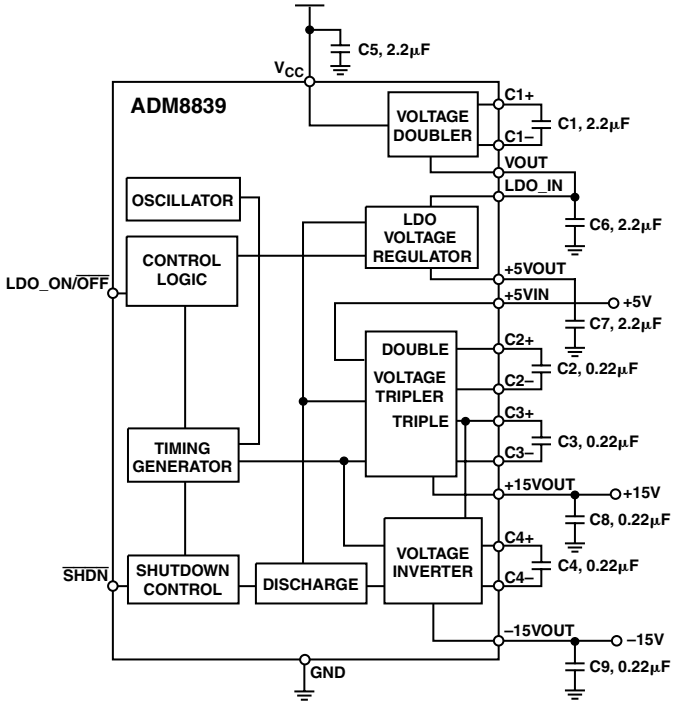


Figure 2. Typical Configuration

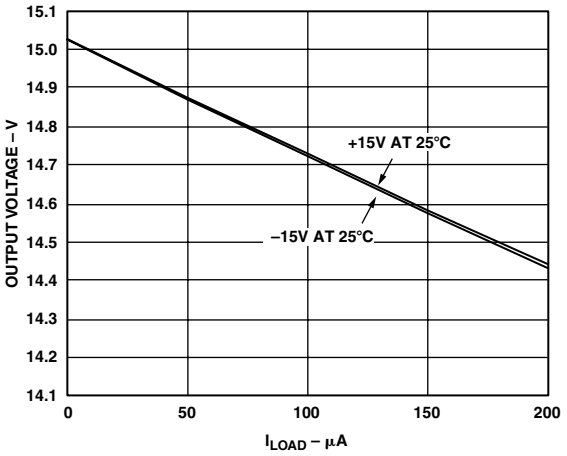


Figure 3. +15 V/–15 V Output Voltage vs. Load Current, Typical Configuration

It is possible to configure the ADM8839 to supply up to 400 µA on the ±15 V outputs by changing its configuration slightly, as shown in Figure 4.

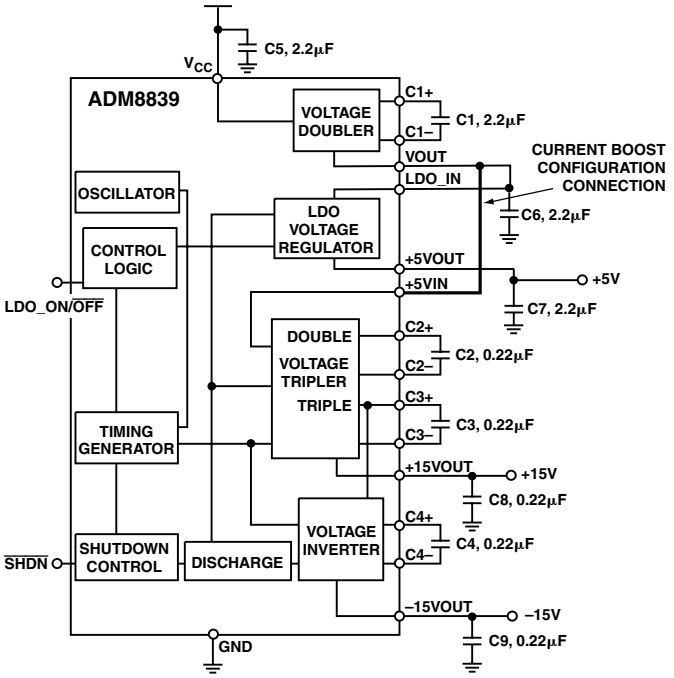


Figure 4. Current Boost Configuration

The configuration in Figure 4 can supply up to 400 µA of current on both the +15 V and the –15 V outputs. If the load on the ±15 V does not draw any current, the voltage on the ±15 V outputs can rise up to ±16.5 V (see Figure 5). In this configuration, VOUT (Pin 2) is connected to +5VIN (Pin 5).

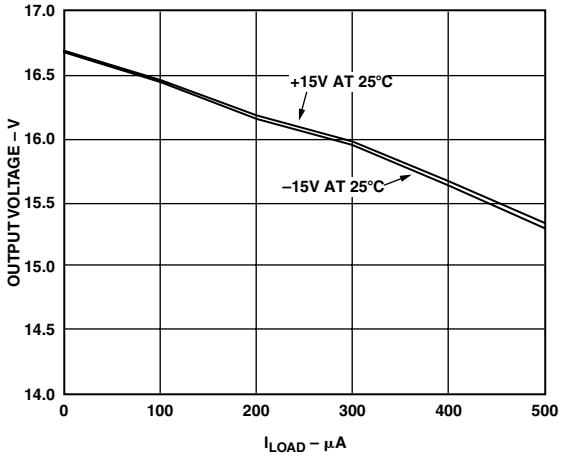
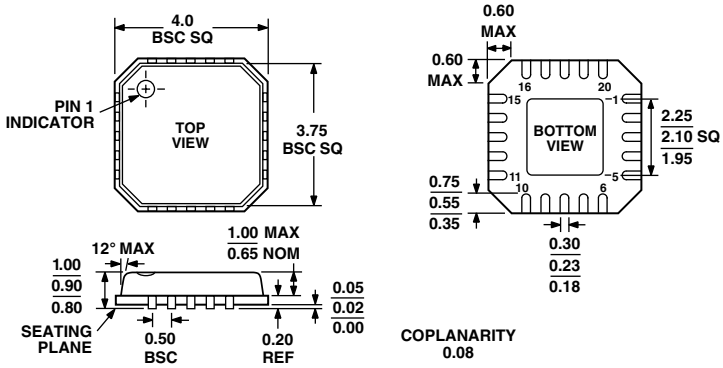


Figure 5. +15 V/–15 V Output Voltage vs. Load Current, Current Boost Configuration

C03075–0–2/03(A)

OUTLINE DIMENSIONS

20-Lead Leadframe Chip Scale Package [LFCSP]
4 × 4 mm Body
(CP-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

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Revision History

2/03 – Data Sheet Changed from Rev. 0 to Rev. A

Changed SPECIFICATIONS 2
Updated OUTLINE DIMENSIONS 8