Data Sheet | October 31, 2002 | FN7288

40MHz Non-Inverting Quad CMOS Driver

élantec

The EL7457 is a high speed, non-inverting, quad CMOS driver. It is capable of running at clock rates up to 40MHz and features 2A peak drive capability and a nominal on-resistance of just 3Ω. The EL7457 is ideal for driving highly capacitive loads, such as storage and vertical clocks in CCD applications. It is also well suited to ATE pin driving, level-shifting, and clock-driving applications.

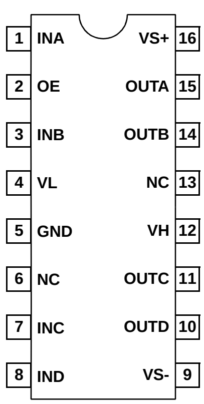
The EL7457 is capable of running from single or dual power supplies while using ground referenced inputs. Each output can be switched to either the high (V_H) or low (V_L) supply pins, depending on the related input pin. The inputs are compatible with both 3V and 5V CMOS and TTL logic. The output enable (OE) pin can be used to put the outputs into a high-impedance state. This is especially useful in CCD applications, where the driver should be disabled during power down.

The EL7457 also features very fast rise and fall times which are matched to within 1ns. The propagation delay is also matched between rising and falling edges to within 2ns.

The EL7457 is available in both 16-pin QSOP and 16-pin SO (0.150") packages. It is specified for operation over the full -40°C to +85°C temperature range.

Pinout

EL7457
[16-PIN SO (0.150"), QSOP]
TOP VIEW



Features

- Clocking speeds up to 40MHz
- 4 channels
- 12ns tr/tf at 1000pF C_{LOAD}
- 1ns rise and fall time match
- 1.5ns prop delay match
- Low quiescent current - <1mA
- Fast output enable function - 12ns
- Wide output voltage range
- $8V \geq V_L \geq -5V$
- $-2V \leq V_H \leq 15V$
- 2A peak drive
- 3Ω on resistance
- Input level shifters
- TTL/CMOS input-compatible

Applications

- CCD drivers
- Digital cameras
- Pin drivers
- Clock/line drivers
- Ultrasound transducer drivers
- Ultrasonic and RF generators
- Level shifting

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. NO.
EL7457CU	16-Pin QSOP	-	MDP0040
EL7457CU-T13	16-Pin QSOP	13”	MDP0040
EL7457CS	16-Pin SO (0.150”)	-	MDP0027
EL7457CS-T7	16-Pin SO (0.150”)	7”	MDP0027
EL7457CS-T13	16-Pin SO (0.150”)	13”	MDP0027

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S+ to V_S-) . . . . +16.5V
Input Voltage . . . . V_S- -0.3V, V_S+ +0.3V
Continuous Output Current 100mA
Storage Temperature Range . . . . -65°C to +150°C
Ambient Operating Temperature . . . . -40°C to +85°C
Maximum Die Temperature . . . . +125°C
Power Dissipation . . . . See Curves
Maximum ESD. 2kV

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, V_H = +5V, V_L = -5V, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT						
V_{IH}	Logic “1” Input Voltage		2.0			V
I_{IH}	Logic “1” Input Current	V_{IH} = 5V		0.1	10	µA
V_{IL}	Logic “0” Input Voltage				0.8	V
I_{IL}	Logic “0” Input Current	V_{IL} = 0V		0.1	10	µA
C_{IN}	Input Capacitance			3.5		pF
R_{IN}	Input Resistance			50		MΩ
OUTPUT						
R_{OH}	ON Resistance V_H to OUTx	I_{OUT} = -100mA		4.5	6	Ω
R_{OL}	ON Resistance V_L to OUTx	I_{OUT} = +100mA		4	6	Ω
I_{LEAK}	Output Leakage Current	V_H = V_S+, V_L = V_S-		0.1	10	µA
I_{PK}	Peak Output Current	Source		2.0		A
		Sink		2.0		A
POWER SUPPLY						
I_S	Power Supply Current	Inputs = V_S+		0.5	1.5	mA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	C_L = 1000pF		13.5		ns
t_F	Fall Time	C_L = 1000pF		13		ns
$t_{RF\Delta}$	t_R, t_F Mismatch	C_L = 1000pF		0.5		ns
t_D+	Turn-Off Delay Time	C_L = 1000pF		12.5		ns
t_D-	Turn-On Delay Time	C_L = 1000pF		14.5		ns
t_{DD}	t_{D-1} - t_{D-2} Mismatch	C_L = 1000pF		2		ns
t_{ENABLE}	Enable Delay Time			12		ns
$t_{DISABLE}$	Disable Delay Time			12		ns

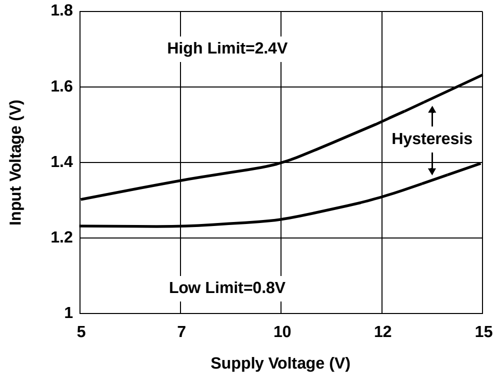
Electrical Specifications

$V_S+ = +15V$, $V_S- = 0V$, $V_H = +15V$, $V_L = 0V$, $T_A = 25°C$, unless otherwise specified

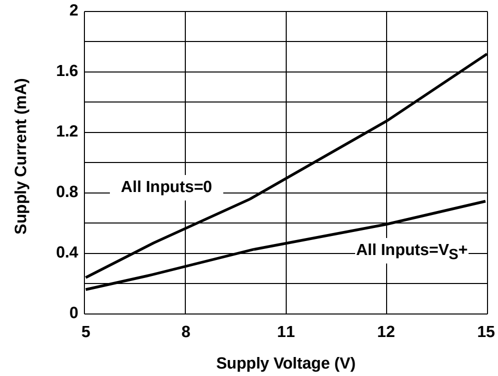
PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT						
V_{IH}	Logic “1” Input Voltage		2.4			V
I_{IH}	Logic “1” Input Current	$V_{IH} = 5V$		0.1	10	µA
V_{IL}	Logic “0” Input Voltage				0.8	V
I_{IL}	Logic “0” Input Current	$V_{IL} = 0V$		0.1	10	µA
C_{IN}	Input Capacitance			3.5		pF
R_{IN}	Input Resistance			50		MΩ
OUTPUT						
R_{OH}	ON Resistance V_H to OUT	$I_{OUT} = -100mA$		3.5	5	Ω
R_{OL}	ON Resistance V_L to OUT	$I_{OUT} = +100mA$		3	5	Ω
I_{LEAK}	Output Leakage Current	$V_H = V_S+$, $V_L = V_S-$		0.1	10	µA
I_{PK}	Peak Output Current	Source		2.0		A
		Sink		2.0		A
POWER SUPPLY						
I_S	Power Supply Current	Inputs = V_S+		0.8	2	mA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	$C_L = 1000pF$		11		ns
t_F	Fall Time	$C_L = 1000pF$		12		ns
$t_{RF\Delta}$	t_R, t_F Mismatch	$C_L = 1000pF$		1		ns
t_D+	Turn-Off Delay Time	$C_L = 1000pF$		11.5		ns
t_D-	Turn-On Delay Time	$C_L = 1000pF$		13		ns
t_{DD}	t_{D-1} - t_{D-2} Mismatch	$C_L = 1000pF$		1.5		ns
t_{ENABLE}	Enable Delay Time			12		ns
$t_{DISABLE}$	Disable Delay Time			12		ns

Typical Performance Curves

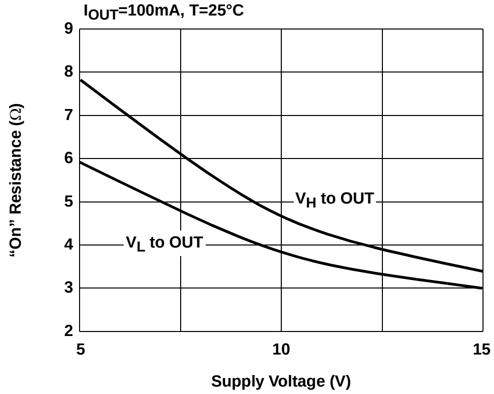
Switch Threshold vs Supply Voltage
T=25°C



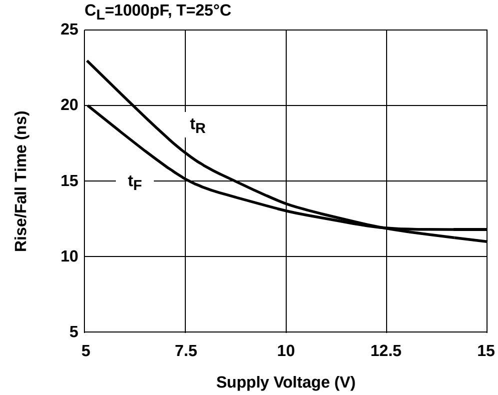
Quiescent Supply Current vs Supply Voltage
T=25°C



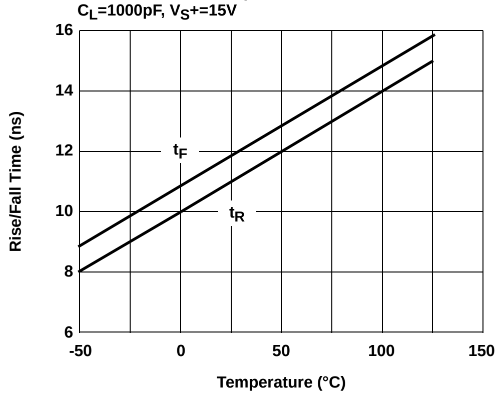
"On" Resistance vs Supply Voltage
I_{OUT}=100mA, T=25°C



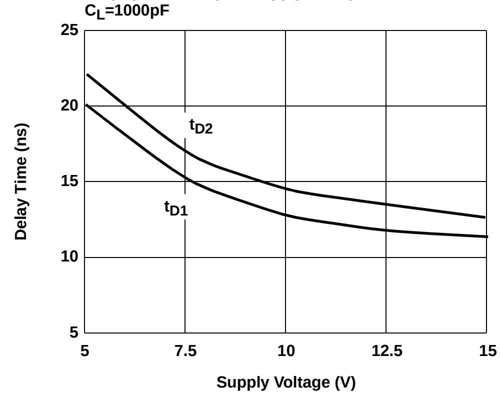
Rise/Fall Time vs Supply Voltage
C_L=1000pF, T=25°C



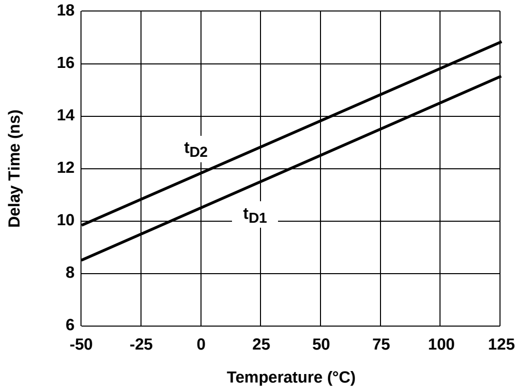
Rise/Fall Time vs Temperature
C_L=1000pF, V_S+=15V



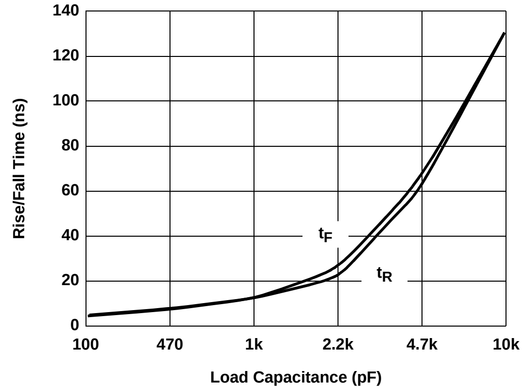
Propagation Delay vs Supply Voltage
C_L=1000pF



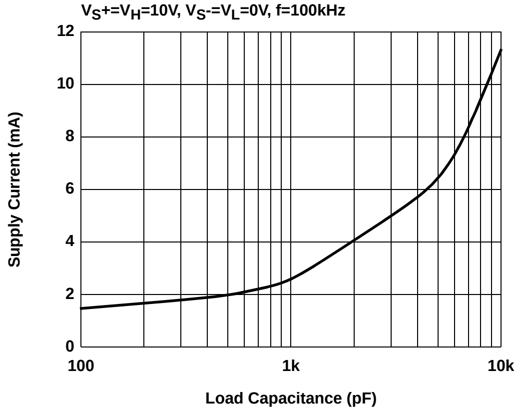
Typical Performance Curves (Continued)



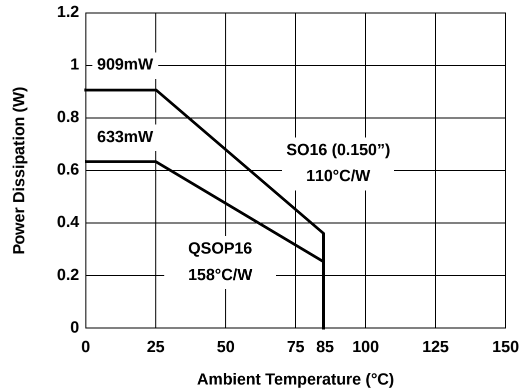
Propagation Delay vs Temperature
C_L=1000pF, V_S+=15V



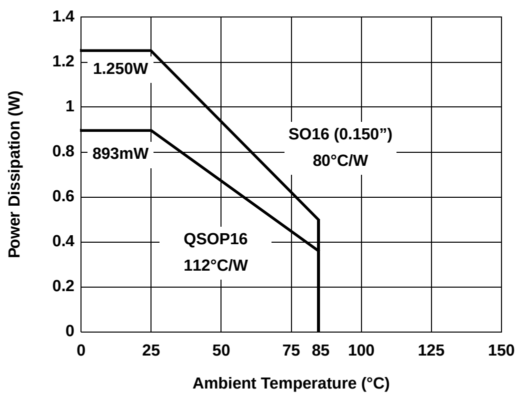
Rise/Fall Time vs Load
V_S+=15V



Supply Current Per Channel vs Capacitive Load
V_S+=V_H=10V, V_S-=V_L=0V, f=100kHz



Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-3 Low Effective Thermal Conductivity Test Board

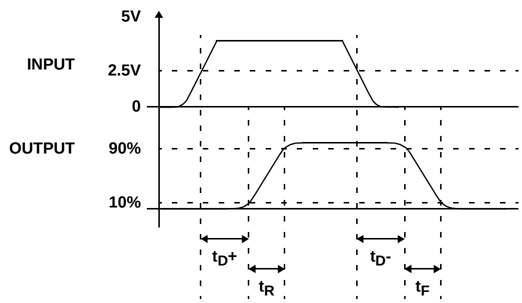


Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-7 High Effective Thermal Conductivity Test Board

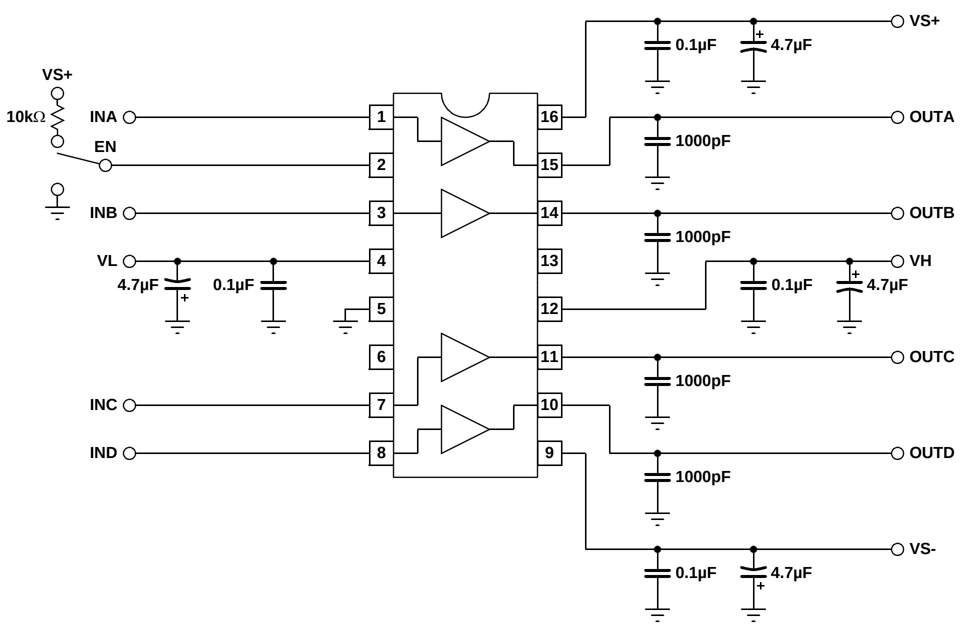
Nominal Operating Voltage Range

PIN	MIN	MAX
V_S+ to V_S-	5V	15V
V_S- to GND	-5V	0V
V_H	V_S- + 2.5V	V_S+
V_L	V_S-	V_S+
V_H to V_L	0V	15V
V_L to V_S-	0V	8V

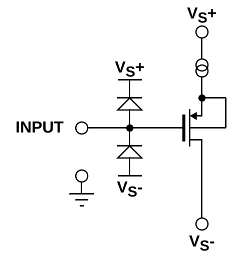
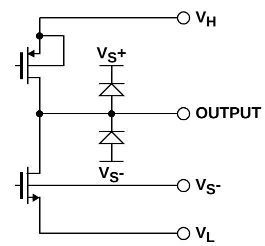
Timing Diagram



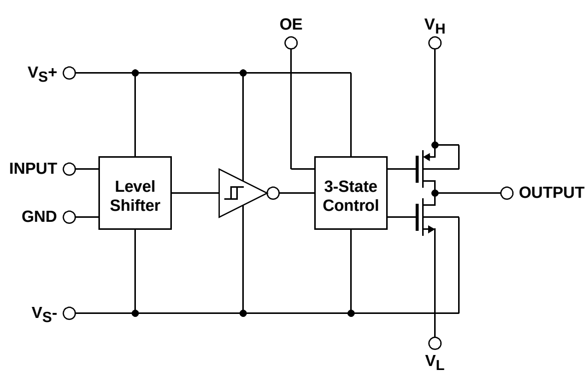
Standard Test Configuration



Pin Descriptions

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
1	INA	Input channel A	 Circuit 1
2	OE	Output Enable	(Reference Circuit 1)
3	INB	Input channel B	(Reference Circuit 1)
4	VL	Low voltage input pin	
5	GND	Input logic ground	
6	NC	No connection	
7	INC	Input channel C	(Reference Circuit 1)
8	IND	Input channel D	(Reference Circuit 1)
9	VS-	Negative supply voltage	
10	OUTD	Output channel D	 Circuit 2
11	OUTC	Output channel C	(Reference Circuit 2)
12	VH	High voltage input pin	
13	NC	No connection	
14	OUTB	Output channel B	(Reference Circuit 2)
15	OUTA	Output channel A	(Reference Circuit 2)
16	VS+	Positive supply voltage	

Block Diagram



Applications Information

Product Description

The EL7457 is a high performance 40MHz high speed quad driver. Each channel of the EL7457 consists of a single P-channel high side driver and a single N-channel low side driver. These 3Ω devices will pull the output (OUT_X) to either the high or low voltage, on V_H and V_L respectively, depending on the input logic signal (IN_X). It should be noted that there is only one set of high and low voltage pins.

A common output enable (OE) pin is available on the EL7457. This pin, when pulled low will put all outputs in to the high impedance state.

The EL7457 is available in both the 16-pin SO (0.150") and the space saving 16-pin QSOP packages. The relevant package should be chosen depending on the calculated power dissipation.

Supply Voltage Range and Input Compatibility

The EL7457 is designed for operation on supplies from 5V to 15V with 10% tolerance (i.e. 4.5V to 16.5V). The table on page 6 shows the specifications for the relationship between the V_S+, V_S-, V_H, V_L, and GND pins. The EL7457 does not contain a true analog switch and therefore V_L should always be less than V_H.

All input pins are compatible with both 3V and 5V CMOS signals With a positive supply (V_S+) of 5V, the EL7457 is also compatible with TTL inputs.

Power Supply Bypassing

When using the EL7457, it is very important to use adequate power supply bypassing. The high switching currents developed by the EL7457 necessitate the use of a bypass capacitor on both the positive and negative supplies. It is recommended that a 4.7µF tantalum capacitor be used in parallel with a 0.1µF low-inductance ceramic MLC capacitor. These should be placed as close to the supply pins as possible. It is also recommended that the V_H and V_L pins have some level of bypassing, especially if the EL7457 is driving highly capacitive loads.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the EL7457 drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below T_{JMAX} (125°C). It is necessary to calculate the power dissipation for a given application prior to selecting package type.

Power dissipation may be calculated:

$$PD = (V_S \times I_S) + \sum_{1}^{4}(C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)$$

where:

V_S is the total power supply to the EL7457 (from V_S+ to V_S-)

V_{OUT} is the swing on the output (V_H - V_L)

C_L is the load capacitance

C_{INT} is the internal load capacitance (80pF max)

I_S is the quiescent supply current (3mA max)

f is frequency

Having obtained the application's power dissipation, the maximum junction temperature can be calculated:

$$T_{JMAX} = T_{MAX} + \Theta_{JA} \times PD$$

where:

T_{JMAX} is the maximum junction temperature (125°C)

T_{MAX} is the maximum ambient operating temperature

PD is the power dissipation calculated above

θ_{JA} is the thermal resistance, junction to ambient, of the application (package + PCB combination). Refer to the Package Power Dissipation curves on page 5.