Charge Pump Regulator for Color TFT Panel

ADM8830

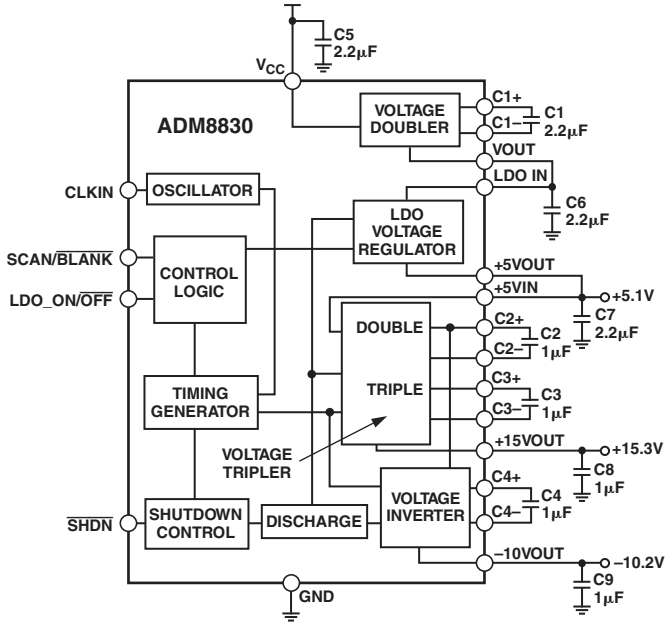
FEATURES

- 3 Output Voltages (+5.1 V, +15.3 V, –10.2 V) from One 3 V Input Supply
- Power Efficiency Optimized for Use with TFT in Mobile Phones
- Low Quiescent Current
- Low Shutdown Current (<1 μA)
- Fast Transient Response
- Shutdown Function
- Power Saving during Blanking Period
- Option to Use External LDO

APPLICATIONS

- Handheld Instruments
- TFT LCD Panels
- Cellular Phones

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM8830 is a charge pump regulator used for color thin film transistor (TFT) liquid crystal displays (LCD). Using charge pump technology, the device can be used to generate three output voltages (+5.1 V ± 2%, +15.3 V ± 4%, –10.2 V ± 4%) from a single 3 V input supply. These outputs are then used to provide supplies for the LCD controller (5.1 V) and the gate drives for the transistors in the panel (+15.3 V and –10.2 V). Only a few external capacitors are needed for the charge pumps. An efficient low dropout voltage regulator also ensures that the power efficiency is high and provides a low ripple 5.1 V output. This LDO can be shut down and an external LDO used to regulate the 5 V doubler output and drive the input to the charge pump section, which generates the +15.3 V and –10.2 V outputs if so required by the user.

The ADM8830 has an internal 100 kHz oscillator for use in scanning mode, but the part must be clocked by an external clock source in blanking (low current) mode. The internal oscillator is used to clock the charge pumps during scanning mode where the current is highest. During blanking periods, the ADM8830 switches to use an external, lower frequency clock. This allows the user to vary the frequency and maximize power efficiency during blanking periods. The tolerances on the output voltages are seamlessly maintained when switching from scanning mode to blanking mode or vice versa.

The ADM8830 has a number of power saving features, including low power shutdown and reduced quiescent current consumption during the blanking periods mentioned above. The 5.1 V output consumes the most power, so power efficiency is also maximized on this output with an oscillator enabling scheme (Green Idle™). This effectively senses the load current that is flowing and turns on the charge pump only when charge needs to be delivered to the 5 V pump doubler output.

The ADM8830 is fabricated using CMOS technology for minimal power consumption. The part is packaged in 20-lead LFCSP (lead frame chip scale package) and TSSOP packages.

REV. A

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ADM8830–SPECIFICATIONS

(V_{CC} = 2.6 V to 3.6 V, T_A = –40°C to +85°C, unless otherwise noted, C1, C5, C6, C7 = 2.2 μF, C2, C3, C4, C8, C9 = 1 μF, CLKIN = 1 kHz in Blanking Mode.)

Parameter	Min	Typ	Max	Unit	Test Conditions
INPUT VOLTAGE, V_{CC}	2.6		3.6	V	
SUPPLY CURRENT, I_{CC}		150	400	μA	Unloaded, Scanning Period
		70	140	μA	Unloaded, Blanking Period
			1	μA	Shutdown Mode, T_A = 25°C
+5.1 V OUTPUT					
Output Voltage	5.0	5.1	5.2	V	I_L = 10 μA to 8 mA
Output Current		4	5	mA	Scanning Period
		5	8	mA	Scanning Period, V_{CC} > 2.7 V
		50	200	μA	Blanking Period
Power Efficiency		80		%	V_{CC} = 3 V, I_L = 5 mA (Scanning)
		70		%	V_{CC} = 3 V, I_L = 200 μA (Blanking)
Output Ripple		10		mV p-p	8 mA Load
Transient Response		5		μs	I_L Stepped from 10 μA to 8 mA
+15.3 V OUTPUT					
Output Voltage	14.4	15.3	15.6	V	I_L = 1 μA to 100 μA
Output Current		50	100	μA	Scanning Period
		1	10	μA	Blanking Period
Output Ripple		50		mV p-p	I_L = 100 μA
–10.2 V OUTPUT					
Output Voltage	–10.4	–10.2	–9.6	V	I_L = –1 μA to –100 μA
Output Current	–100	–50		μA	Scanning Period
	–10	–1		μA	Blanking Period
Output Ripple		50		mV p-p	I_L = –100 μA
POWER EFFICIENCY		90		%	Relative to 5.1 V Output, I_L = 100 μA (Scanning)
(+15.3 V and –10.2 V Outputs)		80		%	Relative to 5.1 V Output, I_L =10 μA (Blanking)
CHARGE PUMP FREQUENCY	60	100	140	kHz	Scanning Period
CONTROL PINS					
$\overline{SHDN}$					
Input Voltage, V_{SHDN}			0.3 V_{CC}	V	$\overline{SHDN}$ Low = Shutdown Mode
	0.7 V_{CC}			V	$\overline{SHDN}$ High = Normal Mode
Digital Input Current			±1	μA	
Digital Input Capacitance*			10	pF	
SCAN/$\overline{BLANK}$					
Input Voltage			0.3 V_{CC}	V	Low = $\overline{BLANK}$ Period
	0.7 V_{CC}			V	High = SCAN Period
Digital Input Current			±1	μA	
Digital Input Capacitance*			10	pF	
LDO_ON/$\overline{OFF}$					
Input Voltage			0.3 V_{CC}	V	Low = External LDO
	0.7 V_{CC}			V	High = Internal LDO
Digital Input Current			±1	μA	
Digital Input Capacitance*			10	pF	
CLKIN					
Minimum Frequency	0.9	1		kHz	Duty Cycle = 50%, Rise/Fall Times = 20 ns
Input Voltage					
V_{IL}			0.3 V_{CC}	V	
V_{IH}	0.7 V_{CC}			V	
Digital Input Current			±1	μA	
Digital Input Capacitance*			10	pF	

*Guaranteed by design. Not 100% production tested.

Specifications are subject to change without notice.

TIMING SPECIFICATIONS

(V_{CC} = 2.6 V to 3.6 V, T_A = –40°C to +85°C, unless otherwise noted, C1, C5, C6, C7 = 2.2 μF, C2, C3, C4, C8, C9 = 1 μF, CLKIN = 1 kHz in Blanking Mode.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-UP SEQUENCE					
+5 V Rise Time, t_{R5V}		300		μs	10% to 90%, Figure 2
+15 V Rise Time, t_{R15V}		8		ms	10% to 90%, Figure 2
–10 V Fall Time, t_{F10V}		12		ms	90% to 10%, Figure 2
Delay between –10 V Fall and +15 V, t_{DELAY}		3		ms	Figure 2
POWER-DOWN SEQUENCE					
+5 V Fall Time, t_{F5V}		75		ms	90% to 10%, Figure 2
+15 V Fall Time, t_{F15V}		40		ms	90% to 10%, Figure 2
–10 V Rise Time, t_{R10V}		40		ms	10% to 90%, Figure 2

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

Supply Voltage . . . . . –0.3 V to +4.0 V
Input Voltage to Digital Inputs . . . . . –0.3 V to +4.0 V
Output Short Circuit Duration to GND . . . . . 10 sec
Output Voltage
+5.1 V Output . . . . . –0.3 V to +6 V
–10.2 V Output . . . . . –12 V to +0.3 V
+15.3 V Output . . . . . –0.3 V to +17 V
Operating Temperature Range . . . . . –40°C to +85°C
Power Dissipation . . . . . 3.55 W
(Derate 33 mW/°C above 25°C)
Storage Temperature Range . . . . . –65°C to +150°C
ESD . . . . . Class I

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

THERMAL CHARACTERISTICS

20-Lead TSSOP Package:
θ_{JA} = 72°C/W
20-Lead LFCSP Package:
θ_{JA} = 31°C/W

ORDERING GUIDE

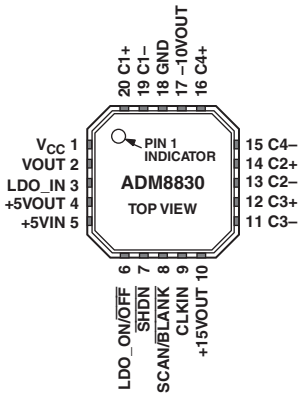
Model	Temperature Range	Package Description	Package Option
ADM8830ACP	–40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADM8830ARU	–40°C to +85°C	Thin Shrink Small Outline Package	RU-20

CAUTION

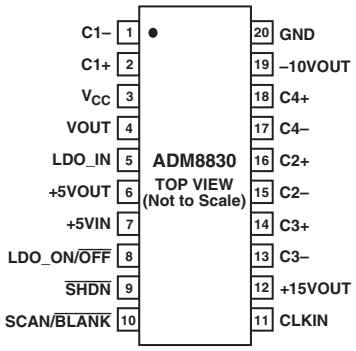
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM8830 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

LFCSP

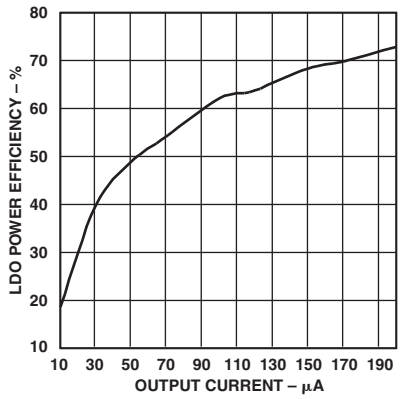


TSSOP

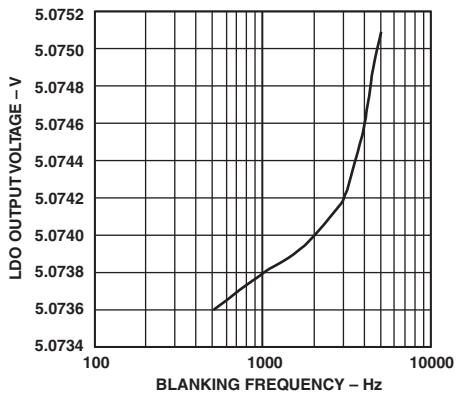


PIN FUNCTION DESCRIPTIONS

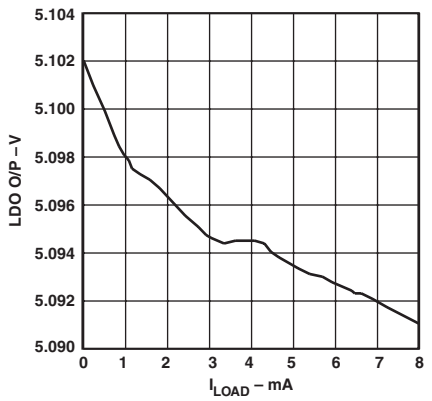
Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Function**
1, 2	19, 20	C1–, C1+	External capacitor C1 is connected between these pins. A 2.2 µF capacitor is recommended.
3	1	V_{CC}	Positive Supply Voltage Input. Connect this pin to 3 V supply with a 2.2 µF decoupling capacitor.
4	2	VOUT	Voltage Doubler Output. This is derived by doubling the 3 V supply. A 2.2 µF capacitor to ground is required on this pin.
5	3	LDO_IN	Voltage Regulator Input. The user has the option to bypass this circuit using the LDO_ON/$\overline{\text{OFF}}$ pin.
6	4	+5VOUT	+5.1 V Output Pin. This is derived by doubling and regulating the +3 V supply. A 2.2 µF capacitor to ground is required on this pin to stabilize the regulator.
7	5	+5VIN	+5.1 V Input Pin. This is the input to the voltage tripler and doubler inverter charge pump circuits.
8	6	LDO_ON/$\overline{\text{OFF}}$	Control Logic Input. 3 V CMOS logic. A logic high selects the internal LDO for regulation of the 5 V voltage doubler output. A logic low isolates the internal LDO from the rest of the charge pump circuits. This allows the use of an external LDO to regulate the 5 V voltage doubler output. The output of this LDO is then fed back into the voltage tripler and doubler/inverter circuits of the ADM8830.
9	7	$\overline{\text{SHDN}}$	Digital Input. 3 V CMOS logic. Active low shutdown control. This shuts down the timing generator and enables the discharge circuit to dissipate the charge on the voltage outputs, thus driving them to 0 V.
10	8	SCAN/$\overline{\text{BLANK}}$	Drive Mode Input. 3 V CMOS logic. A logic high places the part in scan (high current) mode and the charge pump is driven by the internal oscillator. A logic low places the part in blanking (low current) mode and the charge pump is driven by the (slower) external oscillator. This is a power saving feature on the ADM8830.
11	9	CLKIN	External CLOCK Input. During a blanking period, the oscillator circuit selects this pin to drive the charge pump circuit. This is at a lower frequency than the internal oscillator, resulting in lower quiescent current consumption, thus saving power.
12	10	+15VOUT	+15.3 V Output Pin. This is derived by tripling the +5.1 V regulated output. A 1 µF capacitor is required on this pin.
13, 14	11, 12	C3–, C3+	External capacitor C3 is connected between these pins. A 1 µF capacitor is recommended.
15, 16	13, 14	C2–, C2+	External capacitor C2 is connected between these pins. A 1 µF capacitor is recommended.
17, 18	15, 16	C4–, C4+	External capacitor C4 is connected between these pins. A 1 µF capacitor is recommended.
19	17	–10VOUT	–10.2 V Output Pin. This is derived by doubling and inverting the +5.1 V regulated output. A 1 µF capacitor is required on this pin.
20	18	GND	Device Ground Pin.



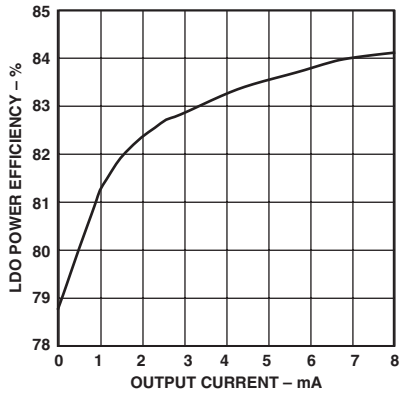
TPC 1. LDO Efficiency in Blanking Mode with V_{CC} = 3 V



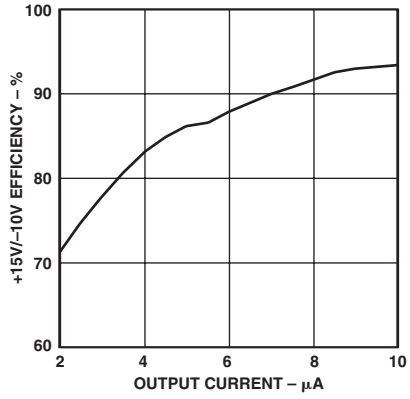
TPC 2. LDO Output Voltage (Unloaded) vs. Blanking Mode Frequency



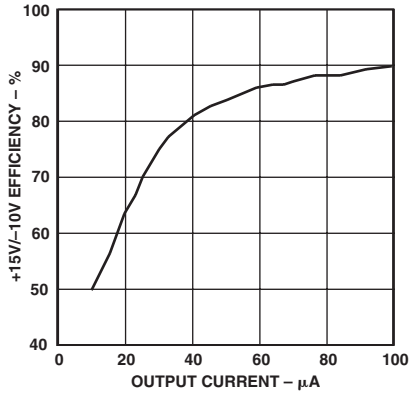
TPC 3. LDO O/P Voltage vs. Load Current in Scanning Mode, V_{CC} = 3.3 V



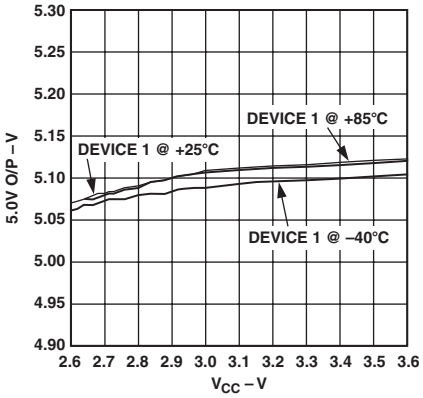
TPC 4. LDO Efficiency in Scanning Mode with V_{CC} = 3 V



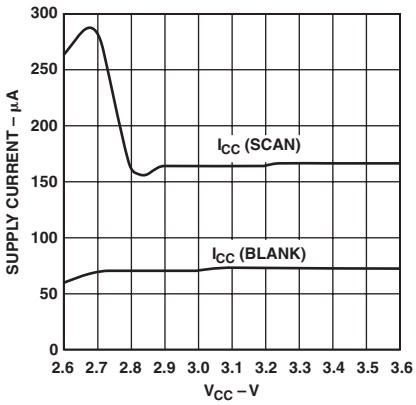
TPC 5. +15 V/–10 V Efficiency vs. Output Current in Blanking Mode, V_{CC} = 3 V



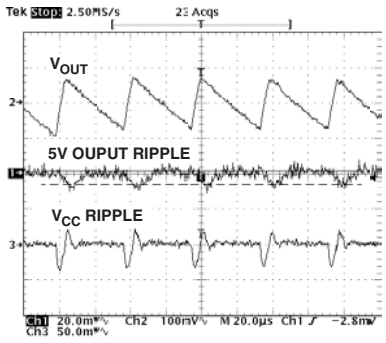
TPC 6. +15 V/–10 V Efficiency vs. Output Current in Scanning Mode, V_{CC} = 3 V



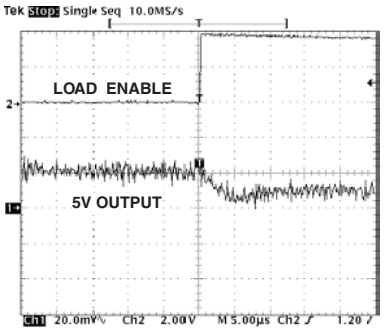
TPC 7. LDO Variation over Supply and Temperature



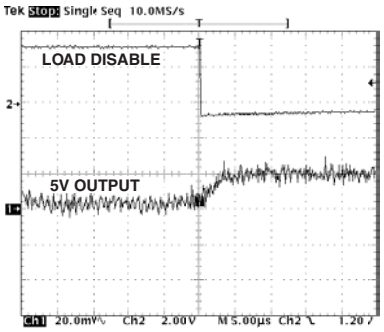
TPC 8. Supply Current vs. Voltage



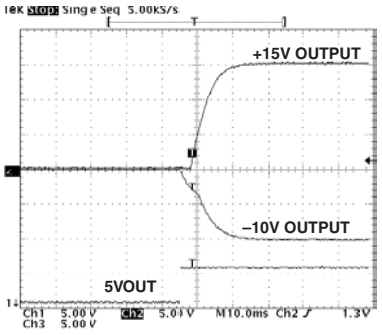
TPC 9. Output Ripple on LDO (5 V Output)



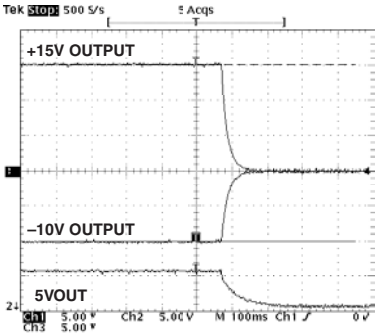
TPC 10. 5 V Output Transient Response for Max Load Current



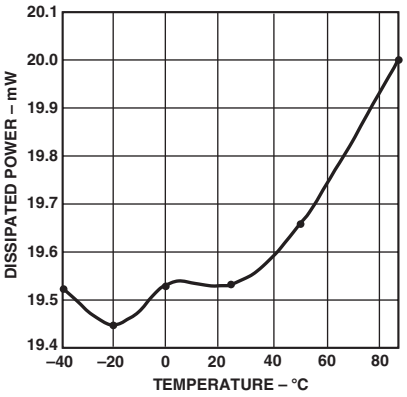
TPC 11. 5 V Output Transient Response, Load Disconnected



TPC 12. +15 V and –10 V Outputs at Power-Up



TPC 13. +15 V and –10 V Outputs at Power-Down (Unloaded)



TPC 14. Power Dissipation over Temperature, V_{CC} = 3.6 V, Scanning Mode with All O/Ps at Maximum Load

SCANNING AND BLANKING

A TFT LCD panel is essentially made up of a bank of capacitors, each representing a pixel in the display. These capacitors store different levels of charge, depending on the amount of luminescence required for a given pixel. When a picture is being displayed on the panel, a scan of all the pixel capacitors is performed, placing different levels of charge on each in order to create the image. The process of updating the display like this is called "scanning." Once scanned, an image will be held by pixel capacitance and the controller and source line drivers can be put into a low power mode. This low power mode is referred to as the blanking mode on the ADM8830. Over a finite period of time, this pixel charge will leak and the capacitors will have to be refreshed in order to maintain the image.

The ADM8830 caters to the two modes of operation described above as follows. When the TFT LCD panel is in scanning mode, a logic high on the SCAN/$\overline{\text{BLANK}}$ input places the device in high current power mode, providing extra power (extra current) to the LCD controller and the source line drivers. If the panel continues to be updated (as when a moving picture is being displayed), then the ADM8830 can be continually operated in scanning mode. If the same image is kept on the panel, a logic low is applied to the SCAN/$\overline{\text{BLANK}}$ input and the ADM8830 enters blanking (low current) mode. Depending on how often the image is being updated, the ADM8830 can be operated with a variable SCAN/$\overline{\text{BLANK}}$ duty cycle. This helps to maximize power efficiency and therefore extends the battery life.

POWER SEQUENCING

The gate drive supplies must be sequenced such that the –10 V supply is up before the +15 V supply for the TFT panel to power up correctly. The ADM8830 controls this sequence. When the device is turned on (a logic high on $\overline{\text{SHDN}}$), the ADM8830 allows the –10 V output to ramp immediately but holds off the +15 V output. It continues to do this until the negative output has reached –3 V. At this point, the positive output is enabled and allowed to ramp up to +15 V. This sequence is highlighted in Figure 2.

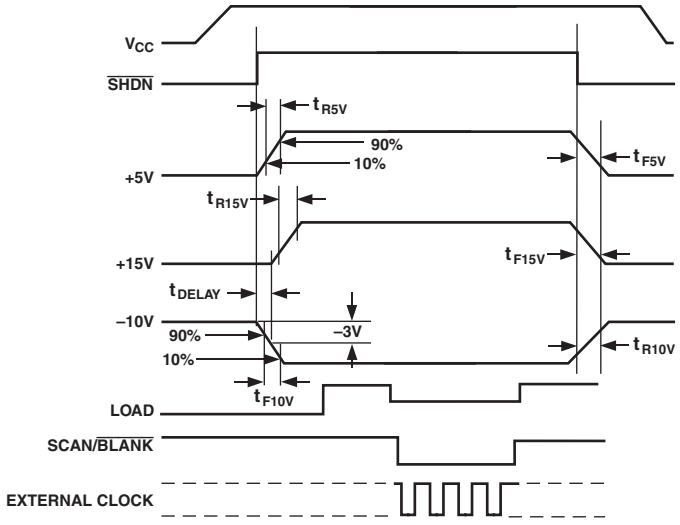


Figure 2. Power Sequence

TRANSIENT RESPONSE

The ADM8830 features extremely fast transient response, making it very suitable for fast image updates on TFT LCD panels. This means that even under changing load conditions there is still very effective regulation of the 5 V output. TPCs 10 and 11 show how the 5.1 V output responds when a maximum load is dynamically connected and disconnected. Note that the output settles within 5 μs to less than 1% of the output level.

EXTERNAL CLOCK

The ADM8830 has an internal 100 kHz oscillator, but an external clock source can also be used to clock the part. This clock source must be applied to the CLKIN pin. Power is saved during blanking periods by disabling the internal oscillator and switching to the lower frequency external clock source. To achieve optimum performance of the charge pump circuitry, it is important that the duty cycle of the external clock source be 50% and that the rise and fall times be less than 20 ns.

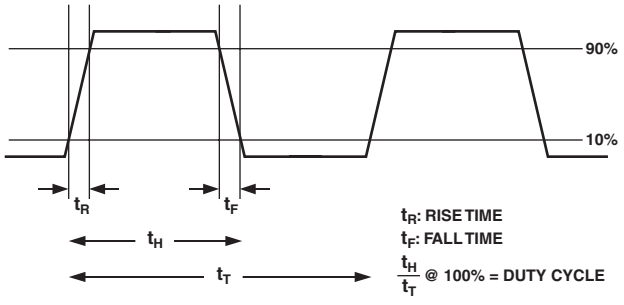


Figure 1. Duty Cycle of External Clock

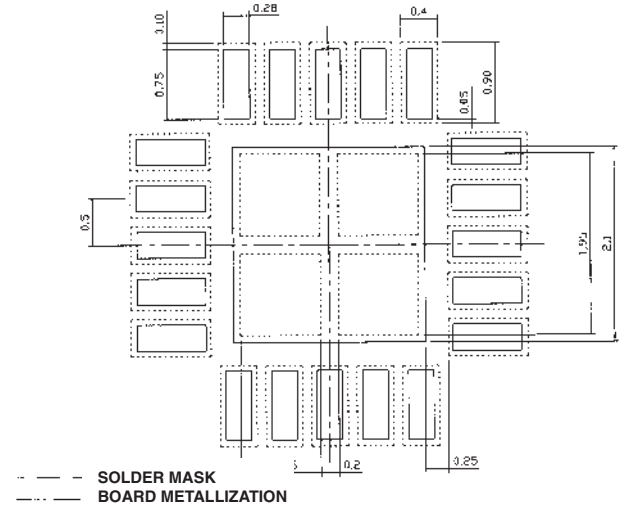
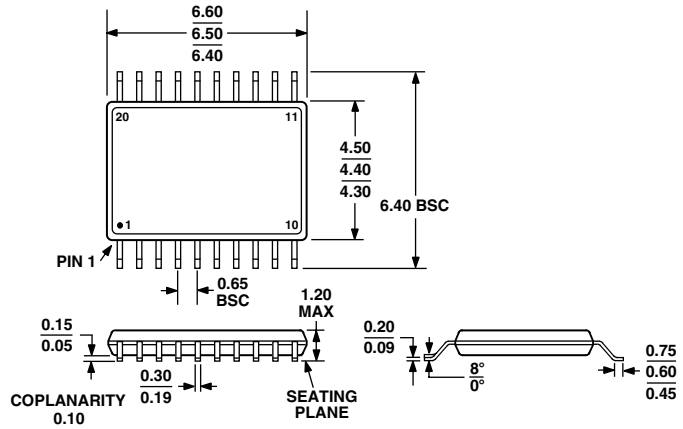


Figure 3. Suggested LFCSP 4 × 4 20-Lead Land Pattern

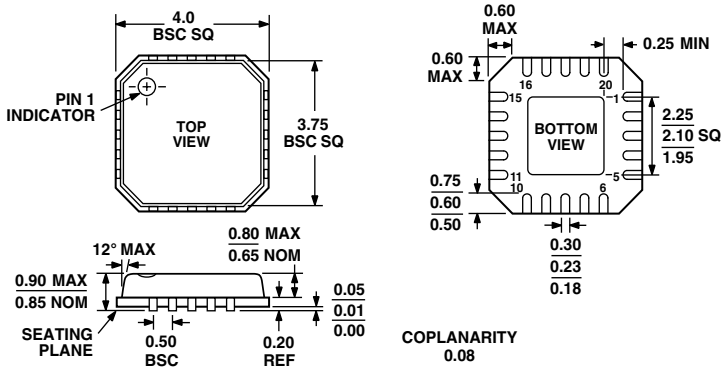
OUTLINE DIMENSIONS

20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-153AC

20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body
(CP-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Revision History

Location	Page
3/03—Data Sheet changed from REV. SpA to REV. A.	
Edits to SPECIFICATIONS	2
Edits to TPC 12 and TPC 13	6
11/02—Data Sheet changed from REV. 0 to REV. SpA.	
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	3
Changes to THERMAL CHARACTERISTICS	3
Edits to captions of TPCs 2, 3, and 6	5
Edits to caption of TPC 13	6
Added TPC 14	6
OUTLINE DIMENSIONS updated	8

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