



# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

MAX9312/MAX9314

## General Description

The MAX9312/MAX9314 are low skew, dual 1-to-5 differential drivers designed for clock and data distribution. These devices accept two inputs. Each input is reproduced at five differential outputs. The differential inputs can be adapted to accept single-ended inputs by connecting the on-chip  $V_{BB}$  supply to one input as a reference voltage.

The MAX9312/MAX9314 feature low part-to-part skew (30ps) and output-to-output skew (12ps), making them ideal for clock and data distribution across a backplane or a board. For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

The MAX9312 features an on-chip  $V_{BB}$  reference output of 1.425V below the positive supply voltage. The MAX9314 offers an on-chip  $V_{BB}$  reference output of 1.32V below the positive supply voltage.

Both devices are offered in space-saving, 32-pin 5mm x 5mm TQFP, 5mm x 5mm QFN, and industry-standard 32-pin 7mm x 7mm TQFP packages.

## Applications

Precision Clock Distribution  
Low-Jitter Data Repeater

## Features

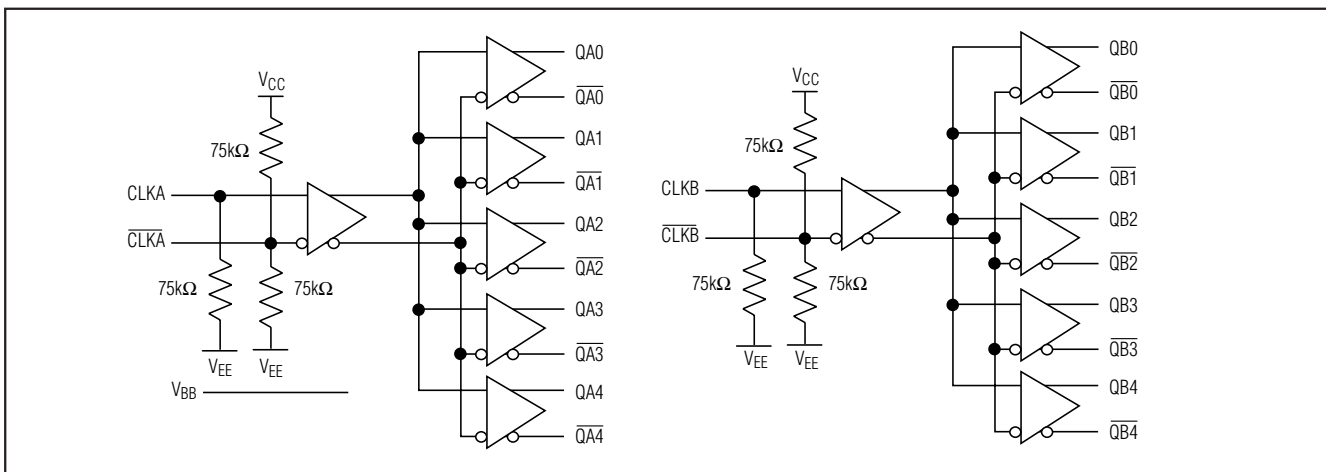
- ◆ +2.25V to +3.8V Differential HSTL/LVPECL Operation
- ◆ -2.25V to -3.8V Differential LVECL Operation
- ◆ 30ps (typ) Part-to-Part Skew
- ◆ 12ps (typ) Output-to-Output Skew
- ◆ 312ps (typ) Propagation Delay
- ◆  $\geq 300\text{mV}$  Differential Output at 3GHz
- ◆ On-Chip Reference for Single-Ended Inputs
- ◆ Output Low with Open Input
- ◆ Pin Compatible with MC100LVEP210 (MAX9312) and MC100EP210 (MAX9314)
- ◆ Offered in Tiny QFN\* Package (70% Smaller Footprint than LQFP)

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9312ECJ	-40°C to +85°C	32 TQFP (7mm x 7mm)
MAX9312EGJ*	-40°C to +85°C	32 QFN (5mm x 5mm)
MAX9312EHJ*	-40°C to +85°C	32 TQFP (5mm x 5mm)
MAX9314ECJ	-40°C to +85°C	32 TQFP (7mm x 7mm)
MAX9314EGJ*	-40°C to +85°C	32 QFN (5mm x 5mm)
MAX9314EHJ*	-40°C to +85°C	32 TQFP (5mm x 5mm)

\*Future product—contact factory for availability.

## Functional Diagram



Pin Configuration appears at end of data sheet.



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# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## ABSOLUTE MAXIMUM RATINGS

V<sub>CC</sub> - V<sub>EE</sub>.....4.1V  
 Inputs (CLK<sub>-</sub>, CLK<sub>-</sub>) .....V<sub>EE</sub> - 0.3V to V<sub>CC</sub> + 0.3V  
 CLK<sub>-</sub> to CLK<sub>-</sub> .....±3.0V  
 Continuous Output Current .....50mA  
 Surge Output Current.....100mA  
 V<sub>BB</sub> Sink/Source Current .....±0.65mA  
 Junction-to-Ambient Thermal Resistance in Still Air  
 32-Pin 7mm × 7mm TQFP.....+90°C/W  
 Junction-to-Ambient Thermal Resistance with  
 500 LFPM Airflow  
 32-Pin 7mm × 7mm TQFP .....+60°C/W

Junction-to-Case Thermal Resistance  
 32-Pin 7mm × 7mm TQFP .....+12°C/W  
 Operating Temperature Range .....-40°C to +85°C  
 Junction Temperature .....+150°C  
 Storage Temperature Range .....-65°C to +150°C  
 ESD Protection  
 Human Body Model (CLK<sub>-</sub>, CLK<sub>-</sub>, Q<sub>-</sub>, Q<sub>-</sub>) .....2kV  
 Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> - V<sub>EE</sub> = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to V<sub>CC</sub> - 2V.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS	-40°C		+25°C		+85°C		UNITS	
			MIN	MAX	MIN	MAX	MIN	MAX		
<b>INPUTS (CLK<sub>-</sub>, CLK<sub>-</sub>)</b>										
Single-Ended Input High Voltage	V <sub>IH</sub>	V <sub>BB</sub> connected to CLK <sub>-</sub> (V <sub>IL</sub> for V <sub>BB</sub> connected to CLK <sub>-</sub> )	MAX9312	V <sub>CC</sub> - 1.23	V <sub>CC</sub>	V <sub>CC</sub> - 1.23	V <sub>CC</sub>	V <sub>CC</sub> - 1.23	V <sub>CC</sub>	V
			MAX9314	V <sub>CC</sub> - 1.165	V <sub>CC</sub>	V <sub>CC</sub> - 1.165	V <sub>CC</sub>	V <sub>CC</sub> - 1.165	V <sub>CC</sub>	
Single-Ended Input Low Voltage	V <sub>IL</sub>	V <sub>BB</sub> connected to CLK <sub>-</sub> (V <sub>IL</sub> for V <sub>BB</sub> connected to CLK <sub>-</sub> )	MAX9312	V <sub>EE</sub>	V <sub>CC</sub> - 1.62	V <sub>EE</sub>	V <sub>CC</sub> - 1.62	V <sub>EE</sub>	V <sub>CC</sub> - 1.62	V
			MAX9314	V <sub>EE</sub>	V <sub>CC</sub> - 1.475	V <sub>EE</sub>	V <sub>CC</sub> - 1.475	V <sub>EE</sub>	V <sub>CC</sub> - 1.475	
High Voltage of Differential Input	V <sub>IHD</sub>		V <sub>EE</sub> + 1.2	V <sub>CC</sub>	V <sub>EE</sub> + 1.2	V <sub>CC</sub>	V <sub>EE</sub> + 1.2	V <sub>CC</sub>	V	
Low Voltage of Differential Input	V <sub>ILD</sub>		V <sub>EE</sub>	V <sub>CC</sub> - 0.095	V <sub>EE</sub>	V <sub>CC</sub> - 0.095	V <sub>EE</sub>	V <sub>CC</sub> - 0.095	V	
Differential Input Voltage	V <sub>IHD</sub> - V <sub>ILD</sub>	For V <sub>CC</sub> - V <sub>EE</sub> < 3.0V	0.095	V <sub>CC</sub> - V <sub>EE</sub>	0.095	V <sub>CC</sub> - V <sub>EE</sub>	0.095	V <sub>CC</sub> - V <sub>EE</sub>	V	
		For V <sub>CC</sub> - V <sub>EE</sub> ≥ 3.0V	0.095	3.0	0.095	3.0	0.095	3.0		
Input High Current	I <sub>IH</sub>			150		150		150	μA	
CLK <sub>-</sub> Input Low Current	I <sub>ILCLK</sub>		-10	+10	-10	+10	-10	+10	μA	

# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

MAX9312/MAX9314

## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} - V_{EE} = +2.25V$  to  $+3.8V$ , outputs loaded with  $50\Omega \pm 1\%$  to  $V_{CC} - 2V$ .) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS	-40°C		+25°C		+85°C		UNITS	
			MIN	MAX	MIN	MAX	MIN	MAX		
CLK <sub>-</sub> Input Low Current	$I_{IL\overline{CLK}}$		-150		-150		-150		$\mu A$	
<b>OUTPUTS (Q<sub>-</sub>, Q<sub>-</sub>)</b>										
Single-Ended Output High Voltage	$V_{OH}$	Figure 1	$V_{CC} - 1.025$	$V_{CC} - 0.900$	$V_{CC} - 1.025$	$V_{CC} - 0.900$	$V_{CC} - 1.025$	$V_{CC} - 0.900$	V	
Single-Ended Output Low Voltage	$V_{OL}$	Figure 1	$V_{CC} - 1.930$	$V_{CC} - 1.695$	$V_{CC} - 1.930$	$V_{CC} - 1.695$	$V_{CC} - 1.930$	$V_{CC} - 1.695$	V	
Differential Output Voltage	$V_{OH} - V_{OL}$	Figure 1	670	950	670	950	670	950	mV	
<b>REFERENCE (V<sub>BB</sub>)</b>										
Reference Voltage Output (Note 5)	$V_{BB}$	$I_{BB} = \pm 0.5mA$	MAX9312	$V_{CC} - 1.525$	$V_{CC} - 1.325$	$V_{CC} - 1.525$	$V_{CC} - 1.325$	$V_{CC} - 1.525$	$V_{CC} - 1.325$	V
			MAX9314	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.26$	
<b>POWER SUPPLY</b>										
Supply Current (Note 6)	$I_{EE}$			75		82		95	mA	

# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} - V_{EE} = +2.25V$  to  $+3.8V$ , outputs loaded with  $50\Omega \pm 1\%$  to  $V_{CC} - 2V$ , input frequency =  $1.5GHz$ , input transition time =  $125ps$  (20% to 80%),  $V_{IHD} = V_{EE} + 1.2V$  to  $V_{CC}$ ,  $V_{ILD} = V_{EE}$  to  $V_{CC} - 0.15V$ ,  $V_{IHD} - V_{ILD} = 0.15V$  to the smaller of  $3V$  or  $V_{CC} - V_{EE}$ , unless otherwise noted. Typical values are at  $V_{CC} - V_{EE} = 3.3V$ ,  $V_{IHD} = V_{CC} - 1V$ ,  $V_{ILD} = V_{CC} - 1.5V$ .) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input-to-Output Delay	$t_{PLHD}$ , $t_{PHLD}$	Figure 2	220	321	380	220	312	410	260	322	400	ps
Output-to-Output Skew (Note 8)	$t_{SKOO}$			12	46		12	46		10	35	ps
Part-to-Part Skew (Note 9)	$t_{SKPP}$			30	160		30	190		30	140	ps
Added Random Jitter (Note 10)	$t_{RJ}$	$f_{IN} = 1.5GHz$ clock pattern		1.2	2.5		1.2	2.5		1.2	2.5	ps (RMS)
		$f_{IN} = 3.0GHz$ clock pattern		1.2	2.6		1.2	2.6		1.2	2.6	
Added Deterministic Jitter (Note 10)	$t_{DJ}$	3Gbps, 2 <sup>23</sup> -1 PRBS pattern		80	95		80	95		80	95	ps (pk-pk)
Switching Frequency	$f_{MAX}$	$V_{OH} - V_{OL} \geq 300mV$ , clock pattern, Figure 2		3.0			3.0			3.0		GHz
		$V_{OH} - V_{OL} \geq 500mV$ , clock pattern, Figure 2		1.5			1.5			1.5		
Output Rise/Fall Time (20% to 80%)	$t_R$ , $t_F$	Figure 2	100	112	140	100	116	140	100	121	140	ps

**Note 1:** Measurements are made with the device in thermal equilibrium.

**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative.

**Note 3:** Single-ended input operation using  $V_{BB}$  is limited to  $V_{CC} - V_{EE} = 3.0V$  to  $3.8V$  for the MAX9312 and  $V_{CC} - V_{EE} = 2.7V$  to  $3.8V$  for the MAX9314.

**Note 4:** DC parameters production tested at  $T_A = +25^\circ C$ . Guaranteed by design and characterization over the full operating temperature range.

**Note 5:** Use  $V_{BB}$  only for inputs that are on the same device as the  $V_{BB}$  reference.

**Note 6:** All pins open except  $V_{CC}$  and  $V_{EE}$ .

**Note 7:** Guaranteed by design and characterization limits are set at  $\pm 6\sigma$ .

**Note 8:** Measured between outputs on the same part at the signal crossing points for a same-edge transition.

**Note 9:** Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.

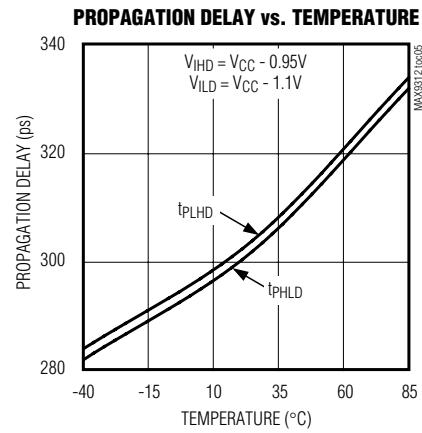
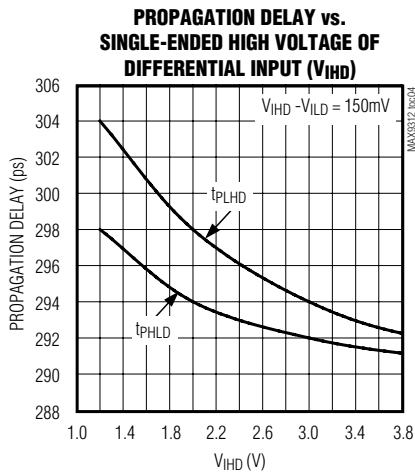
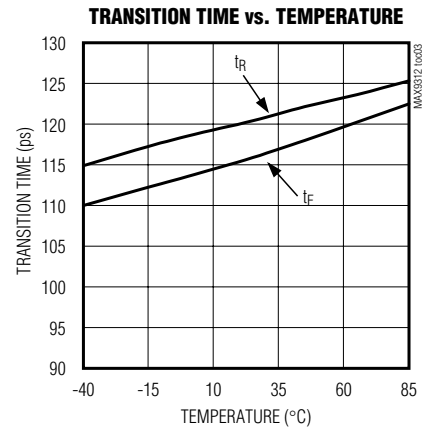
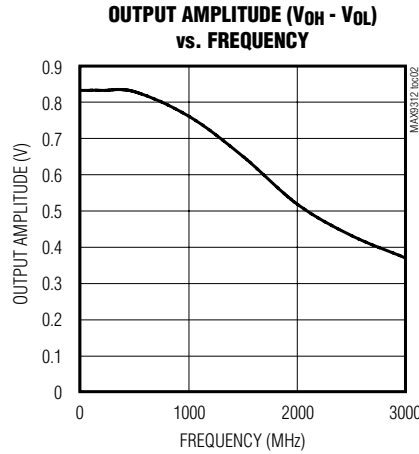
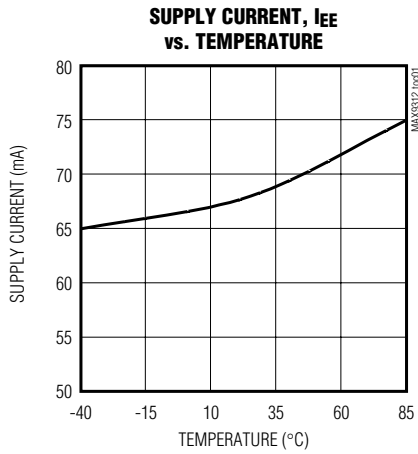
**Note 10:** Device jitter added to the input signal.

# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## Typical Operating Characteristics

( $V_{CC} = +3.3V$ ,  $V_{EE} = 0$ ,  $V_{IHD} = V_{CC} - 0.95V$ ,  $V_{ILD} = V_{CL} - 1.25V$ , input transition time = 125ps (20% to 80%),  $f_{IN} = 1.5GHz$ , outputs loaded with  $50\Omega$  to  $V_{CC} - 2V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX9312/MAX9314



# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## Pin Description

PIN	NAME	FUNCTION
1, 9, 16, 25, 32	V <sub>CC</sub>	Positive Supply Voltage. Bypass from V <sub>CC</sub> to V <sub>EE</sub> with 0.1μF and 0.01μF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	N.C.	Not Connected
3	CLKA	Noninverting Differential Clock Input A
4	$\overline{\text{CLKA}}$	Inverting Differential Clock Input A
5	V <sub>BB</sub>	Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass to V <sub>CC</sub> with a 0.01μF ceramic capacitor.
6	CLKB	Noninverting Differential Clock Input B
7	$\overline{\text{CLKB}}$	Inverting Differential Clock Input B
8	V <sub>EE</sub>	Negative Supply Voltage
10	$\overline{\text{QB4}}$	Inverting QB4 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
11	QB4	Noninverting QB4 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
12	$\overline{\text{QB3}}$	Inverting QB3 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
13	QB3	Noninverting QB3 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
14	$\overline{\text{QB2}}$	Inverting QB2 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
15	QB2	Noninverting QB2 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
17	$\overline{\text{QB1}}$	Inverting QB1 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
18	QB1	Noninverting QB1 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
19	$\overline{\text{QB0}}$	Inverting QB0 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
20	QB0	Noninverting QB0 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
21	$\overline{\text{QA4}}$	Inverting QA4 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
22	QA4	Noninverting QA4 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
23	$\overline{\text{QA3}}$	Inverting QA3 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
24	QA3	Noninverting QA3 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
26	$\overline{\text{QA2}}$	Inverting QA2 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
27	QA2	Noninverting QA2 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
28	$\overline{\text{QA1}}$	Inverting QA1 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
29	QA1	Noninverting QA1 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
30	$\overline{\text{QA0}}$	Inverting QA0 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.
31	QA0	Noninverting QA0 Output. Typically terminate with 50Ω resistor to V <sub>CC</sub> - 2V.

# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

MAX9312/MAX9314

## Detailed Description

The MAX9312/MAX9314 are low-skew, dual 1-to-5 differential drivers designed for clock and data distribution.

For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

The differential inputs can be configured to accept single-ended inputs when operating at approximately  $V_{CC} - V_{EE} = 3.0V$  to 3.8V for the MAX9312 or  $V_{CC} - V_{EE} = 2.7V$  to 3.8V for the MAX9314. This is accomplished by connecting the on-chip reference voltage,  $V_{BB}$ , to an input as a reference. For example, the differential  $CLKA$ ,  $\overline{CLKA}$  input is converted to a noninverting, single-ended input by connecting  $V_{BB}$  to  $\overline{CLKA}$  and connecting the single-ended input to  $CLKA$ . Similarly, an inverting input is obtained by connecting  $V_{BB}$  to  $CLKA$  and connecting the single-ended input to  $\overline{CLKA}$ . With a differential input configured as single ended (using  $V_{BB}$ ), the single-ended input can be driven to  $V_{CC}$  and  $V_{EE}$  or with a single-ended LVPECL/LVECL signal.

When a differential input is configured as a single-ended input (using  $V_{BB}$ ), the approximate supply range is  $V_{CC} - V_{EE} = 3.0V$  to 3.8V for the MAX9312 and  $V_{CC} - V_{EE} = 2.7V$  to 3.8V for the MAX9314. This is because one of the inputs must be  $V_{EE} + 1.2V$  or higher for proper operation of the input stage.  $V_{BB}$  must be at least  $V_{EE} + 1.2V$  because it becomes the high-level input when the other (single-ended) input swings below it. Therefore, minimum  $V_{BB} = V_{EE} + 1.2V$ .

The minimum  $V_{BB}$  output for the MAX9312 is  $V_{CC} - 1.525V$  and the minimum  $V_{BB}$  output for the MAX9314 is  $V_{CC} - 1.38V$ . Substituting the minimum  $V_{BB}$  output for each device into  $V_{BB} = V_{EE} + 1.2V$  results in a minimum supply of 2.725V for the MAX9312 and 2.58V for the MAX9314. Rounding up to standard supplies gives the single-ended operating supply ranges of  $V_{CC} - V_{EE} = 3.0V$  to 3.8V for the MAX9312 and  $V_{CC} - V_{EE} = 2.7V$  to 3.8V for the MAX9314.

When using the  $V_{BB}$  reference output, bypass it with a 0.01 $\mu F$  ceramic capacitor to  $V_{CC}$ . If the  $V_{BB}$  reference is not used, it can be left open. The  $V_{BB}$  reference can source or sink 0.5mA, which is sufficient to drive two inputs. Use  $V_{BB}$  only for inputs that are on the same device as the  $V_{BB}$  reference.

The maximum magnitude of the differential input from  $CLK_{-}$  to  $\overline{CLK}_{-}$  is 3.0V or  $V_{CC} - V_{EE}$ , whichever is less.

This limit also applies to the difference between any reference voltage input and a single-ended input.

The differential inputs have bias resistors that drive the outputs to a differential low when the inputs are open. The inverting inputs ( $\overline{CLKA}$  and  $\overline{CLKB}$ ) are biased with a 75k $\Omega$  pullup to  $V_{CC}$  and a 75k $\Omega$  pulldown to  $V_{EE}$ . The noninverting inputs ( $CLKA$  and  $CLKB$ ) are biased with a 75k $\Omega$  pulldown to  $V_{EE}$ .

Specifications for the high and low voltages of a differential input ( $V_{IHD}$  and  $V_{ILD}$ ) and the differential input voltage ( $V_{IHD} - V_{ILD}$ ) apply simultaneously ( $V_{ILD}$  cannot be higher than  $V_{IHD}$ ).

Output levels are referenced to  $V_{CC}$  and are considered LVPECL or LVECL, depending on the level of the  $V_{CC}$  supply. With  $V_{CC}$  connected to a positive supply and  $V_{EE}$  connected to GND, the outputs are LVPECL. The outputs are LVECL when  $V_{CC}$  is connected to GND and  $V_{EE}$  is connected to a negative supply.

A single-ended input of at least  $V_{BB} \pm 95mV$  or a differential input of at least 95mV switches the outputs to the  $V_{OH}$  and  $V_{OL}$  levels specified in the *DC Electrical Characteristics* table.

## Applications Information

### Supply Bypassing

Bypass  $V_{CC}$  to  $V_{EE}$  with high-frequency surface-mount ceramic 0.1 $\mu F$  and 0.01 $\mu F$  capacitors in parallel as close to the device as possible, with the 0.01 $\mu F$  value capacitor closest to the device. Use multiple parallel vias for low inductance. When using the  $V_{BB}$  reference output, bypass it with a 0.01 $\mu F$  ceramic capacitor to  $V_{CC}$  (if the  $V_{BB}$  reference is not used, it can be left open).

### Traces

Input and output trace characteristics affect the performance of the MAX9312/MAX9314.

Connect each signal of a differential input or output to a 50 $\Omega$  characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50 $\Omega$  characteristic impedance through connectors and across cables. Reduce skew within a differential pair by matching the electrical length of the traces.

### Output Termination

Terminate outputs through 50 $\Omega$  to  $V_{CC} - 2V$  or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if QA0 is used as a single-ended output, terminate both QA0 and  $\overline{QA0}$ .

# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

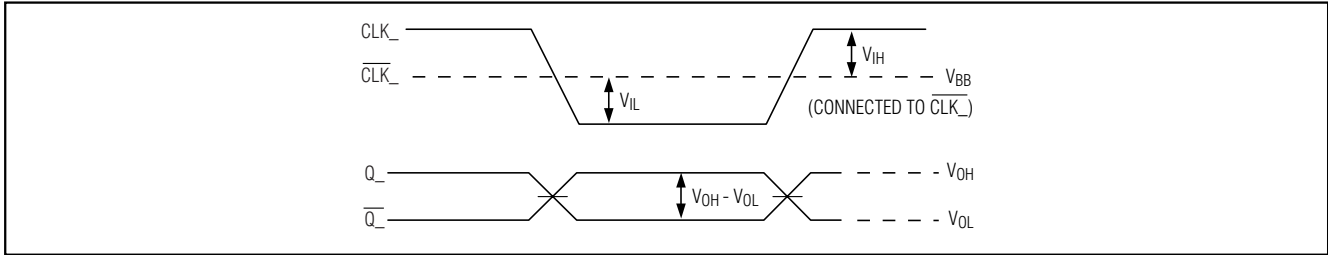


Figure 1. Switching with Single-Ended Input

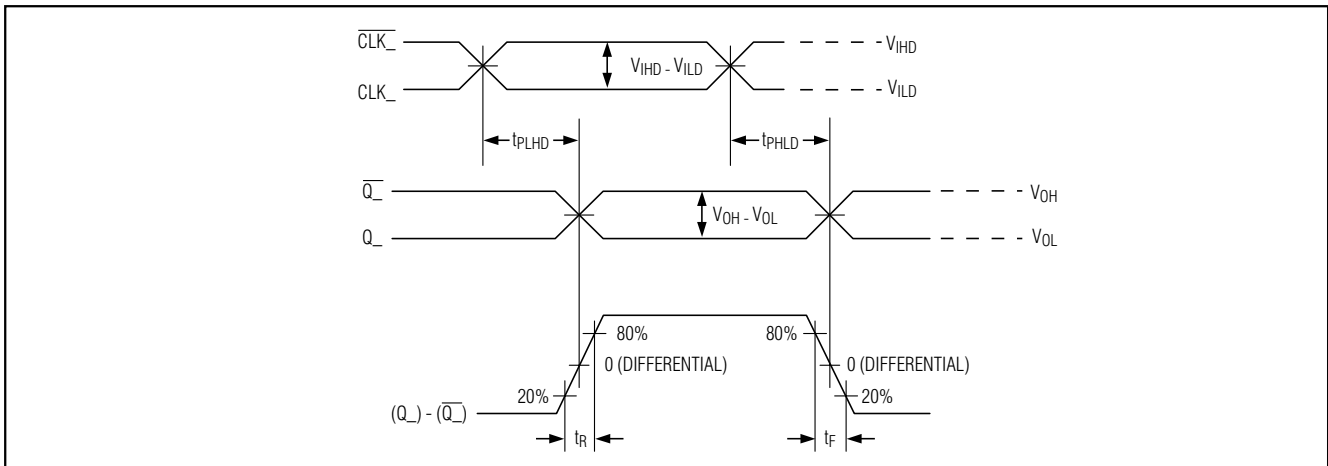
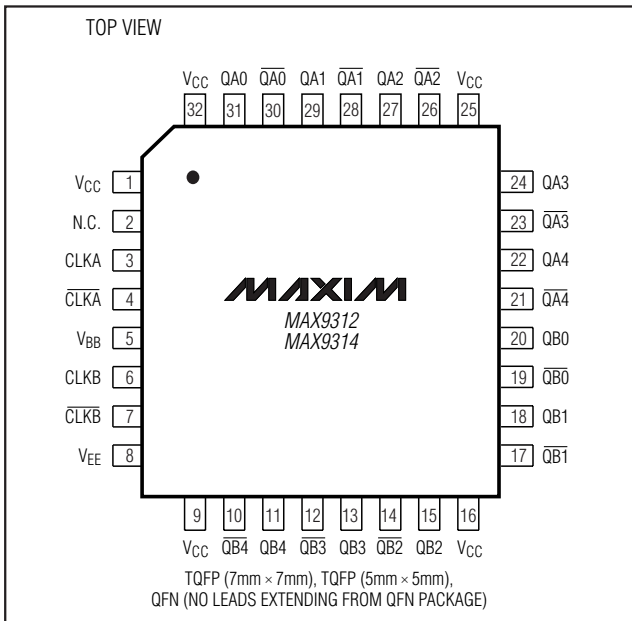


Figure 2. Differential Transition Time and Propagation Delay Timing Diagram

## Pin Configuration



## Chip Information

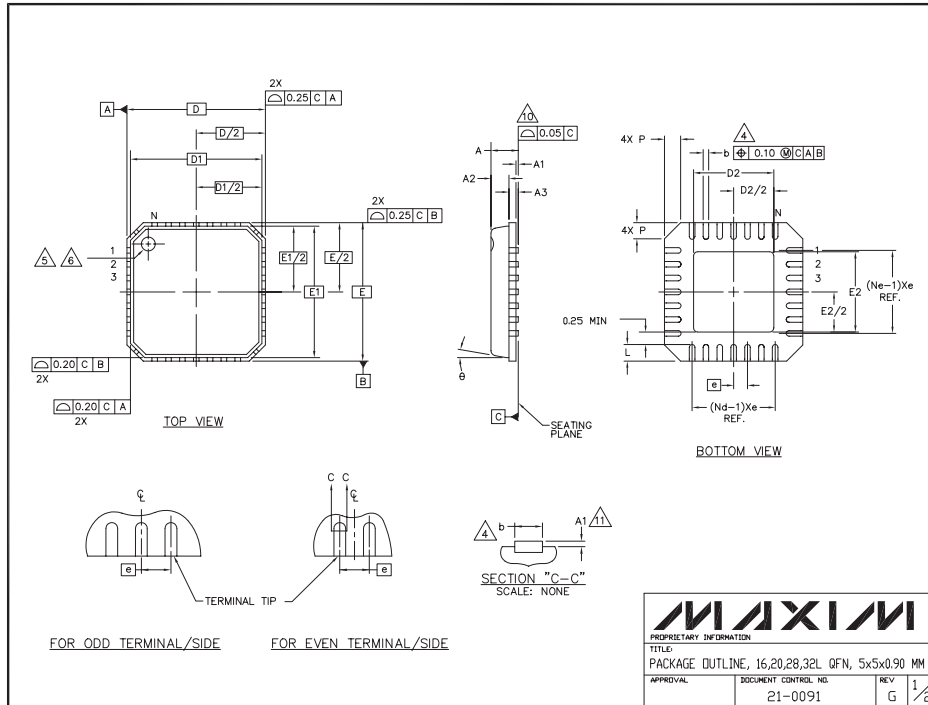
TRANSISTOR COUNT: 250



# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## Package Information

MAX9312/MAX9314



### NOTES:

- DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
- DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
- N IS THE NUMBER OF TERMINALS.  
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &  
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
- THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
- EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- PACKAGE WARPAGE MAX 0.05mm.
- APPLIED FOR EXPOSED PAD AND TERMINALS.  
EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
- MEETS JEDEC MO220.
- THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

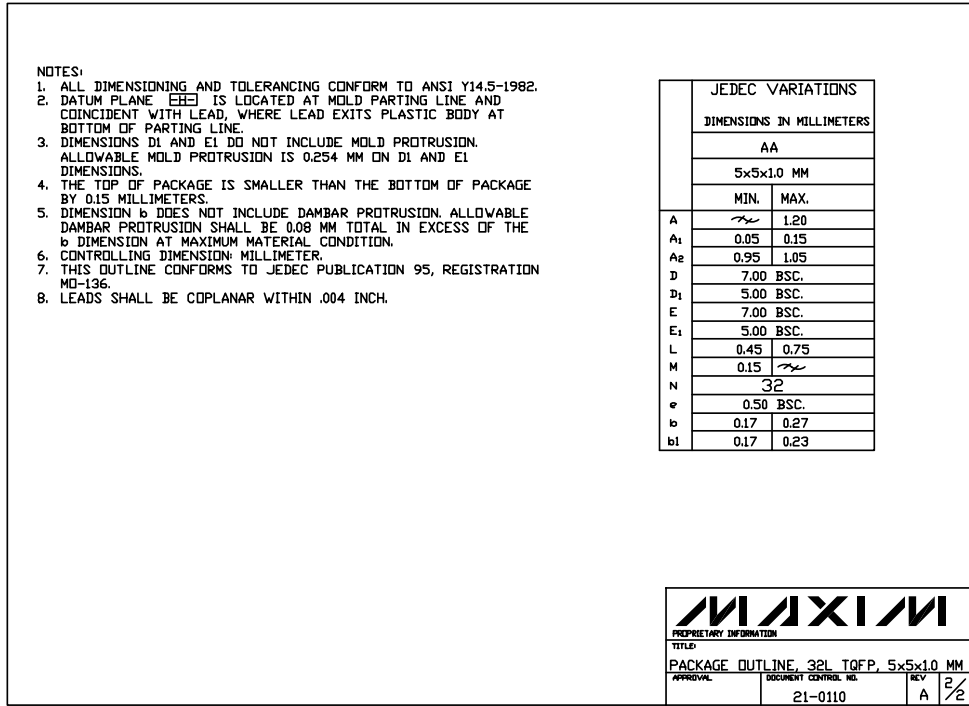
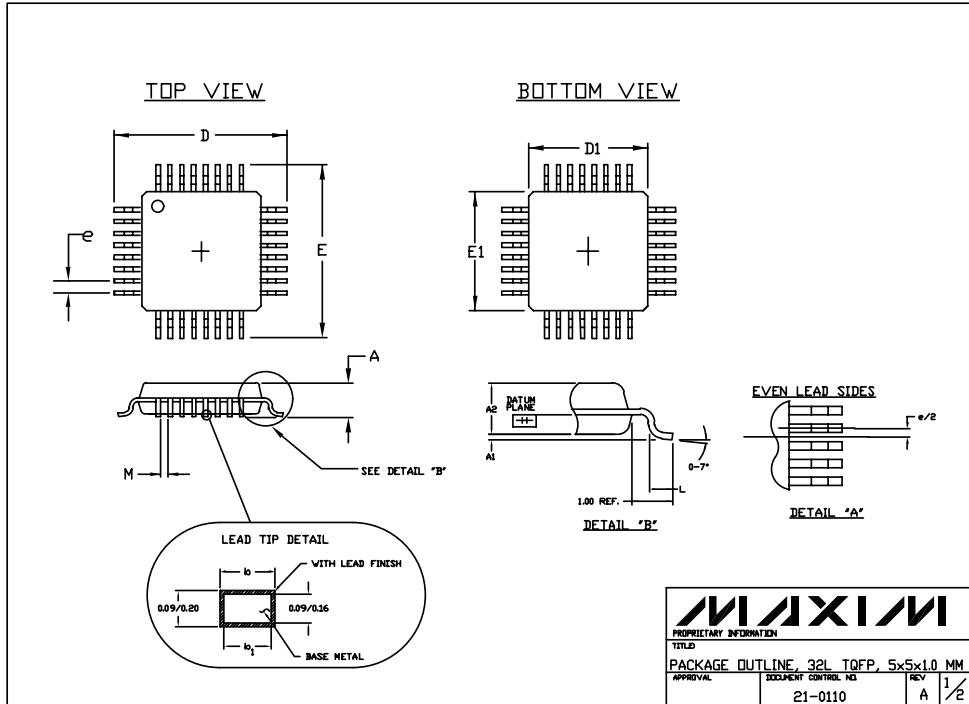
SYMBOL	COMMON DIMENSIONS			N <sub>d</sub> / N <sub>e</sub>
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3	0.20 REF.			
D	5.00 BSC			
D1	4.75 BSC			
E	5.00 BSC			
E1	4.75 BSC			
θ	0°	-	12°	
P	0	-	0.60	
D2	1.25	-	3.25	
E2	1.25	-	3.25	

SYMBOL	PITCH VARIATION B			N <sub>d</sub> / N <sub>e</sub>	SYMBOL	PITCH VARIATION B			N <sub>d</sub> / N <sub>e</sub>	SYMBOL	PITCH VARIATION C			N <sub>d</sub> / N <sub>e</sub>	SYMBOL	PITCH VARIATION D			N <sub>d</sub> / N <sub>e</sub>
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
B	0.60 BSC				B	0.65 BSC				B	0.50 BSC				B	0.50 BSC			
N	16			3	N	20			3	N	28			3	N	32			3
N <sub>d</sub>	4			3	N <sub>d</sub>	5			3	N <sub>d</sub>	7			3	N <sub>d</sub>	8			3
N <sub>e</sub>	4			3	N <sub>e</sub>	5			3	N <sub>e</sub>	7			3	N <sub>e</sub>	8			3
I	0.35	0.55	0.75	1	I	0.35	0.55	0.75	1	I	0.35	0.55	0.75	1	I	0.30	0.40	0.50	1
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4

PROPRIETARY INFORMATION	
TITLE PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM	
APPROVAL	DOCUMENT CONTROL NO. REV. 2/2
	21-0091 G

# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

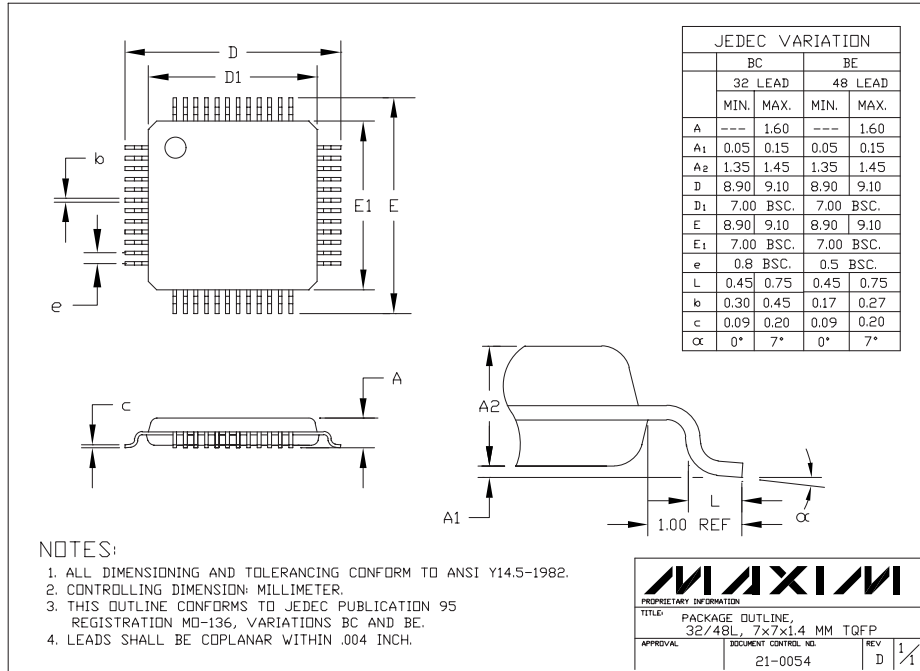
## Package Information (continued)



# Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## Package Information (continued)

**MAX9312/MAX9314**



32L/48L TQFP EP5

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