INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT

TC74AC574P/F/FW/FS

SILICON MONOLITHIC

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The TC74AC574 is an advanced high speed CMOS OCTAL FLIP-FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

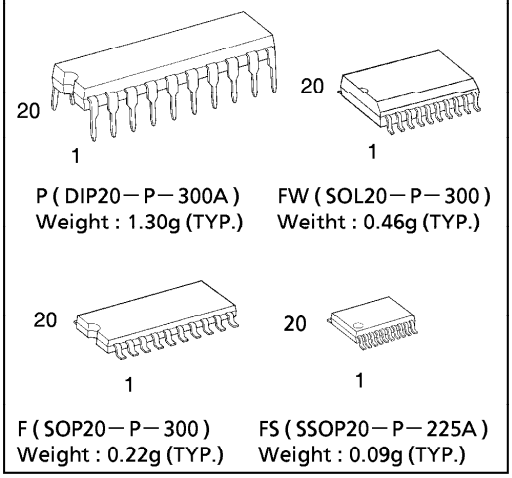
These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX} = 180MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 8μA(Max.) at Ta = 25°C
- High Noise Immunity ..... $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range .... V_{CC} (opr) = 2V~5.5V
- Pin and Function Compatible with 74F574



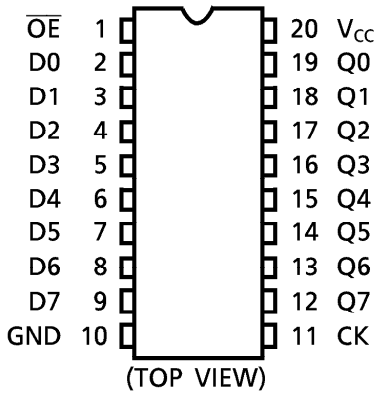
P (DIP20-P-300A) Weight : 1.30g (TYP.)

FW (SOL20-P-300) Weitht : 0.46g (TYP.)

F (SOP20-P-300) Weight : 0.22g (TYP.)

FS (SSOP20-P-225A) Weight : 0.09g (TYP.)

PIN ASSIGNMENT

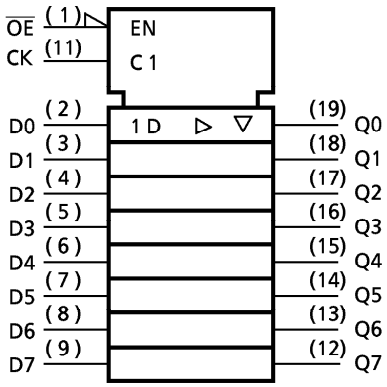


TRUTH TABLE

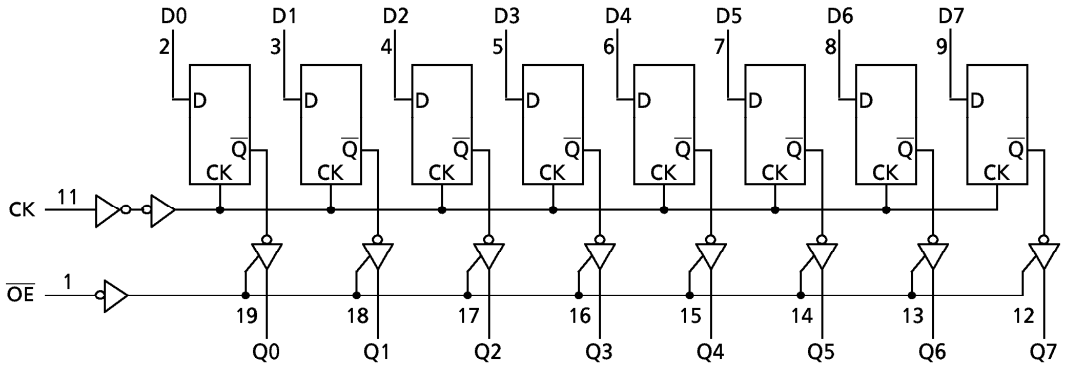
INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	Q_n
L	↑	L	L
L	↑	H	H

X : Don't Care
Z : High Impedance
Q_n : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP)*/ 180 (SOP/SSOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~ 100 (Vcc = 3.3 ± 0.3V) 0~ 20 (Vcc = 5 ± 0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I_{OH} = −4mA I_{OH} = −24mA I_{OH} = −75mA*	3.0 4.5 5.5	2.58 3.94 —	— — —	— — —	2.48 3.80 3.85	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I_{OL} = 12mA I_{OL} = 24mA I_{OL} = 75mA*	3.0 4.5 5.5	— — —	— — —	0.36 0.36 —	— — —	0.44 0.44 1.65	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	Ta = −40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	ns
Minimum Set - up Time	t_s		3.3 ± 0.3 5.0 ± 0.5	9.0 4.5	9.0 4.5	
Minimum Hold Time	t_h		3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF , R_L = 500Ω , Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = −40~85°C		UNIT
		V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}	3.3 ± 0.3 5.0 ± 0.5	— —	9.8 6.1	16.7 9.2	1.0 1.0	19.0 10.5	ns
Output Enable Time	t_{pZL} t_{pZH}	3.3 ± 0.3 5.0 ± 0.5	— —	9.2 6.1	15.8 9.3	1.0 1.0	18.0 10.6	
Output Disable Time	t_{pLZ} t_{pHZ}	3.3 ± 0.3 5.0 ± 0.5	— —	6.6 5.8	11.0 8.8	1.0 1.0	12.5 10.0	
Maximum Clock Frequency	f_{MAX}	3.3 ± 0.3 5.0 ± 0.5	50 95	100 160	— —	50 95	— —	MHz
Input Capacitance	C_{IN}		—	5	10	—	10	pF
Output Capacitance	C_{OUT}		—	10	—	—	—	
Power Dissipation Capacitance	C_{PD} (1)		—	36	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

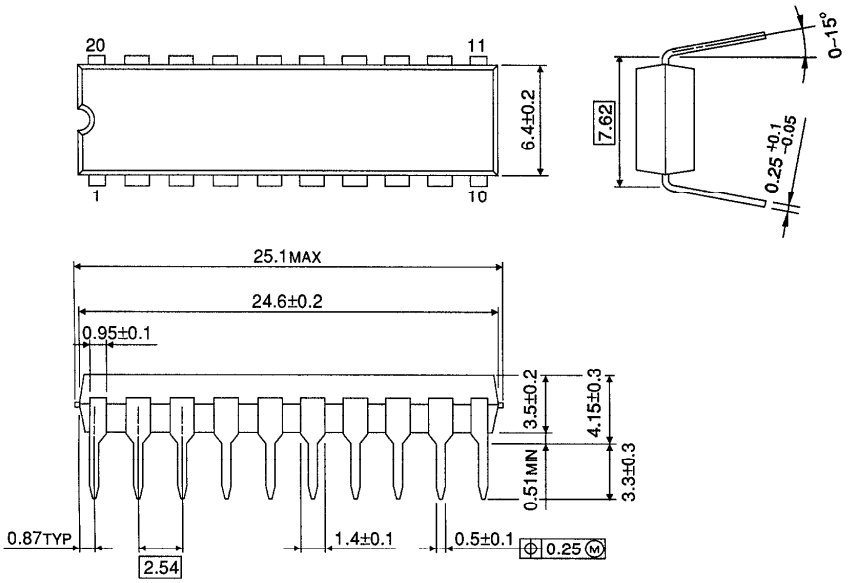
Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

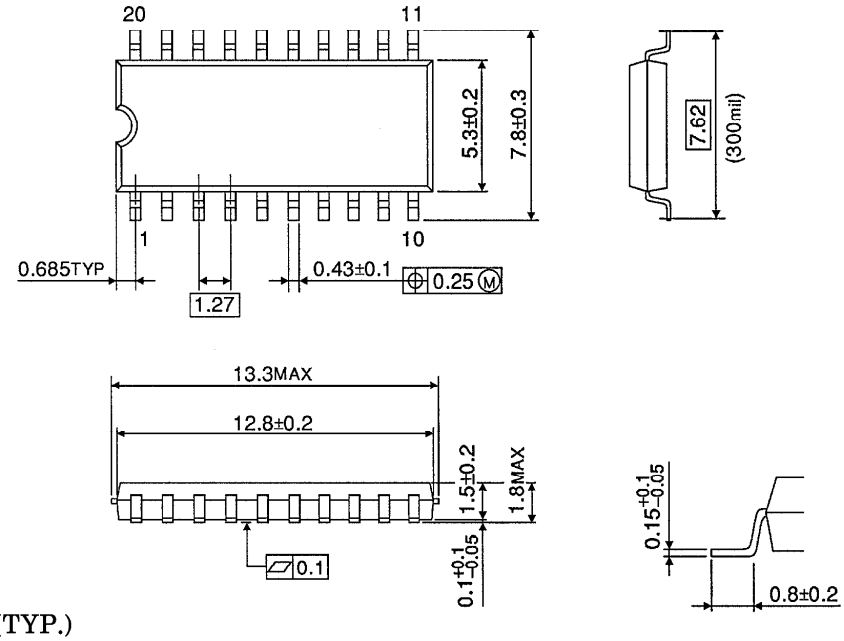
$$C_{PD}(total) = 26 + 10 \cdot n$$

DIP 20PIN OUTLINE DRAWING (DIP20−P−300A) Unit in mm



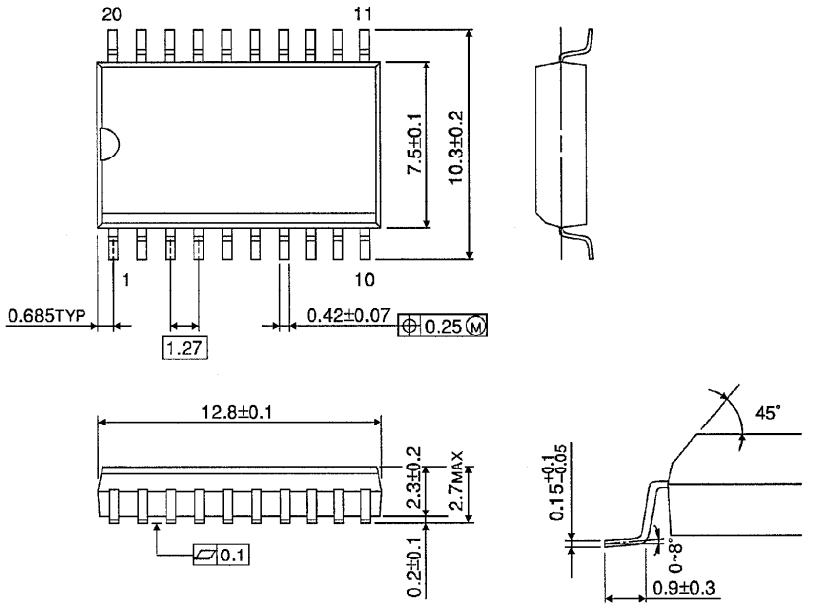
Weight : 1.30g (TYP.)

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20−P−300) Unit in mm



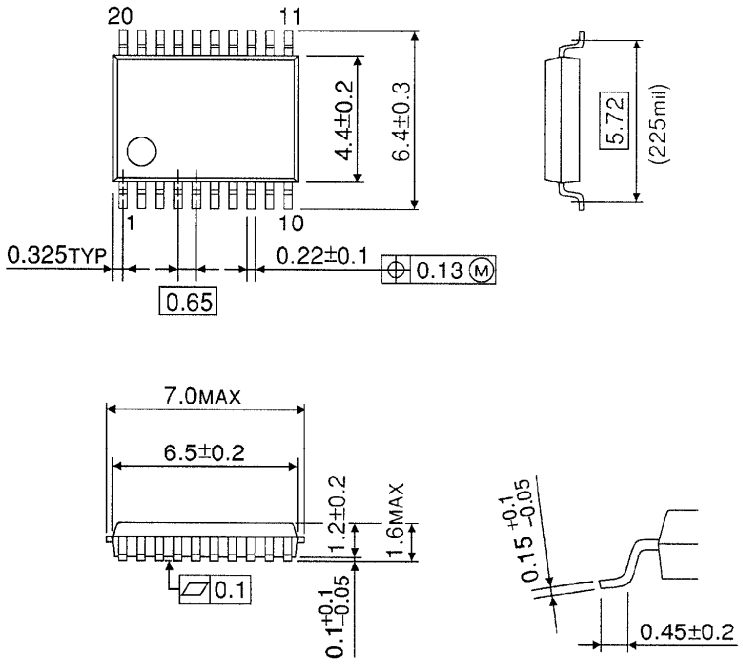
Weight : 0.22g (TYP.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20−P−300) Unit in mm



Weight : 0.46g (TYP.)

SSOP 20PIN OUTLINE DRAWING (SSOP20−P−225A) Unit in mm



Weight : 0.09g (TYP.)