



## TV Horizontal Processors

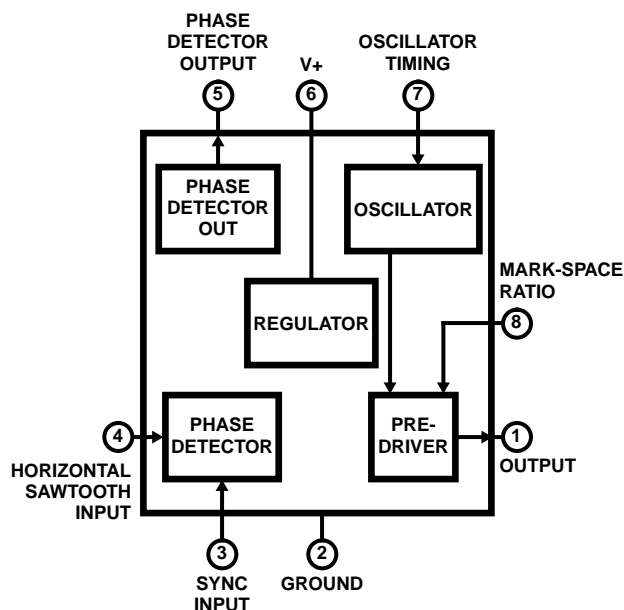
### Description

- The Harris CA1391E and CA1394E are monolithic integrated circuits designed for use in the low-level horizontal section of monochrome or color television receivers. Functions include a phase detector, an oscillator, a regulator, and a pre-driver.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA1391E	0 to 85	8 Ld PDIP	E8.3
CA1394E	0 to 85	8 Ld PDIP	E8.3

### Functional Diagram

File Number **981.3**

# CA1391, CA1394

## Absolute Maximum Ratings

DC Supply Current	40mA
DC Output Voltage	40V
DC Output Current	30mA
Sync Input Voltage	5V <sub>P-P</sub>
Sawtooth Input Voltage	5V <sub>P-P</sub>

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
PDIP Package	120
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

## Operating Conditions

Temperature Range . . . . . 0°C to 85°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications (See Figure 1)

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Supply Voltage	S <sub>1</sub> , S <sub>5</sub> , S <sub>6</sub> = 2; S <sub>2</sub> , S <sub>3</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub> = 1 Measure Terminal 6 to GND	25	8	-	9	V
Free Running Frequency -1%	S <sub>1</sub> , S <sub>5</sub> , S <sub>6</sub> = 2; S <sub>2</sub> , S <sub>3</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub> = 1 Counter to Terminal 1	25	14734	-	16734	Hz
Output Leakage	S <sub>2</sub> , S <sub>3</sub> , S <sub>6</sub> , S <sub>8</sub> = 1; S <sub>1</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>7</sub> = 2 Measure Terminal 1 to 25V	25	-	10	-	mV
Output Saturation	S <sub>2</sub> , S <sub>3</sub> , S <sub>5</sub> , S <sub>6</sub> , S <sub>8</sub> = 1; S <sub>1</sub> , S <sub>4</sub> , S <sub>7</sub> = 2 Measure Terminal 1 to GND	25	-	60	-	mV
Phase Detector Bias	S <sub>2</sub> , S <sub>5</sub> , S <sub>6</sub> , S <sub>8</sub> = 1; S <sub>1</sub> , S <sub>3</sub> , S <sub>4</sub> , S <sub>7</sub> = 2 Measure Terminal 3 to GND	25	-	1.9	-	V
Phase Detector Leak	S <sub>5</sub> , S <sub>8</sub> = 1; S <sub>1</sub> , S <sub>2</sub> , S <sub>3</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>7</sub> = 2 Measure Terminal 5 to +4V	25	-2	-	2	mV
Phase Detector Low	S <sub>1</sub> , S <sub>5</sub> , S <sub>8</sub> = 1; S <sub>2</sub> , S <sub>3</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>7</sub> = 2 Measure Terminal 5 to +4V	25	-0.55 (Note 2)	-	-	V
Phase Detector High	S <sub>1</sub> , S <sub>5</sub> , S <sub>6</sub> , S <sub>8</sub> = 1; S <sub>2</sub> , S <sub>3</sub> , S <sub>4</sub> , S <sub>7</sub> = 2 Measure Terminal 5 to +4V	25	+0.55 (Note 2)	-	-	V
Phase Detector Balance	V <sub>DET2</sub> + V <sub>DET3</sub>	25	-100	-	100	mV
Sync Diode	S <sub>1</sub> , S <sub>2</sub> , S <sub>3</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>7</sub> = 1; S <sub>5</sub> , S <sub>8</sub> = 2	25	0.3	-	1.2	V
Static Phase Error	See Figure 3	25	-	0.5	-	μs
Oscillator Pull In Range			-	±300	-	Hz
Oscillator Hold In Range			-	±900	-	Hz

NOTE:

2. Polarity reversed in the CA1391.

# Test Circuit

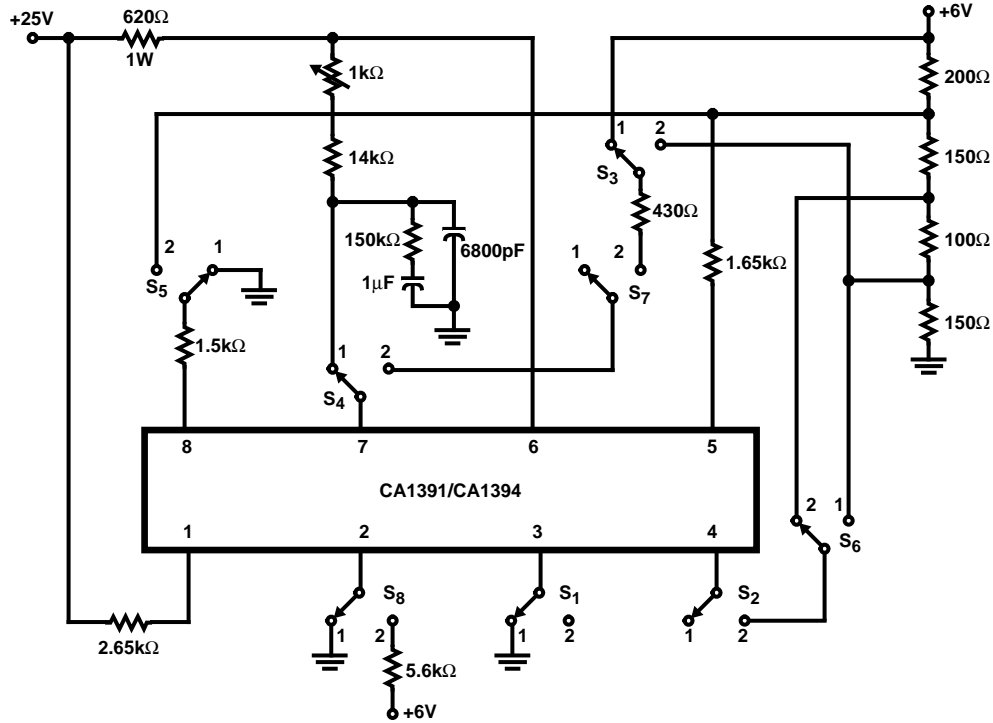
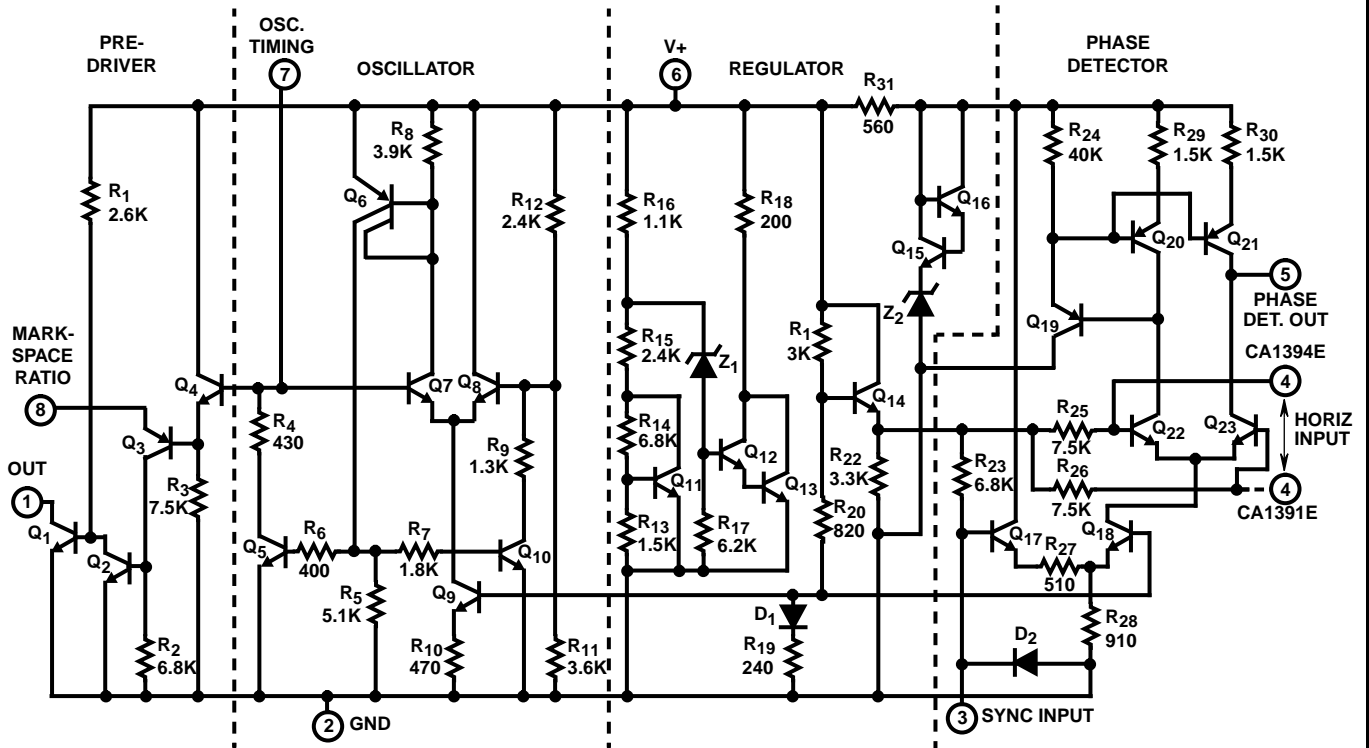


FIGURE 1. DC TEST CIRCUIT

# Schematic Diagram



NOTE: All resistances are in ohms.

## Application Information

### Circuit Operation (See Schematic Diagram)

The CA1391 and CA1394 contain the oscillator, phase detector, and predriver sections necessary for the television horizontal oscillator and AFC loop.

The oscillator is an RC type with Terminal 7 used to control the timing. If it is assumed that  $Q_7$  is initially off, then an external capacitor connected from Terminal 7 to ground charges through an external resistance connected between Terminals 6 and 7. As soon as the voltage at Terminal 7 exceeds the potential set at the base of  $Q_8$  by resistors  $R_{11}$  and  $R_{12}$ ,  $Q_7$  turns on, and  $Q_6$  supplies base current to  $Q_5$  and  $Q_{10}$ . Transistor  $Q_5$  discharges the capacitor through  $R_4$  until the base bias of  $Q_7$  falls below that of  $Q_8$  at which time,  $Q_7$  turns off, and the cycle repeats.

The sawtooth generated at the base of  $Q_4$  appears across  $R_3$  and turns off  $Q_3$  whenever the sawtooth voltage rises to a value that exceeds the bias set at Terminal 8. By adjusting the potential at Terminal 8, the duty cycle at the pre-drive output (Terminal 1) may be changed. The phase detector is isolated from the remainder of the circuit by  $R_{31}$ ,  $Z_2$ ,  $Q_{15}$  and  $Q_{16}$ . The phase detector consists of the comparator  $Q_{22}$  and  $Q_{23}$ , and the gated current source  $Q_{18}$ . Negative going sync pulses at Terminal 3 turn off  $Q_{17}$ , and the current division between  $Q_{22}$  and  $Q_{23}$  is then determined by the phase relationship of the sync and the sawtooth waveform at Terminal 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents flow in the collectors of  $Q_{22}$  and  $Q_{23}$  during each half of the sync pulse period. The current in  $Q_{22}$  is turned around by current mirror

$Q_{20}$  and  $Q_{21}$  so that there is no net output current at Terminal 5 for balanced conditions. When a phase offset occurs, current flows either in or out of Terminal 5. In circuit applications, this terminal is connected to Terminal 7 through an external low pass filter, thereby controlling the oscillator.

Shunt regulation for the circuit is obtained by using a  $V_{BE}$  and zener multiplier. Resistors  $R_{13}$  and  $R_{14}$  multiply the  $V_{BE}$  of  $Q_{11}$ , and the ratio of  $R_{15}$  and  $R_{16}$  multiplies the voltage of the zener diode  $Z_1$ .

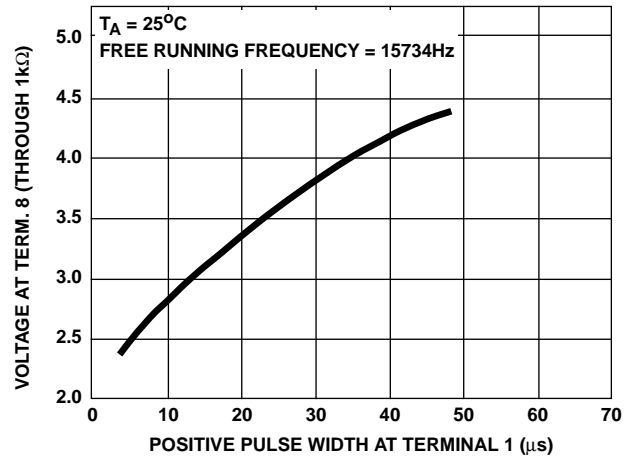


FIGURE 2. DUTY CYCLE AT THE PRE-DRIVE OUTPUT (TERMINAL 1) AS IT IS AFFECTED BY THE INPUT AT TERMINAL 8

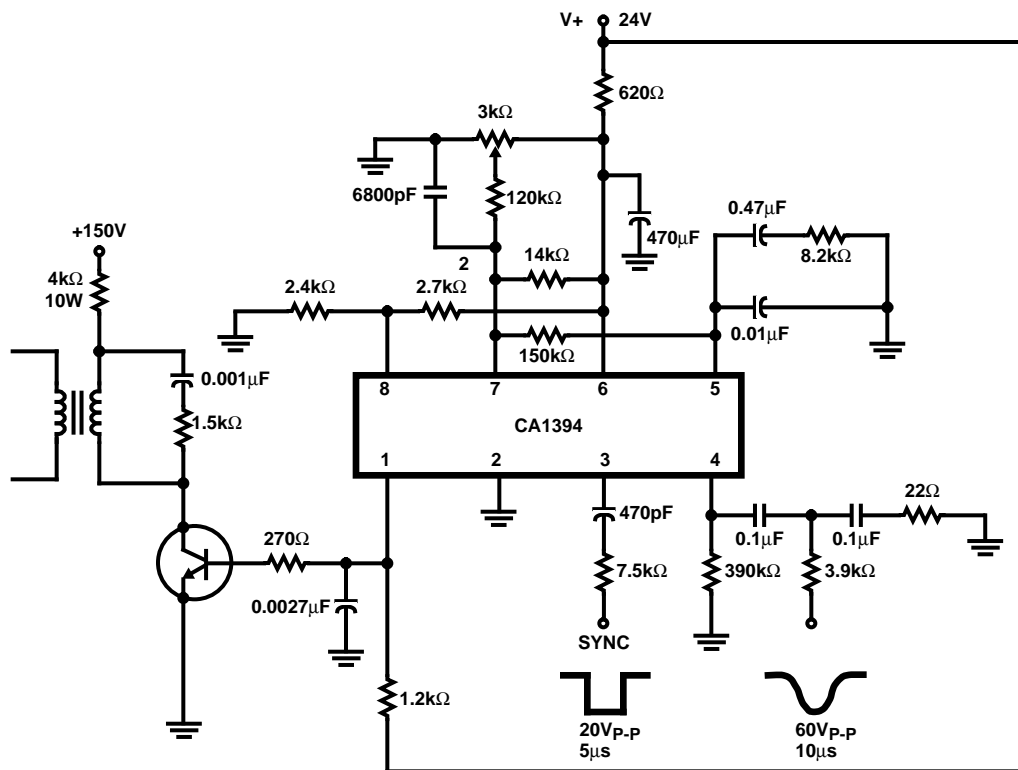


FIGURE 3. TYPICAL CIRCUIT APPLICATION