NIS5101

Advance Information

Smart Hot Plug

The Smart Hot Plug is a controller/FET IC that saves design time and reduces the number of components required for a complete hot swap application. It is designed to allow safe insertion and removal of electronic equipment to -48 volt backplanes. This chip features simplicity of use combined with an integrated solution.

The Smart Hot Plug includes user selectable undervoltage and overvoltage lockout levels. It also has adjustable current limiting that can be reduced from the maximum level with a single resistor. Operation at the maximum current level requires no extra external components. An internal temperature shutdown circuit greatly increases the reliability of this device.

Features

- Integrated Power Device
- 100 Volt Operation
- Thermal Limit Protection
- Adjustable Current Limit
- No External Current Shunt Required
- Undervoltage & Overvoltage Lockouts
- 5 Amp Continuous Operation

Typical Applications

- -48 V Telecom Power Systems
- High Availability Systems
- Electronic Circuit Breaker
- Current Inrush Limiting Circuits

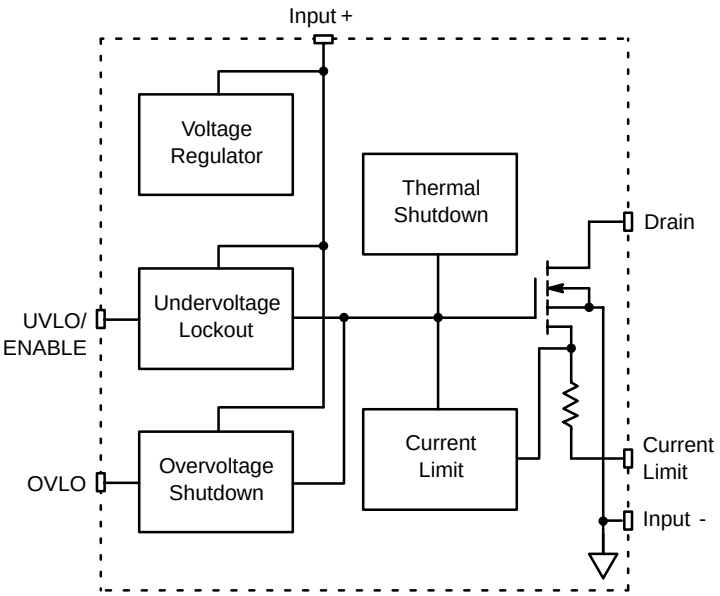

Figure 1. Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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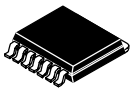
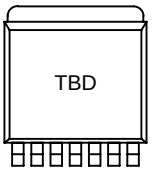
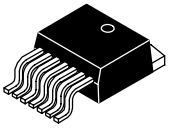
MARKING DIAGRAMS

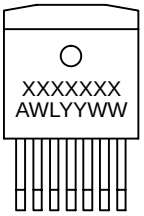


S-P AK
TBD SUFFIX
CASE 936J





D²PAK
TBD SUFFIX
CASE 936H



XXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NIS5101B1T1	D²PAK Latch Off	TBD
NIS5101B2T1	D²PAK Auto-Retry	TBD
NIS5101E1T1	S-P AK Latch Off	TBD
NIS5101E2T1	S-P AK Auto-Retry	TBD

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1, 2	Input -	Negative input voltage to the device. This is used as the internal reference for the IC.
3	Current Limit	This pin is shorted to the Input - pin for maximum current limit setting. If a reduced current limit level is desired, a series resistor is added between this pin and the Input - pin.
4	Drain	Drain of power FET, which is also the switching node for the load.
5	OVLO	The overvoltage shutdown point is programmed by a resistor from this pin to the Input + supply.
6	UVLO/ENABLE	A resistor from Input + to the UVLO pin adjusts the voltage at which the device will turn on. An open drain device can be connected to this pin, which will inhibit operation, when in its low impedance state.
7	Input +	Positive input voltage to the device.

MAXIMUM RATINGS (Maximum ratings are those, that, if exceeded, may cause damage to the device. Electrical Characteristics are not guaranteed over this range.)

Rating	Symbol	Value	Unit
Input Voltage, Operating (Input + to Input -) Transient (1 second) Steady-State	V_{in}	 -0.3 to 110 -0.3 to 100	V
Drain Voltage, Operating (Drain to Input -) Transient (1 second) Steady-State	V_{DD}	 -0.3 to 110 -0.3 to 100	V
Drain Current, Peak	I_{Dpk}	-	I
Thermal Resistance, Junction-to-Air 0.1 in^2 copper 0.5 in^2 copper	Q_{JA}	 - -	°C/W
Thermal Resistance, Junction-to-Lead (Pin 1)[2]	Q_{JL}	-	°C/W
Power Dissipation @ T_A = 25°C SPAK D^2PAK	P_{max}	 - -	W
Energy Rating SPAK D^2PAK	E_{max}	 - -	J
Operating Temperature Range	T_j	-40 to 175	°C
Non-Operating Temperature Range	T_j	-55 to 175	°C
Lead Temperature, Soldering (?? Sec)	T_L	-	°C
Drain Current, Peak (Internally Limited)	I_{pk}	25	A
Thermal Resistance, Junction-to-Air 0.5 in^2 copper - SPAK 1.0 in^2 copper - SPAK 0.5 in^2 copper - D^2PAK 1.0 in^2 copper - D^2PAK	$R_{\theta JA}$	 75 43 70 40	°C/W
Power Dissipation @ T_A = 25°C (T_J = 130°C) 0.5 in^2 copper - SPAK 1.0 in^2 copper - SPAK 0.5 in^2 copper - D^2PAK 1.0 in^2 copper - D^2PAK	P_{max}	 1.4 2.4 1.5 2.6	W

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: Vinput - = -48 volts, C_L = 470 μF, T_j = 25°C for typical values. For min/max values T_j is the applicable junction temperature.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER FET					
Charging Time (Turn-On to Rated Max Current)	t_{chg}	-	5.0	-	ms
ON Resistance	R_{DSon}	-	36	40	mΩ
Zero Gate Voltage Drain Current (V_{DS} = 100 V_{dc}, V_{GS} = 0 V_{dc})	I_{DSS}	-	10	-	μA
Output Capacitance (V_{DS} = 100 V_{dc}, V_{GS} = 0 V_{dc}, f = 1.0 MHz)	-	-	-	-	pF
Source-Drain Diode Characteristics					
Forward On-Voltage (I_S = 5.0 A, V_{GS} = 0 V (Note 1)	V_{SD}	-	0.8	1.0	V
Reverse Recovery Time (I_S = 5.0 A, V_{GS} = 0 V, dI_S/dt = 100	t_{rr}	-	-	-	ns
A/μs (Notes 1 and 2)	t_a	-	-	-	ns
	t_b	-	-	-	ns
Reverse Recovery Stored Charge (Above Conditions)	Q_{BB}	-	-	-	μC
Continuous Current (T_A = 25°C, 0.5 in^2 Pad)	I_{Davg}	-	5.0	-	A
THERMAL LIMIT					
Shutdown Temperature (Note 3)	T_{SD}	170	180	190	°C
Hysteresis (Note 3)	T_{hyst}	8.0	10	12	°C
OVER/UNDERVOLTAGE					
Turn-On Voltage (UVLO Pin Open)	V_{on}	41	44	47	V
Hysteresis ($Rext_{UVLO}$ = ∞)	V_{hyst}	6.0	6.5	7.0	V
Turn-On Voltage ($Rext_{UVLO}$ = 270 kΩ)	V_{on}	30	32	34	V
Hysteresis ($Rext_{UVLO}$ = 270 kΩ)	V_{hyst}	4.2	4.6	5.0	V
Zener Voltage (UVLO Pin Voltage at Turn-On)	V_Z	15.2	16	16.8	V
OVLO Threshold (Input + Increasing, R_{OV} = ∞)	-	109	111	113	V
OVLO Hysteresis (Input + Decreasing, R_{OV} = ∞)	-	7.0	8.0	9.0	V
OVLO Threshold (Input + Increasing, R_{OV} = 680 k)	-	81	83	85	V
OVLO Hysteresis (Input + Decreasing, R_{OV} = 680 k)	-	4.3	5.3	6.3	V
CURRENT LIMIT					
Current Limit (I_{LIMIT} Pin Shorted to Input -)	I_{LIM}	17	20	23	A
Current Limit (1000 Ω between I_{LIMIT} and Input -)	I_{LIM}	6.0	7.0	8.0	A
Response Time for Short Circuit	t_{off}	-	3.0	-	μs
Overshoot (Short Applied to Output, dI_S/dt = 100 A/μs)	I_{MAX}	-	40	-	A
TOTAL DEVICE					
Bias Current (Operational)	I_{LIM}	-	1.4	-	mA
Bias Current (Non-Operational) (V_{input} = 30 V, R_{UVLO} = ∞)	I_{LIM}	-	800	-	μA
Minimum Operating Voltage (R_{UVLO} = 22 k)	Vin_{min}	-	17	-	V

1. Pulse Test: Pulse width 300 μs, duty cycle 2%.
2. Switching characteristics are independent of operating junction temperatures.
3. Verified by design.

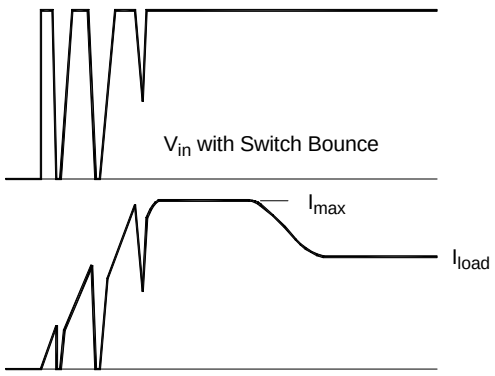


Figure 2. Timing Diagram

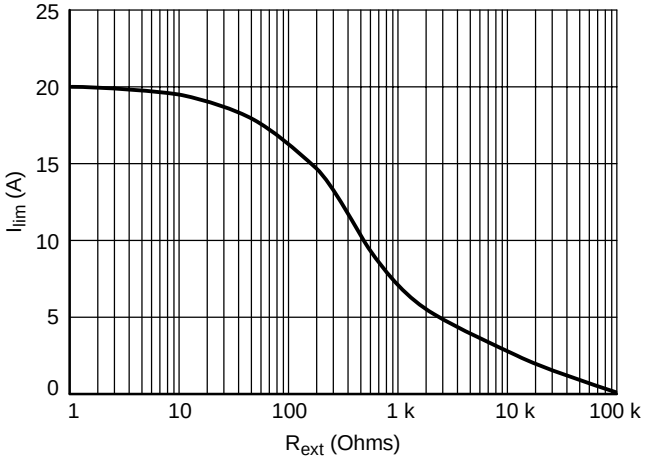


Figure 3. Current Limit Adjustment

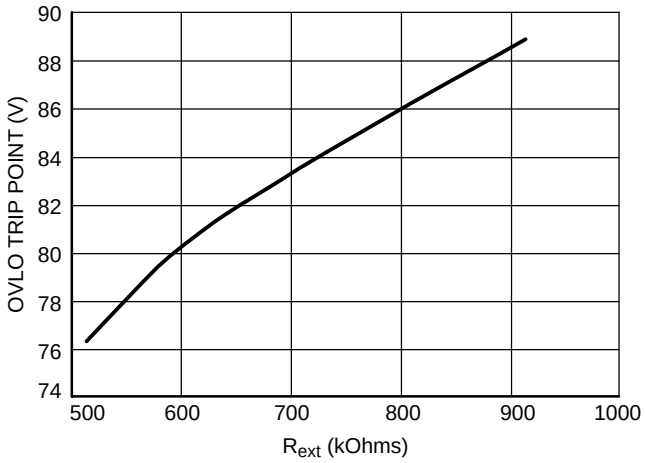


Figure 4. OVLO Adjustment

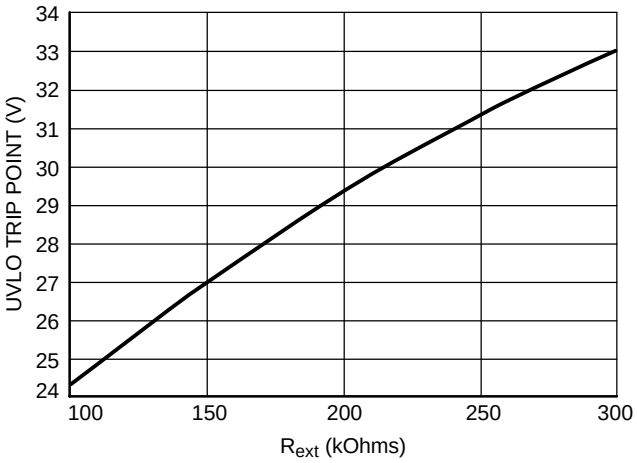


Figure 5. UVLO Adjustment

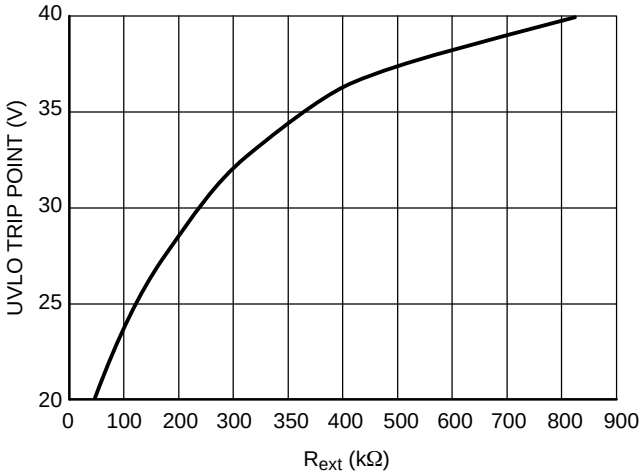


Figure 6. UVLO versus Resistance

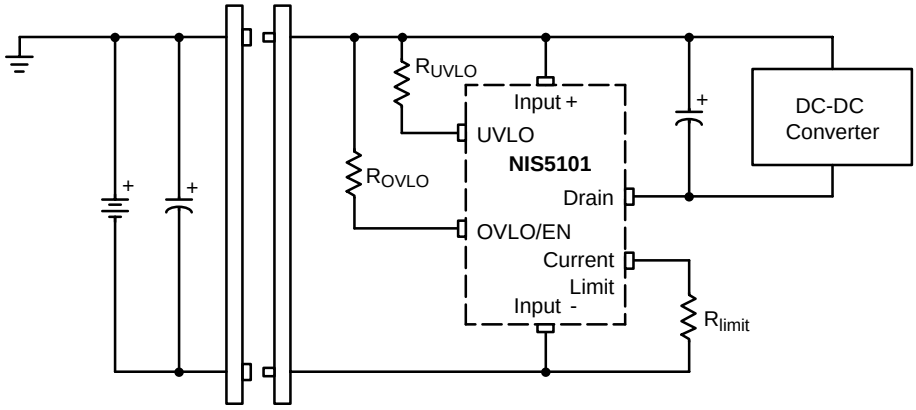


Figure 7. Typical Application

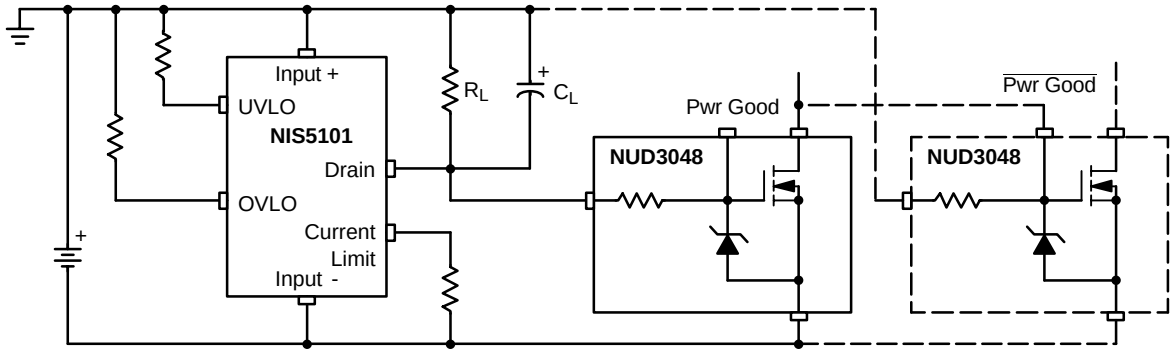


Figure 8. Power Good Signal Circuit

OPERATION

The Smart Hot Plug monitors the input voltage by sensing the voltage across the Input + to Input - pins. The undervoltage lockout circuit allows the internal FET to turn on, once its threshold is reached. At turn-on, the FET drive is enabled by applying the drive voltage via a high impedance gate drive circuit. This allows the current to gradually ramp up over a period of approximately 1.0 ms.

When the current reaches its maximum allowable level, the current limit circuit reduces the gate drive to a level that holds the current constant. The current will reduce from its maximum level when the output capacitor is fully charged, or when the unit reaches its thermal limit.

Circuit Description

Undervoltage Lockout: The UVLO circuit holds the chip off when the input voltage is less than the turn-on limit. It includes internal hysteresis to assure clean on/off switching. An internal divider sets the turn-on voltage level at 44 volts. This voltage can be reduced by adding an external resistor from the UVLO pin to the Input + pin. The equivalent circuit is shown in Figure 9.

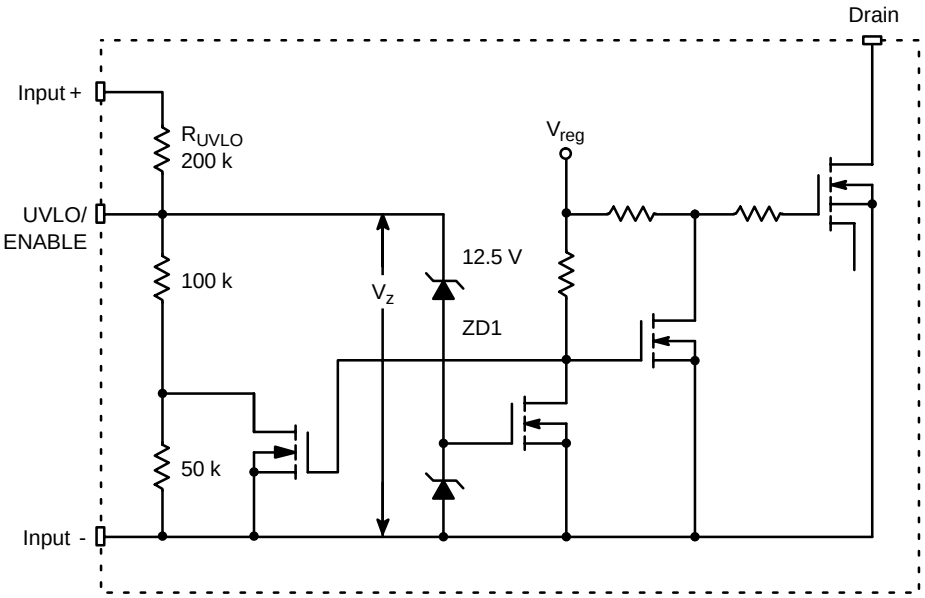


Figure 9. Undervoltage Lockout Circuit

The equation for the UVLO turn-on voltage is:

$$R_{UVLO} = \frac{215\ V_{in} - 2970}{46.8 - V_{in}}$$

where R_{UVLO} is in kΩ.

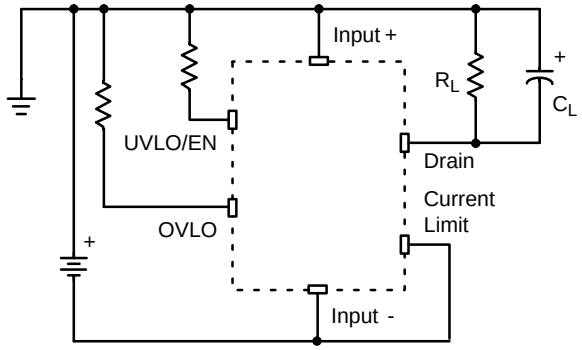


Figure 10.

Where V_{in} is the desired turn-on voltage, and R_{UVLO} is the programming resistance from the UVLO pin to the Input + pin.

To reduce nuisance tripping due to transients and noise spikes, a capacitor may be added from the UVLO pin to the Input – pin. This will create a low pass filter with a cutoff frequency of f. The required capacitance on this pin is:

$$C = \frac{1}{2\pi \cdot f\left[150\ k + \left(\frac{R_{UVLO} \cdot 200\ k}{R_{UVLO} + 200\ k}\right)\right]}$$

Overvoltage Lockout: The overvoltage shutdown circuit is an optional protection feature that can be disabled by simply grounding the OVLO pin.

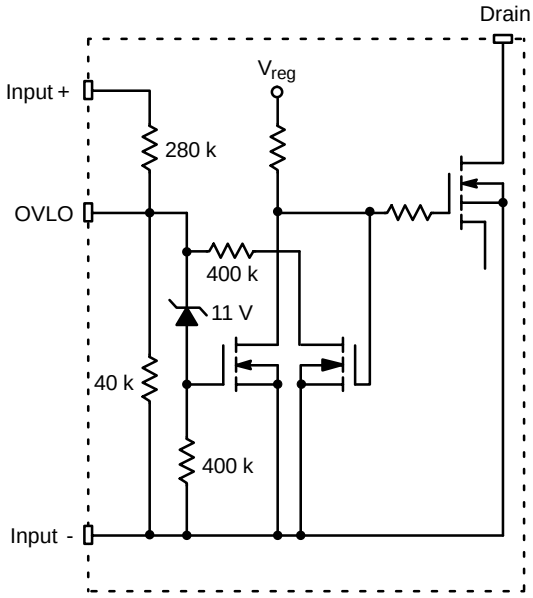


Figure 11.

This circuit contains an internal zener diode/resistor combination in series with the gate of a FET. When the input + to input - voltage reaches a level sufficient to apply the required gate voltage to the FET, operation of the Smart Hot Plug will be inhibited. There is a hysteresis circuit built in that will eliminate on/off bursts due to noise on the input.

The equation for the OVLO trip point is:

$$R_{OVLO} = \frac{290\ V_{in} - 3200}{113.7\ - V_{in}}$$

Where R_{OVLO} is the overvoltage programming resistor from the OVLO pin to Input +, and V_{in} is the desired trip point for the overvoltage shutdown to occur.

Similar to the undervoltage lockout circuit, the noise sensitivity of this circuit can be reduced by adding a capacitor from the OVLO pin to Input -. The capacitor required for the desired pole frequency is:

$$C_{OVLO} = \frac{(1 + 31.3 \cdot 10^{-6} \cdot R_{OVLO})}{2\pi f \cdot R_{OVLO}}$$

Temperature Limit: The temperature limit circuit senses the temperature of the Power FET and removes the gate drive if the maximum level is exceeded. There is a nominal hysteresis of 10°C for this circuit. After a thermal shutdown, the device will automatically restart when the temperature drops to a safe level as determined by the hysteresis.

Current Limit: The current limit for the Smart Hot Plug, is a simple, single level limit. In this device, the maximum current is limited by an internal circuit. The limit level can be set by a single external resistor. The current limit will not shut down the device, but only restrict the maximum current allowable. If a high level of current occurs for a substantial period of time, the part may overheat, at which time the thermal limit circuit will shut down the device. Once it is shut down, restart will depend on the current limit option selected (hysteretic or latching).

The Smart Hot Plug uses a SENSEFET™ to measure the Drain current. The SENSEFET develops a voltage across the sense resistor, which is internal to this device. If the voltage drop across this resistor reaches 150 millivolts, the current limit circuit will reduce the gate drive of the FET to maintain a safe level of current.

The negative end of the sense resistor is available at the current limit pin for external adjustment. If the device is to be used at its maximum current rating, this pin should be connected to the Input - pin. If it is desired to reduce the maximum current limit level, an external resistor can be added.

$$E = 1/2 \cdot C_L \cdot V^2$$

There is a minimum current limit level and lower current limitations cannot be achieved regardless of the value used for the current limit resistor. This occurs because the voltage generated at the source of the FET is derived from the voltage that exists at the drain. Since the trip point is 150 millivolts, if the voltage at the drain terminal is less than 150 millivolts, the source voltage can never reach this level, and the device will not current limit.

Turn-on Surge: During the turn-on event, there is a large amount of energy dissipated due to the linear operation of the power device. Over this period of time, the energy absorbed by the power FET does not have time to be conducted to the surface of the part for dissipation by conduction or convection means.

The energy rating for a given device is listed in the absolute maximum ratings table. This rating is the amount of energy that the device can absorb before the thermal limit circuit will shut the unit down. The calculation for the energy is very simple if the load is not operational when the hot swap is turned on. In this case the energy is given by the equation:

where:

C_L is the total load capacitance (F)

V is the input voltage (v)

If the load will be active during the charging event, the load current must also be considered. The energy required to charge the capacitor will not change, however, the losses due to the load current must also be calculated over the period of time from when the load begins to draw current, and when the current is reduced to its steady state level. The equation for this will vary dependent on whether the load is a constant current, constant resistance, constant power or non-linear , and at what voltage the load begins to draw current.

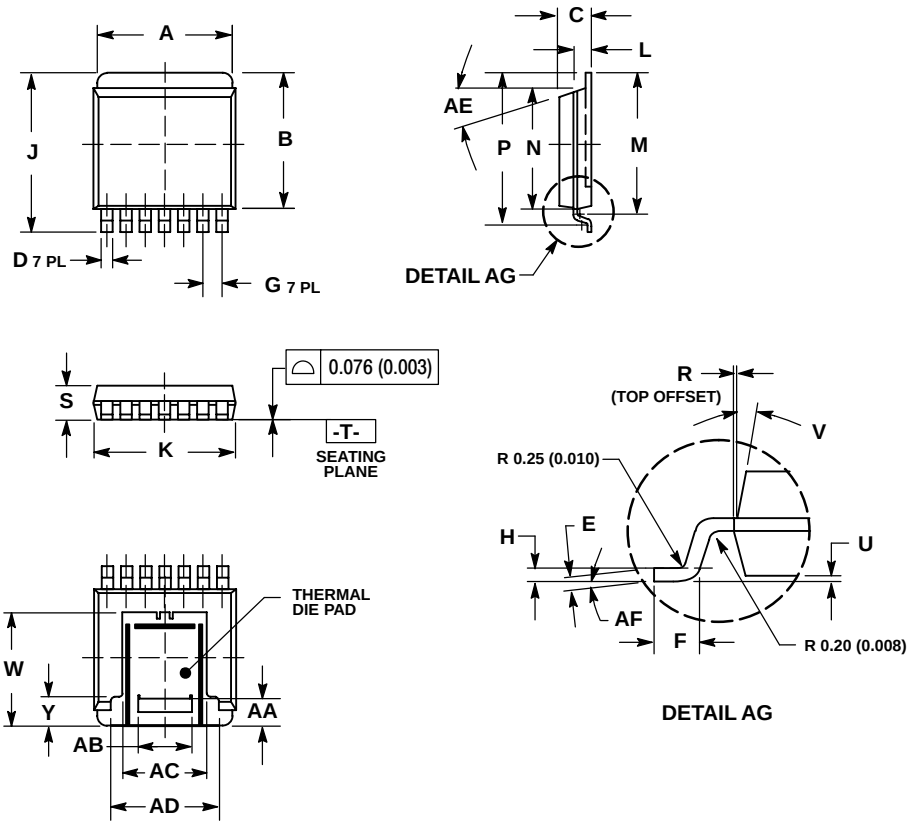
Enable: The UVLO pin serves a double function. In addition to the UVLO function, it can also be used to disable the chip when it is pulled to the input- rail, with an open drain type of device. The open drain device must be able to sink the current from the internal 100 kOhm resistor in parallel with the external adjustment resistor, at the highest input voltage required.

The turn on voltage at the UVLO pin is approximately 15 volts, so any device that can sink the required amount of current should have a saturation voltage well below this requirement. The maximum sinking current can be calculated by the following equation:

$$I_{enable(max)} = V_{in(max)} \frac{100\ k + R_{UVLO}}{100\ k \cdot R_{UVLO}}$$

PACKAGE DIMENSIONS

S-PAK™
TBD SUFFIX
CASE 936J-01
ISSUE O



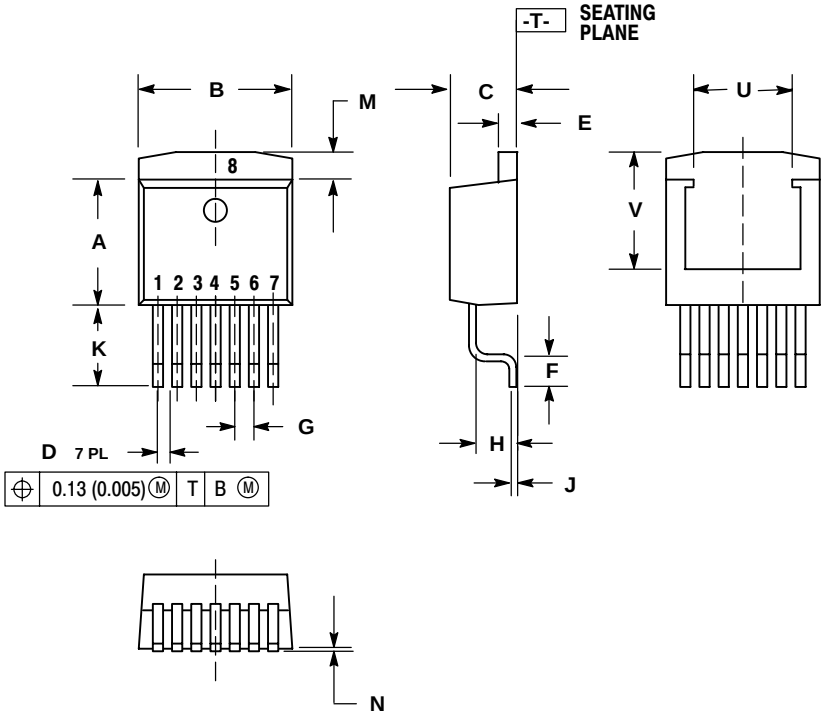
DETAIL AG

NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.350	0.360	8.89	9.14
B	0.350	0.360	8.89	9.14
C	0.070	0.080	1.78	2.03
D	0.026	0.030	0.66	0.76
E	0.005	0.015	0.13	0.38
F	0.031	0.041	0.79	1.04
G	0.050 BSC		1.270 BSC	
H	0.008	0.012	0.199	0.301
J	0.410	0.420	10.41	10.67
K	0.365	00.375	9.27	9.53
L	0.040 REF		1.02 REF	
M	0.361	0.367	9.16	9.31
N	0.310	0.320	7.87	8.13
P	0.394	0.400	10.00	10.16
R	0.002	---	0.05	---
S	0.070	0.080	1.78	2.03
U	0.001	0.005	0.03	0.13
V	12 °		12 °	
W	0.296 REF		7.52 REF	
Y	0.075 REF		1.91 REF	
AA	0.071 REF		1.81 REF	
AB	0.140 REF		3.56 REF	
AC	0.220 REF		5.58 REF	
AD	0.281 REF		7.14 REF	
AE	12 °		12 °	
AF	3 °	6 °	3 °	6 °

PACKAGE DIMENSIONS

7 LEAD D^{2}PAK (DPS7)
TBD SUFFIX
CASE 936H-01
ISSUE O



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS B AND M.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.058	0.078	1.41	1.98
G	0.050 BSC		1.27 BSC	
H	0.100	0.110	2.54	2.79
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10
U	0.256 REF		6.50 REF	
V	0.305 REF		7.75 REF	

The product described herein (NIS5101), may be covered by U.S. patents. Other patents may be pending, including ON Semiconductor disclosures ONS00448 and ONS00458.
SENSEFET is a trademark of Semiconductor Components Industries, LLC.

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ON Semiconductor Website: http://onsemi.com

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