M29W400T
M29W400B

4 Mbit (512Kb x8 or 256Kb x16, Boot Block) Low Voltage Single Supply Flash Memory

NOT FOR NEW DESIGN

- **M29W400T and M29W400B are replaced respectively by the M29W400BT and M29W400BB**
- 2.7V to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- FAST ACCESS TIME: 90ns
- FAST PROGRAMMING TIME
  - 10µs by Byte / 16µs by Word typical
- PROGRAM/ERASE CONTROLLER (P/E.C.)
  - Program Byte-by-Byte or Word-by-Word
  - Status Register bits and Ready/Busy Output
- MEMORY BLOCKS
  - Boot Block (Top or Bottom location)
  - Parameter and Main blocks
- BLOCK, MULTI-BLOCK and CHIP ERASE
- MULTI BLOCK PROTECTION/TEMPORARY UNPROTECTION MODES
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- LOW POWER CONSUMPTION
  - Stand-by and Automatic Stand-by
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- 20 YEARS DATA RETENTION
  - Defectivity below 1ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code, M29W400T: 00EEh
  - Device Code, M29W400B: 00EFh

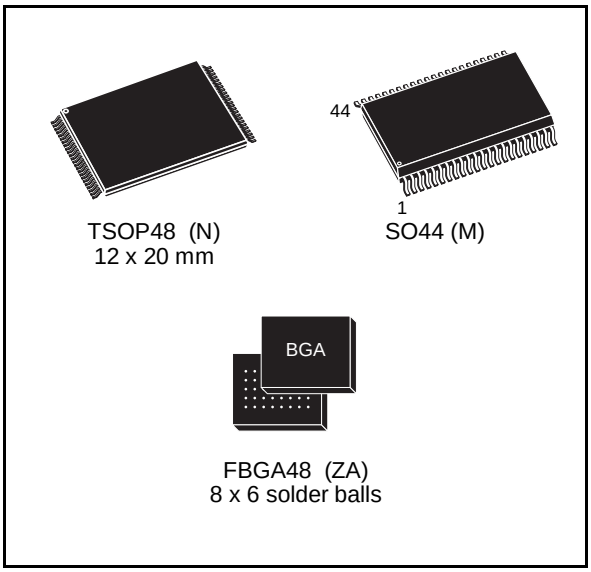
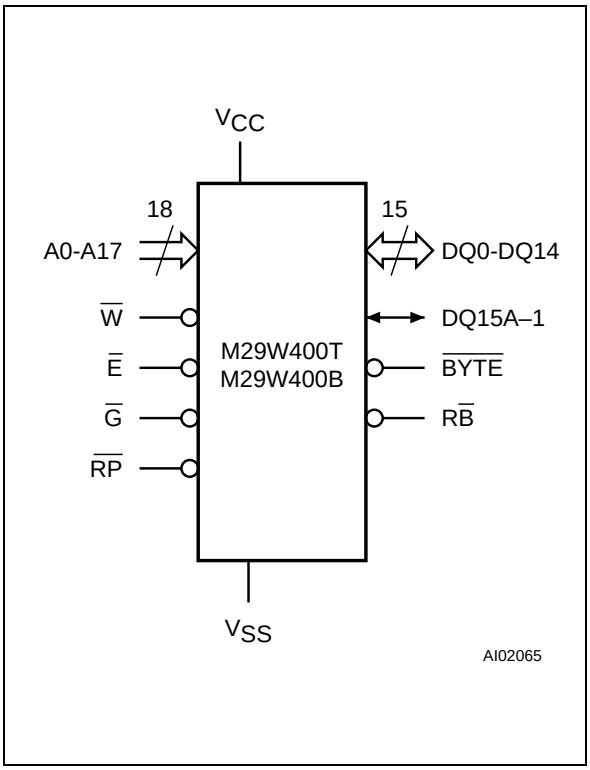


Figure 1. Logic Diagram

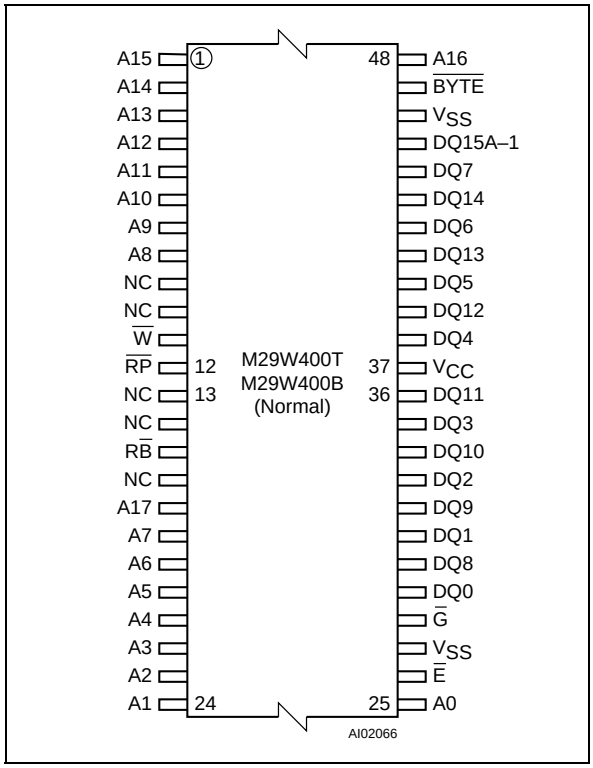


DESCRIPTION

The M29W400 is a non-volatile memory that may be erased electrically at the block or chip level and programmed in-system on a Byte-by-Byte or Word-by-Word basis using only a single 2.7V to 3.6V V_{CC} supply. For Program and Erase operations the necessary high voltages are generated internally. The device can also be programmed in standard programmers.

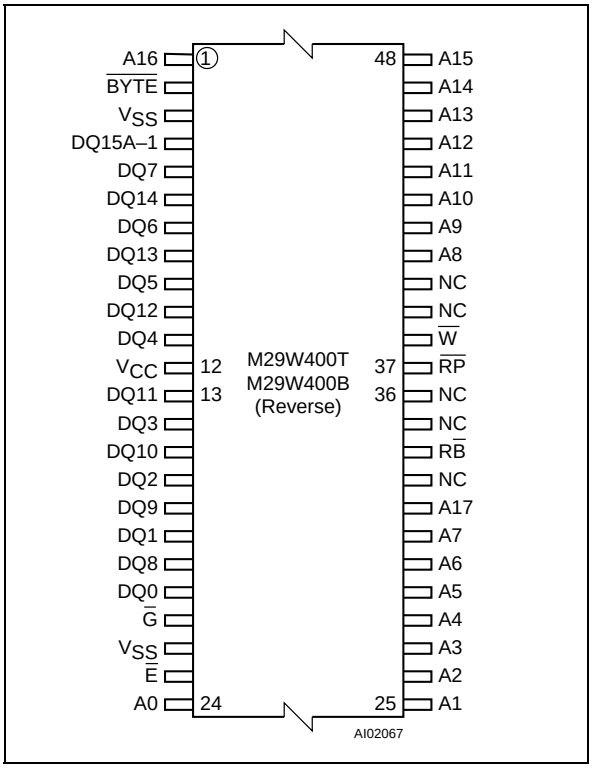
The array matrix organisation allows each block to be erased and reprogrammed without affecting other blocks. Blocks can be protected against programing and erase on programming equipment,

Figure 2A. TSOP Pin Connections



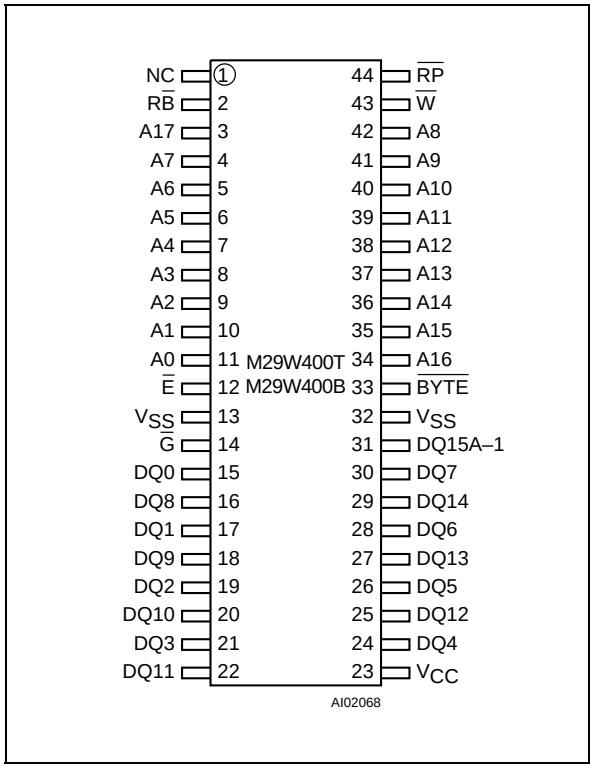
Warning: NC = Not Connected.

Figure 2B. TSOP Reverse Pin Connections



Warning: NC = Not Connected.

Figure 2C. SO Pin Connections

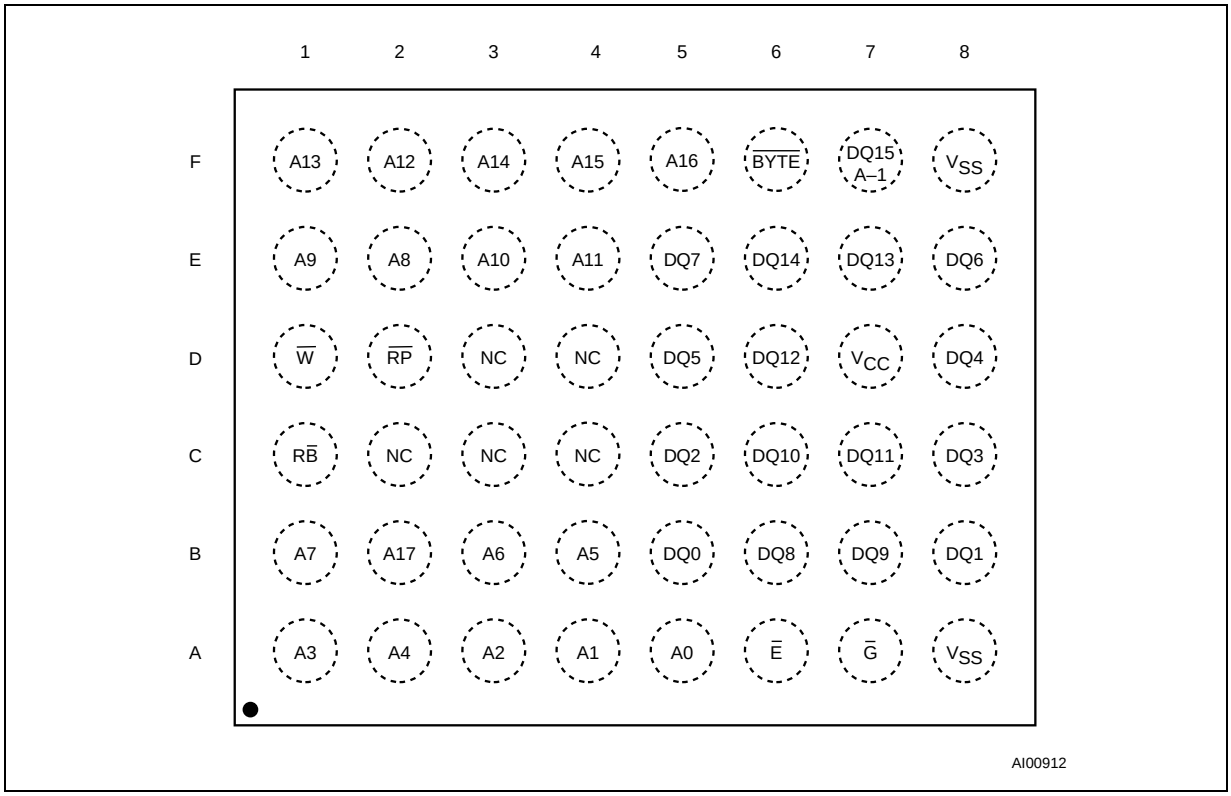


Warning: NC = Not Connected.

Table 1. Signal Names

A0-A17	Address Inputs
DQ0-DQ7	Data Input/Outputs, Command Inputs
DQ8-DQ14	Data Input/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset / Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organisation
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2D. FBGA Package Ball Out (Top View)



Warning: NC = Not Connected.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (3)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.6 to 5	V
V_{CC}	Supply Voltage	–0.6 to 5	V
$V_{(A9, \overline{E}, \overline{G}, \overline{RP})}$ (2)	A9, $\overline{E}$, $\overline{G}$, $\overline{RP}$ Voltage	–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Depends on range.

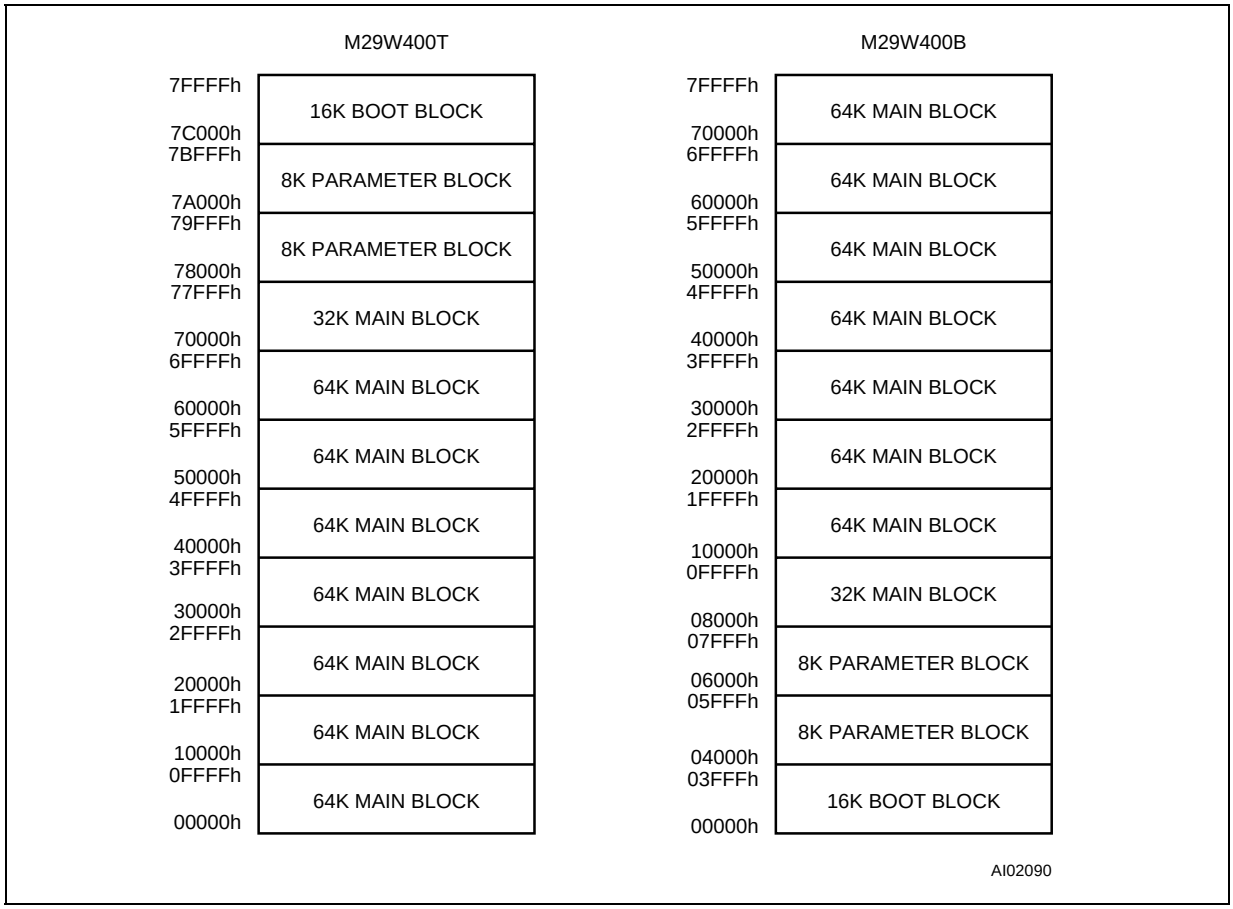
DESCRIPTION (Cont'd)

and temporarily unprotected to make changes in the application. Each block can be programmed and erased over 100,000 cycles.

Instructions for Read/Reset, Auto Select for reading the Electronic Signature or Block Protection status, Programming, Block and Chip Erase, Erase Suspend and Resume are written to the device in cycles of commands to a Command Interface using standard microprocessor write timings.

The device is offered in TSOP48 (12 x 20mm), SO44 and FBGA48 (8 x 6 balls, 0.8mm pitch) packages. Both normal and reverse pinouts are available for the TSOP48 package.

Figure 3. Memory Map and Block Address Table (x8)



Organisation

The M29W400 is organised as 512K x8 or 256K x16 bits selectable by the $\overline{BYTE}$ signal. When $\overline{BYTE}$ is Low the Byte-wide x8 organisation is selected and the address lines are DQ15A–1 and A0-A17. The Data Input/Output signal DQ15A–1 acts as address line A–1 which selects the lower or upper Byte of the memory word for output on DQ0-DQ7, DQ8-DQ14 remain at High impedance. When $\overline{BYTE}$ is High the memory uses the address inputs A0-A17 and the Data Input/Outputs DQ0-DQ15. Memory control is provided by Chip Enable $\overline{E}$, Output Enable $\overline{G}$ and Write Enable $\overline{W}$ inputs.

A Reset/Block Temporary Unprotection $\overline{RP}$ tri-level input provides a hardware reset when pulled Low, and when held High (at V_{ID}) temporarily unprotects blocks previously protected allowing them to be programed and erased. Erase and Program operations are controlled by an internal Program/Erase Controller (P/E.C.). Status Register data output on DQ7 provides a Data Polling signal, and DQ6 and DQ2 provide Toggle signals to indicate the state of the P/E.C operations. A Ready/Busy $\overline{RB}$ output indicates the completion of the internal algorithms.

Memory Blocks

The devices feature asymmetrically blocked architecture providing system memory integration. Both M29W400T and M29W400B devices have an array of 11 blocks, one Boot Block of 16 KBytes or 8 KWords, two Parameter Blocks of 8 KBytes or 4 KWords, one Main Block of 32 KBytes or 16 KWords and seven Main Blocks of 64 KBytes or 32 KWords. The M29W400T has the Boot Block at the top of the memory address space and the M29W400B locates the Boot Block starting at the bottom. The memory maps are showed in Figure 3. Each block can be erased separately, any combination of blocks can be specified for multi-block erase or the entire chip may be erased. The Erase operations are managed automatically by the P/E.C. The block erase operation can be suspended in order to read from or program to any block not being ersased, and then resumed.

Block protection provides additional data security. Each block can be separately protected or unprotected against Program or Erase on programming equipment. All previously protected blocks can be temporarily unprotected in the application.

Table 3A. M29W400T Block Address Table

Address Range (x8)	Address Range (x16)	A17	A16	A15	A14	A13	A12
00000h-0FFFFh	00000h-07FFFh	0	0	0	X	X	X
10000h-1FFFFh	08000h-0FFFFh	0	0	1	X	X	X
20000h-2FFFFh	10000h-17FFFh	0	1	0	X	X	X
30000h-3FFFFh	18000h-1FFFFh	0	1	1	X	X	X
40000h-4FFFFh	20000h-27FFFh	1	0	0	X	X	X
50000h-5FFFFh	28000h-2FFFFh	1	0	1	X	X	X
60000h-6FFFFh	30000h-37FFFh	1	1	0	X	X	X
70000h-77FFFh	38000h-3BFFFh	1	1	1	0	X	X
78000h-79FFFh	3C000h-3CFFFh	1	1	1	1	0	0
7A000h-7BFFFh	3D000h-3DFFFh	1	1	1	1	0	1
7C000h-7FFFFh	3E000h-3FFFFh	1	1	1	1	1	X

Table 3B. M29W400B Block Address Table

Address Range (x8)	Address Range (x16)	A17	A16	A15	A14	A13	A12
00000h-03FFFh	00000h-01FFFh	0	0	0	0	0	X
04000h-05FFFh	02000h-02FFFh	0	0	0	0	1	0
06000h-07FFFh	03000h-03FFFh	0	0	0	0	1	1
08000h-0FFFFh	04000h-07FFFh	0	0	0	1	X	X
10000h-1FFFFh	08000h-0FFFFh	0	0	1	X	X	X
20000h-2FFFFh	10000h-17FFFh	0	1	0	X	X	X
30000h-3FFFFh	18000h-1FFFFh	0	1	1	X	X	X
40000h-4FFFFh	20000h-27FFFh	1	0	0	X	X	X
50000h-5FFFFh	28000h-2FFFFh	1	0	1	X	X	X
60000h-6FFFFh	30000h-37FFFh	1	1	0	X	X	X
70000h-7FFFFh	38000h-3FFFFh	1	1	1	X	X	X

Bus Operations

The following operations can be performed using the appropriate bus cycles: Read (Array, Electronic Signature, Block Protection Status), Write command, Output Disable, Standby, Reset, Block Protection, Unprotection, Protection Verify, Unprotection Verify and Block Temporary Unprotection. See Tables 4 and 5.

Command Interface

Instructions, made up of commands written in cycles, can be given to the Program/Erase Controller through a Command Interface (C.I.). For added data protection, program or erase execution starts after 4 or 6 cycles. The first, second, fourth and fifth cycles are used to input Coded cycles to the C.I. This Coded sequence is the same for all Program/Erase Controller instructions. The 'Command' itself and its confirmation, when applicable, are given on the third, fourth or sixth cycles. Any incorrect command or any improper command sequence will reset the device to Read Array mode.

Instructions

Seven instructions are defined to perform Read Array, Auto Select (to read the Electronic Signature or Block Protection Status), Program, Block Erase, Chip Erase, Erase Suspend and Erase Resume. The internal P/E.C. automatically handles all timing and verification of the Program and Erase operations. The Status Register Data Polling, Toggle, Error bits and the $\overline{RB}$ output may be read at any time, during programming or erase, to monitor the progress of the operation.

Instructions are composed of up to six cycles. The first two cycles input a Coded sequence to the Command Interface which is common to all instructions (see Table 8). The third cycle inputs the instruction set-up command. Subsequent cycles output the addressed data, Electronic Signature or Block Protection Status for Read operations. In order to give additional data protection, the instructions for Program and Block or Chip Erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For an Erase instruction (Block or Chip), the fourth and fifth cycles input a further Coded sequence before the Erase confirm command on the sixth cycle. Erasure of a memory block may be suspended, in order to read data from another block or to program data in another block, and then resumed.

When power is first applied or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Array.

SIGNAL DESCRIPTIONS

See Figure 1 and Table 1.

Address Inputs (A0-A17). The address inputs for the memory array are latched during a write operation on the falling edge of Chip Enable $\overline{E}$ or Write Enable $\overline{W}$. In Word-wide organisation the address lines are A0-A17, in Byte-wide organisation DQ15A–1 acts as an additional LSB address line. When A9 is raised to V_{ID}, either a Read Electronic Signature Manufacturer or Device Code, Block Protection Status or a Write Block Protection or Block Unprotection is enabled depending on the combination of levels on A0, A1, A6, A12 and A15.

Data Input/Outputs (DQ0-DQ7). These Inputs/Outputs are used in the Byte-wide and Word-wide organisations. The input is data to be programmed in the memory array or a command to be written to the C.I. Both are latched on the rising edge of Chip Enable $\overline{E}$ or Write Enable $\overline{W}$. The output is data from the Memory Array, the Electronic Signature Manufacturer or Device codes, the Block Protection Status or the Status register Data Polling bit DQ7, the Toggle Bits DQ6 and DQ2, the Error bit DQ5 or the Erase Timer bit DQ3. Outputs are valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled and when $\overline{RP}$ is at a Low level.

Data Input/Outputs (DQ8-DQ14 and DQ15A–1). These Inputs/Outputs are additionally used in the Word-wide organisation. When $\overline{BYTE}$ is High DQ8-DQ14 and DQ15A–1 act as the MSB of the Data Input or Output, functioning as described for DQ0-DQ7 above, and DQ8-DQ15 are 'don't care' for command inputs or status outputs. When $\overline{BYTE}$ is Low, DQ8-DQ14 are high impedance, DQ15A–1 is the Address A–1 input.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High deselects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. The Chip Enable must be forced to V_{ID} during the Block Unprotection operation.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. When $\overline{G}$ is High the outputs are High impedance. $\overline{G}$ must be forced to V_{ID} level during Block Protection and Unprotection operations.

Write Enable ($\overline{W}$). This input controls writing to the Command Register and Address and Data latches.

Byte/Word Organization Select ($\overline{BYTE}$). The $\overline{BYTE}$ input selects the output configuration for the device: Byte-wide (x8) mode or Word-wide (x16) mode. When $\overline{BYTE}$ is Low, the Byte-wide mode is selected and the data is read and programmed on DQ0-DQ7. In this mode, DQ8-DQ14 are at high impedance and DQ15A–1 is the LSB address. When $\overline{BYTE}$ is High, the Word-wide mode is selected and the data is read and programmed on DQ0-DQ15.

Ready/Busy Output ($R\overline{B}$). Ready/Busy is an open-drain output and gives the internal state of the P/E.C. of the device. When $R\overline{B}$ is Low, the device is Busy with a Program or Erase operation and it will not accept any additional program or erase instructions except the Erase Suspend instruction. When $R\overline{B}$ is High, the device is ready for any Read, Program or Erase operation. The $R\overline{B}$ will also be High when the memory is put in Erase Suspend or Standby modes.

Reset/Block Temporary Unprotect Input ($\overline{RP}$). The $\overline{RP}$ Input provides hardware reset and protected block(s) temporary unprotection functions. Reset of the memory is acheived by pulling $\overline{RP}$ to V_{IL} for at least t_{PLPX}. When the reset pulse is given, if the memory is in Read or Standby modes, it will be available for new operations in t_{PHEL} after the rising edge of $\overline{RP}$. If the memory is in Erase, Erase Suspend or Program modes the reset will take t_{PLYH} during which the $R\overline{B}$ signal will be held at V_{IL}. The end of the memory reset will be indicated by the rising edge of $R\overline{B}$. A hardware reset during an Erase or Program operation will corrupt the data being programmed or the sector(s) being erased (see Table 14 and Figure 9).

Temporary block unprotection is made by holding $\overline{RP}$ at V_{ID}. In this condition previously protected blocks can be programmed or erased. The transition of $\overline{RP}$ from V_{IH} to V_{ID} must slower than t_{PHPHH}. When $\overline{RP}$ is returned from V_{ID} to V_{IH} all blocks temporarily unprotected will be again protected. See Table 15 and Figure 9.

V_{CC} Supply Voltage. The power supply for all operations (Read, Program and Erase).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

DEVICE OPERATIONS

See Tables 4, 5 and 6.

Read. Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register or the Block Protection Status. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory.

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when Chip Enable $\overline{E}$ is High and the P/E.C. is idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Automatic Standby. After 150ns of bus inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo-standby mode where consumption is reduced to the CMOS standby value, while outputs still drive the bus.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory. The manufacturer's code for STMicroelectronics is 20h, the device code is EEh for the M29W400T (Top Boot) and EFh for the M29W400B (Bottom Boot). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the M29W400. The Electronic Signature is output by a Read operation when the voltage applied to A9 is at V_{ID} and address inputs A1 is Low. The manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored. The codes are output on DQ0-DQ7.

The Electronic Signature can also be read, without raising A9 to V_{ID}, by giving the memory the Instruction AS. If the Byte-wide configuration is selected the codes are output on DQ0-DQ7 with DQ8-DQ14 at High impedance; if the Word-wide configuration is selected the codes are output on DQ0-DQ7 with DQ8-DQ15 at 00h.

Table 4. User Bus Operations (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{BYTE}$	A0	A1	A6	A9	A12	A15	DQ15 A–1	DQ8-DQ14	DQ0-DQ7
Read Word	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	A0	A1	A6	A9	A12	A15	Data Output	Data Output	Data Output
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	A0	A1	A6	A9	A12	A15	Address Input	Hi-Z	Data Output
Write Word	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	A0	A1	A6	A9	A12	A15	Data Input	Data Input	Data Input
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	A0	A1	A6	A9	A12	A15	Address Input	Hi-Z	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z
Block Protection(2,4)	V_{IL}	V_{ID}	V_{IL} Pulse	V_{IH}	X	X	X	X	V_{ID}	X	X	X	X	X
Blocks Unprotection(4)	V_{ID}	V_{ID}	V_{IL} Pulse	V_{IH}	X	X	X	X	V_{ID}	V_{IH}	V_{IH}	X	X	X
Block Protection Verify(2,4)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{ID}	A12	A15	X	X	Block Protect Status (3)
Block Unprotection Verify(2,4)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	V_{ID}	A12	A15	X	X	Block Protect Status (3)
Block Temporary Unprotection	X	X	X	V_{ID}	X	X	X	X	X	X	X	X	X	X

Notes: 1. X = V_{IL} or V_{IH}
2. Block Address must be given on A12-A17 bits.
3. See Table 6.
4. Operation performed on programming equipment.

Table 5. Read Electronic Signature (following AS instruction or with A9 = V_{ID})

Org.	Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{BYTE}$	A0	A1	Other Addresses	DQ15 A–1	DQ8-DQ14	DQ0-DQ7
Word-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	Don't Care	0	00h	20h
	Device Code	M29W400T	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Don't Care	0	00h	EEh
		M29W400B	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Don't Care	0	00h	EFh
Byte-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Don't Care	Don't Care	Hi-Z	20h
	Device Code	M29W400T	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Don't Care	Hi-Z	EEh
		M29W400B	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Don't Care	Hi-Z	EFh

Table 6. Read Block Protection with AS Instruction

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A12-A17	Other Addresses	DQ0-DQ7
Protected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	Don't Care	01h
Unprotected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	Don't Care	00h

Table 7. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Chip Erase Confirm
20h	Reserved
30h	Block Erase Resume/Confirm
80h	Set-up Erase
90h	Read Electronic Signature/ Block Protection Status
A0h	Program
B0h	Erase Suspend
F0h	Read Array/Reset

Block Protection. Each block can be separately protected against Program or Erase on programming equipment. Block protection provides additional data security, as it disables all program or erase operations. This mode is activated when both A9 and $\overline{G}$ are raised to V_{ID} and an address in the block is applied on A12-A17. The Block Protection algorithm is shown in Figure 14. Block protection is initiated on the edge of $\overline{W}$ falling to V_{IL}. Then after a delay of 100µs, the edge of $\overline{W}$ rising to V_{IH} ends the protection operations. Block protection verify is achieved by bringing $\overline{G}$, $\overline{E}$, A0 and A6 to V_{IL} and A1 to V_{IH}, while $\overline{W}$ is at V_{IH} and A9 at V_{ID}. Under these conditions, reading the data output will yield 01h if the block defined by the inputs on A12-A17 is protected. Any attempt to program or erase a protected block will be ignored by the device.

Block Temporary Unprotection. Any previously protected block can be temporarily unprotected in order to change stored data. The temporary unprotection mode is activated by bringing $\overline{RP}$ to V_{ID}. During the temporary unprotection mode the previously protected blocks are unprotected. A block can be selected and data can be modified by executing the Erase or Program instruction with the $\overline{RP}$ signal held at V_{ID}. When $\overline{RP}$ is returned to V_{IH}, all the previously protected blocks are again protected.

Block Unprotection. All protected blocks can be unprotected on programming equipment to allow updating of bit contents. All blocks must first be protected before the unprotection operation. Block unprotection is activated when A9, $\overline{G}$ and $\overline{E}$ are at V_{ID} and A12, A15 at V_{IH}. The Block Unprotection algorithm is shown in Figure 15. Unprotection is initiated by the edge of $\overline{W}$ falling to V_{IL}. After a delay of 10ms, the unprotection operation will end. Unprotection verify is achieved by bringing $\overline{G}$ and $\overline{E}$ to V_{IL} while A0 is at V_{IL}, A6 and A1 are at V_{IH} and A9 remains at V_{ID}. In these conditions, reading the output data will yield 00h if the block defined by the inputs A12-A17 has been succesfully unprotected. Each block must be separately verified by giving its address in order to ensure that it has been unprotected.

INSTRUCTIONS AND COMMANDS

The Command Interface latches commands written to the memory. Instructions are made up from one or more commands to perform Read Memory Array, Read Electronic Signature, Read Block Protection, Program, Block Erase, Chip Erase, Erase Suspend and Erase Resume. Commands are made of address and data sequences. The instructions require from 1 to 6 cycles, the first or first three of which are always write operations used to initiate the instruction. They are followed by either further write cycles to confirm the first command or execute the command immediately. Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security. Instructions are initialised by two initial Coded cycles which unlock the Command Interface. In addition, for Erase, instruction confirmation is again preceded by the two Coded cycles.

Table 8. Instructions (1)

Mne.	Instr.	Cyc.			1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
RD (2,4)	Read/Reset Memory Array	1+	**Addr.** (3,7)		X	Read Memory Array until a new write cycle is initiated.					
			Data		F0h						
		3+	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	Read Memory Array until a new write cycle is initiated.			
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	F0h				
AS (4)	Auto Select	3+	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	Read Electronic Signature or Block Protection Status until a new write cycle is initiated. See Note 5 and 6.			
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	90h				
PG	Program	4	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	Program Address	Read Data Polling or Toggle Bit until Program completes.		
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	A0h	Program Data			
BE	Block Erase	6	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	AAAAh	5555h	Block Address	Additional Block (8)
				Word	5555h	2AAAh	5555h	5555h	2AAAh		
			Data		AAh	55h	80h	AAh	55h	30h	30h
CE	Chip Erase	6	**Addr.** (3,7)	**Byte**	AAAAh	5555h	AAAAh	AAAAh	5555h	AAAAh	Note 9
				Word	5555h	2AAAh	5555h	5555h	2AAAh	5555h	
			Data		AAh	55h	80h	AAh	55h	10h	
ES (10)	Erase Suspend	1	**Addr.** (3,7)		X	Read until Toggle stops, then read all the data needed from any Block(s) not being erased then Resume Erase.					
			Data		B0h						
ER	Erase Resume	1	**Addr.** (3,7)		X	Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time					
			Data		30h						

Notes: 1. Commands not interpreted in this table will default to read array mode.
2. A wait of t_{PLYH} is necessary after a Read/Reset command if the memory was in an Erase or Program mode before starting any new operation (see Table 14 and Figure 9).
3. X = Don't Care.
4. The first cycles of the RD or AS instructions are followed by read operations. Any number of read cycles can occur after the command cycles.
5. Signature Address bits A0, A1 at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1 at V_{IL} will output Device code.
6. Block Protection Address: A0 at V_{IL}, A1 at V_{IH} and A12-A17 within the Block will output the Block Protection status.
7. For Coded cycles address inputs A15-A17 are don't care.
8. Optional, additional Blocks addresses must be entered within the erase timeout delay after last write entry, timeout status can be verified through DQ3 value (see Erase Timer Bit DQ3 description). When full command is entered, read Data Polling or Toggle bit until Erase is completed or suspended.
9. Read Data Polling, Toggle bits or RB until Erase completes.
10. During Erase Suspend, Read and Data Program functions are allowed in blocks not being erased.

Status Register Bits

P/E.C. status is indicated during execution by Data Polling on DQ7, detection of Toggle on DQ6 and DQ2, or Error on DQ5 and Erase Timer DQ3 bits. Any read attempt during Program or Erase command execution will automatically output these five Status Register bits. The P/E.C. automatically sets bits DQ2, DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1 and DQ4) are reserved for future use and should be masked. See Tables 9 and 10.

Data Polling Bit (DQ7). When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. During Erase operation, it outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid and only effective during P/E.C. operation,

Table 9. Status Register Bits

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete or erase block in Erase Suspend	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase On-going	
		DQ	Program Complete or data of non erase block during Erase Suspend	
		$\overline{DQ}$	Program On-going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program On-going	Successive reads output complementary data on DQ6 while Programming or Erase operations are on-going. DQ6 remains at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		DQ	Program Complete	
		'-1-1-1-1-1-1-1-'	Erase Complete or Erase Suspend on currently addressed block	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' in the case of Programming or Erase failure.
		'0'	Program or Erase On-going	
4	Reserved			
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES).
		'0'	Erase Timeout Period On-going	An additional block to be erased in parallel can be entered to the P/E.C.
2	Toggle Bit	'-1-0-1-0-1-0-1-'	Chip Erase, Erase or Erase Suspend on the currently addressed block. Erase Error due to the currently addressed block (when DQ5 = '1').	Indicates the erase status and allows to identify the erased block
		1	Program on-going, Erase on-going on another block or Erase Complete	
		DQ	Erase Suspend read on non Erase Suspend block	
1	Reserved			
0	Reserved			

Notes: Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.

that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for erase. It must be performed at the address being programmed or at an address within the block being erased. If all the blocks selected for erasure are protected, DQ7 will be set to '0' for about 100µs, and then return to the previous addressed memory data value. See Figure 11 for the Data Polling flowchart and Figure 10 for the Data Polling waveforms. DQ7 will also flag the Erase Suspend mode by switching from '0' to '1' at the start of the Erase Suspend. In order to monitor DQ7 in the Erase Suspend mode an address within a block being erased must be provided. For a Read Operation in Erase Suspend mode, DQ7 will output '1' if the read is attempted on a block being erased and the data value on other blocks. During Program operation in Erase Suspend Mode, DQ7 will have the same behaviour as in the normal program execution outside of the suspend mode.

Table 10. Polling and Toggle Bits

Mode	DQ7	DQ6	DQ2
Program	$\overline{DQ7}$	Toggle	1
Erase	0	Toggle	Note 1
Erase Suspend Read (in Erase Suspend block)	1	1	Toggle
Erase Suspend Read (outside Erase Suspend block)	DQ7	DQ6	DQ2
Erase Suspend Program	$\overline{DQ7}$	Toggle	N/A

Note: 1. Toggle if the address is within a block being erased. '1' if the address is within a block not being erased.

Toggle Bit (DQ6). When Programming or Erasing operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following toggling of either $\overline{G}$, or $\overline{E}$ when $\overline{G}$ is low. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit DQ6 is valid only during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. If the blocks selected for erasure are protected, DQ6 will toggle for about 100µs and then return back to Read. DQ6 will be set to '1' if a Read operation is attempted on an Erase Suspend block. When erase is suspended DQ6 will toggle during programming operations in a block different to the block in Erase Suspend. Either $\overline{E}$ or $\overline{G}$ toggling will cause DQ6 to toggle. See Figure 12 for Toggle Bit flowchart and Figure 13 for Toggle Bit waveforms.

Toggle Bit (DQ2). This toggle bit, together with DQ6, can be used to determine the device status during the Erase operations. It can also be used to identify the block being erased. During Erase or Erase Suspend a read from a block being erased will cause DQ2 to toggle. A read from a block not being erased will set DQ2 to '1' during erase and to DQ2 during Erase Suspend. During Chip Erase a read operation will cause DQ2 to toggle as all blocks are being erased. DQ2 will be set to '1' during program operation and when erase is complete. After erase completion and if the error bit DQ5 is set to '1', DQ2 will toggle if the faulty block is addressed.

Error Bit (DQ5). This bit is set to '1' by the P/E.C. when there is a failure of programming, block erase, or chip erase that results in invalid data in the memory block. In case of an error in block erase or program, the block in which the error occured or to which the programmed data belongs, must be discarded. The DQ5 failure condition will also appear if a user tries to program a '1' to a location that is previously programmed to '0'. Other Blocks may still be used. The error bit resets after a Read/Reset (RD) instruction. In case of success of Program or Erase, the error bit will be set to '0' .

Erase Timer Bit (DQ3). This bit is set to '0' by the P/E.C. when the last block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the erase timeout period is finished, after 50µs to 90µs, DQ3 returns to '1'.

Coded Cycles

The two Coded cycles unlock the Command Interface. They are followed by an input command or a confirmation command. The Coded cycles consist of writing the data AAh at address AAAAh in the Byte-wide configuration and at address 5555h in the Word-wide configuration during the first cycle. During the second cycle the Coded cycles consist of writing the data 55h at address 5555h in the Byte-wide configuration and at address 2AAAh in the Word-wide configuration. In the Byte-wide configuration the address lines A–1 to A14 are valid, in Word-wide A0 to A14 are valid, other address lines are 'don't care'. The Coded cycles happen on first and second cycles of the command write or on the fourth and fifth cycles.

Instructions

See Table 8.

Read/Reset (RD) Instruction. The Read/Reset instruction consists of one write cycle giving the command F0h. It can be optionally preceded by the two Coded cycles. Subsequent read operations will read the memory array addressed and output the data read. A wait state of 10µs is necessary after Read/Reset prior to any valid read if the memory was in an Erase mode when the RD instruction is given.

Auto Select (AS) Instruction. This instruction uses the two Coded cycles followed by one write cycle giving the command 90h to address AAAAh in the Byte-wide configuration or address 5555h in the Word-wide configuration for command set-up. A subsequent read will output the manufacturer code and the device code or the block protection status depending on the levels of A0 and A1. The manufacturer code, 20h, is output when the addresses lines A0 and A1 are Low, the device code, EEh for Top Boot, EFh for Bottom Boot is output when A0 is High with A1 Low.

The AS instruction also allows access to the block protection status. After giving the AS instruction, A0 is set to V_{IL} with A1 at V_{IH}, while A12-A17 define the address of the block to be verified. A read in these conditions will output a 01h if the block is protected and a 00h if the block is not protected.

Table 11. AC Measurement Conditions

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Figure 4. AC Testing Input Output Waveform

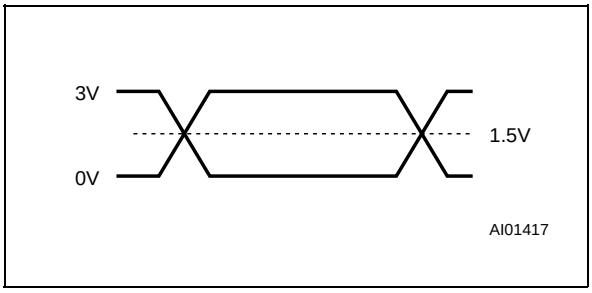


Figure 5. AC Testing Load Circuit

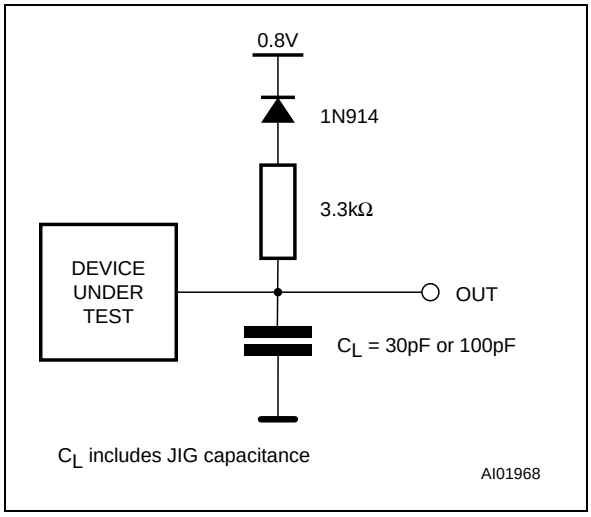


Table 12. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 13. DC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC1}	Supply Current (Read) Byte	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f = 6MHz		10	mA
I_{CC1}	Supply Current (Read) Word	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f = 6MHz		10	mA
I_{CC3}	Supply Current (Standby)	$\overline{E}$ = V_{CC} ± 0.2V		50	µA
I_{CC4} (1)	Supply Current (Program or Erase)	Byte program, Block or Chip Erase in progress		20	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4V		V
V_{ID}	A9 Voltage (Electronic Signature)		11.0	12.0	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		100	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2.0	2.3	V

Note: 1. Sampled only, not 100% tested.

Table 14A. Read AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	Test Condition	M29W400T / M29W400B				Unit
				-90		-100		
				V_{CC} = 3.0V to 3.6V C_L = 30pF		V_{CC} = 2.7V to 3.6V C_L = 30pF		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	90		100		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		100	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		100	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		30	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns
t_{PLYH} (1,3)	t_{RRB} t_{READY}	$\overline{RP}$ Low to Read Mode			10		10	µs
t_{PHEL}	t_{RH}	$\overline{RP}$ High to Chip Enable Low		50		50		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width		500		500		ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to $\overline{BYTE}$ Switching Low or High			5		5	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High Z			50		50	ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ Switching High to Output Valid			50		50	ns

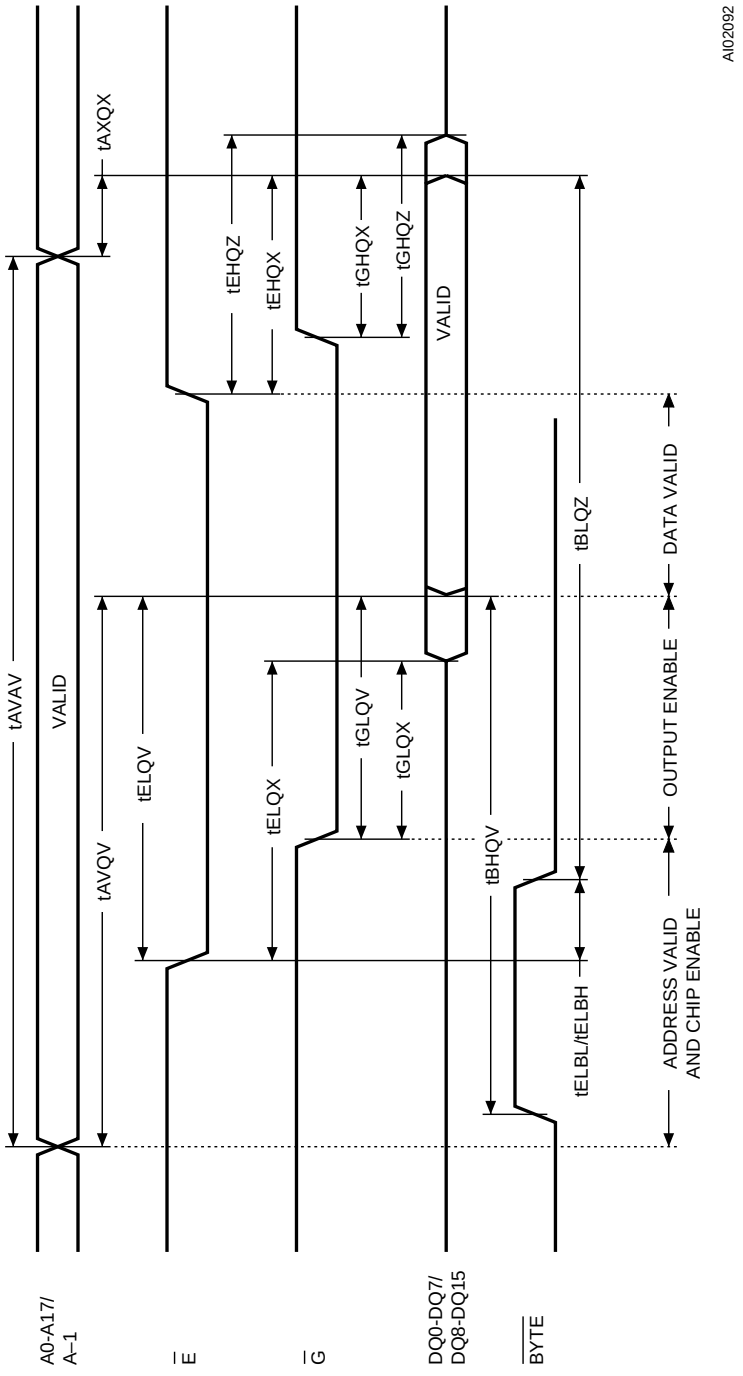
Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.
3. To be considered only if the Reset pulse is given while the memory is in Erase or Program mode.

Table 14B. Read AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	Test Condition	M29W400T / M29W400B				Unit
				-120		-150		
				V_{CC} = 2.7V to 3.6V		V_{CC} = 2.7V to 3.6V		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		55	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		40	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns
t_{PLYH} (1,3)	t_{RRB} t_{READY}	$\overline{RP}$ Low to Read Mode			10		10	µs
t_{PHEL}	t_{RH}	$\overline{RP}$ High to Chip Enable Low		50		50		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width		500		500		ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to $\overline{BYTE}$ Switching Low or High			5		5	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High Z			60		60	ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ Switching High to Output Valid			60		60	ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.
3. To be considered only if the Reset pulse is given while the memory is in Erase or Program mode.

Figure 6. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High.

Table 15A. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	M29W400T / M29W400B				Unit
			-90		-100		
			V_{CC} = 3.0V to 3.6V C_L = 30pF		V_{CC} = 2.7V to 3.6V C_L = 30pF		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	90		100		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	45		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	45		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{PHPHH} (1,2)	t_{VIDR}	$\overline{RP}$ Rise Time to V_{ID}	500		500		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{WHRL} (1)	t_{BUSY}	Program Erase Valid to $R\overline{B}$ Delay		90		90	ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs

Notes: 1. Sample only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Program (PG) Instruction. This instruction uses four write cycles. Both for Byte-wide configuration and for Word-wide configuration. The Program command A0h is written to address AAAAh in the Byte-wide configuration or to address 5555h in the Word-wide configuration on the third cycle after two Coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{W}$ or $\overline{E}$ and the Data to be written on the rising edge and starts the P/E.C. Read operations output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. Status bits DQ6 and DQ7 determine if programming is on-going and DQ5 allows verification of any possible error. Programming at an address not in blocks being erased is also possible during erase suspend. In this case, DQ2 will toggle at the address being programmed.

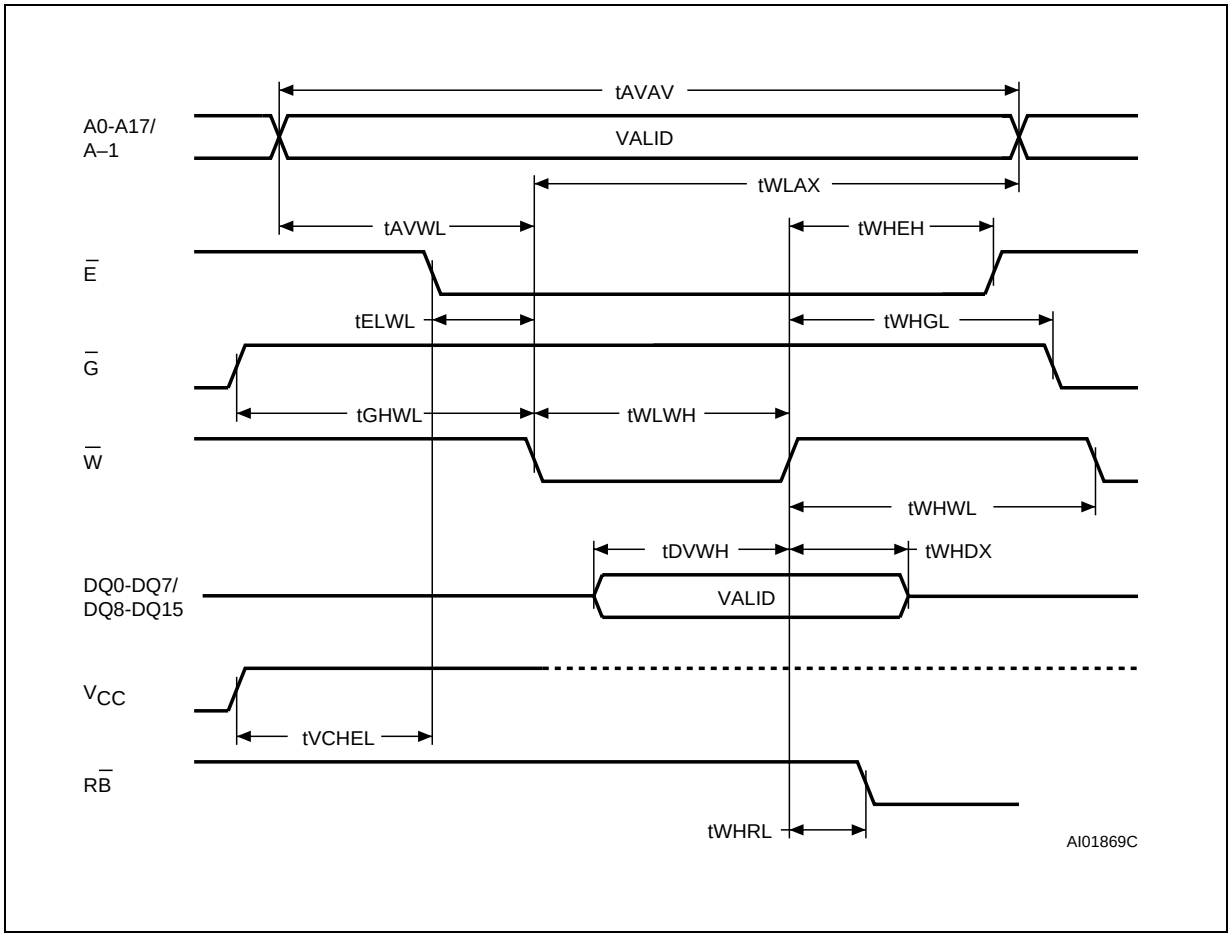
Table 15B. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	M29W400T / M29W400B				Unit
			-120		-150		
			V_{CC} = 2.7V to 3.6V		V_{CC} = 2.7V to 3.6V		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		65		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		65		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		35		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		65		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{PHPHH} (1,2)	t_{VIDR}	$\overline{RP}$ Rise Time to V_{ID}	500		500		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{WHRL} (1)	t_{BUSY}	Program Erase Valid to $R\overline{B}$ Delay		90		90	ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs

Notes: 1. Sample only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Block Erase (BE) Instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address AAAAh in the Byte-wide configuration or address 5555h in the Word-wide configuration on third cycle after the two Coded cycles. The Block Erase Confirm command 30h is similarly written on the sixth cycle after another two Coded cycles. During the input of the second command an address within the block to be erased is given and latched into the memory. Additional block Erase Confirm commands and block addresses can be written subsequently to erase other blocks in parallel, without further Coded cycles. The erase will start after the erase timeout period (see Erase Timer Bit DQ3 description). Thus, additional Erase Confirm commands for other blocks must be given within this delay. The input of a new Erase Confirm command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Block Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the P/E.C. is erasing the Block(s). If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the block with 00h as the P/E.C. will do this automatically before to erasing to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register status bits.

Figure 7. Write AC Waveforms, $\overline{W}$ Controlled



Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.

During the execution of the erase by the P/E.C., the memory accepts only the Erase Suspend ES and Read/Reset RD instructions. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle bit DQ2 and DQ6 toggle during the erase operation. They stop when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an erase failure. In such a situation, the Toggle bit DQ2 can be used to determine which block is not correctly erased. In the case of erase failure, a Read/Reset RD instruction is necessary in order to reset the P/E.C.

Chip Erase (CE) Instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written to address AAAAh in the Byte-wide configuration or the address 5555h in the Word-wide configuration on the third cycle after the two Coded cycles. The Chip Erase Confirm command 10h is similarly written on the sixth cycle after another two Coded cycles. If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing it to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the Status Register bits. During the execution of the erase by the P/E.C., Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle bits DQ2 and DQ6 toggle during erase operation and stop when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure.

Table 16A. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	M29W400T / M29W400B				Unit
			-90		-100		
			V_{CC} = 3.0V to 3.6V C_L = 30pF		V_{CC} = 2.7V to 3.6V C_L = 30pF		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	90		100		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	45		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	45		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		30		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	45		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		µs
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns
t_{PHPHH} (1,2)	t_{VIDR}	$\overline{RP}$ Rise TIme to V_{ID}	500		500		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{EHRL} (1)	t_{BUSY}	Program Erase Valid to $R\overline{B}$ Delay		90		90	ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs

Notes: 1. Sample only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Erase Suspend (ES) Instruction. The Block Erase operation may be suspended by this instruction which consists of writing the command B0h without any specific address. No Coded cycles are required. It permits reading of data from another block and programming in another block while an erase operation is in progress. Erase suspend is accepted only during the Block Erase instruction execution. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the timeout. The Toggle bit DQ6 stops toggling when the P/E.C. is suspended. The Toggle bits will stop toggling between 0.1µs and 15µs after the Erase Suspend (ES) command has been written. The device will then automatically be set to Read Memory Array mode. When erase is suspended, a Read from blocks being erased will output DQ2 toggling and DQ6 at '1'. A Read from a block not being erased returns valid data. During suspension the memory will respond only to the Erase Resume ER and the Program PG instructions. A Program operation can be initiated during erase suspend in one of the blocks not being erased. It will result in both DQ2 and DQ6 toggling when the data is being programmed. A Read/Reset command will definitively abort erasure and result in invalid data in the blocks being erased.

Table 16B. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Symbol	Alt	Parameter	M29W400T / M29W400B				Unit
			-120		-150		
			V_{CC} = 2.7V to 3.6V		V_{CC} = 2.7V to 3.6V		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		35		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	50		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		µs
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns
t_{PHPHH} (1,2)	t_{VIDR}	$\overline{RP}$ Rise TIme to V_{ID}	500		500		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	500		500		ns
t_{EHRL} (1)	t_{BUSY}	Program Erase Valid to R$\overline{B}$ Delay		90		90	ns
t_{PHWL} (1)	t_{RSP}	$\overline{RP}$ High to Write Enable Low	4		4		µs

Notes: 1. Sample only, not 100% tested.
2. This timing is for Temporary Block Unprotection operation.

Erase Resume (ER) Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any Coded cycles.

POWER SUPPLY

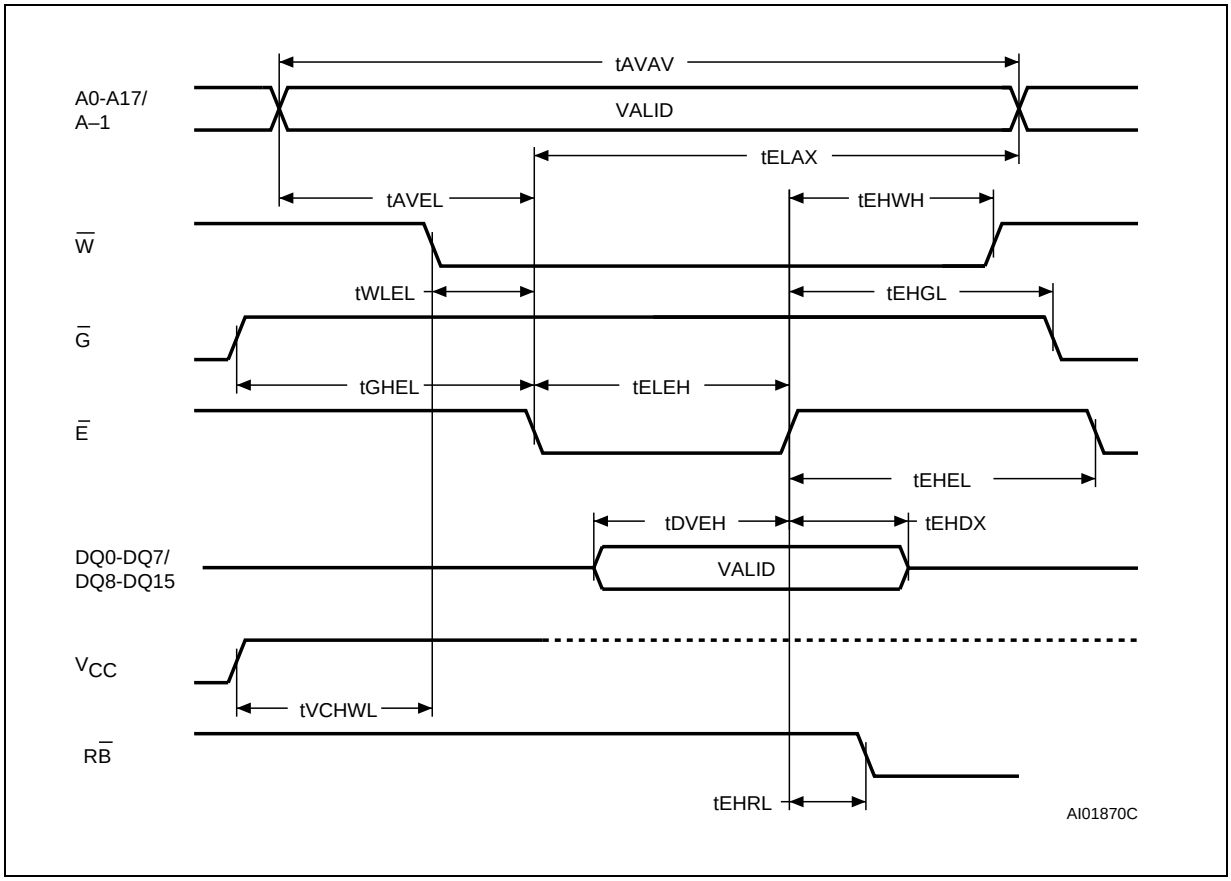
Power Up

The memory Command Interface is reset on power up to Read Array. Either $\overline{E}$ or $\overline{W}$ must be tied to V_{IH} during Power Up to allow maximum security and the possibility to write a command on the first rising edge of $\overline{E}$ and $\overline{W}$. Any write cycle initiation is blocked when Vcc is below V_{LKO}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling; each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{CC} program and erase currents required.

Figure 8. Write AC Waveforms, $\overline{E}$ Controlled



Note: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.

Figure 9. Read and Write AC Characteristics, $\overline{RP}$ Related

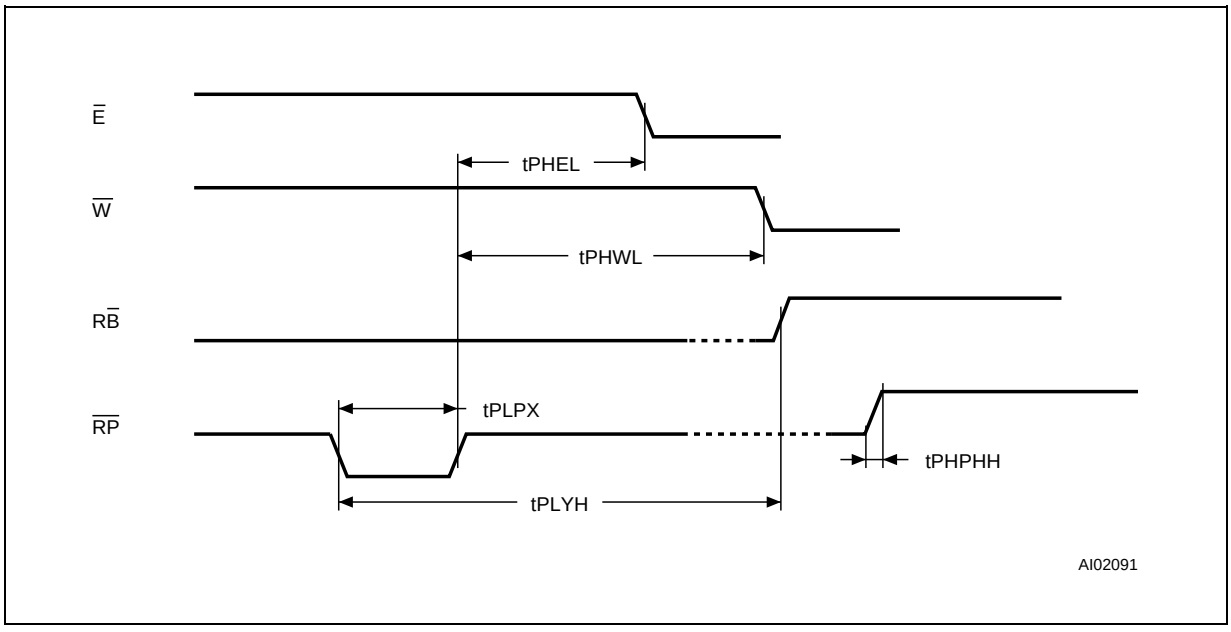


Table 17A. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Sym-bol	Parameter	M29W400T / M29W400B				Unit
		-90		-100		
		V_{CC} = 3.0V to 3.6V C_L = 30pF		V_{CC} = 2.7V to 3.6V C_L = 30pF		
		Min	Max	Min	Max	
t_{WHQ7V}	Write Enable High to DQ7 Valid (Program, W Controlled)	10	2400	10	2400	ms
	Write Enable High to DQ7 Valid (Chip Erase, W Controlled)	1.0	30	1.0	30	sec
t_{EHQ7V}	Chip Enable High to DQ7 Valid (Program, E Controlled)	10	2400	10	2400	µs
	Chip Enable High to DQ7 Valid (Chip Erase, E Controlled)	1.0	30	1.0	30	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		35		40	ns
t_{WHQV}	Write Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Write Enable High to Output Valid (Chip Erase)	1.0	30	1.0	30	sec
t_{EHQV}	Chip Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Chip Enable High to Output Valid (Chip Erase)	1.0	30	1.0	30	sec

Note: 1. All other timings are defined in Read AC Characteristics table.

Table 17B. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C)

Sym-bol	Parameter	M29W400T / M29W400B				Unit
		-120		-150		
		V_{CC} = 2.7V to 3.6V		V_{CC} = 2.7V to 3.6V		
		Min	Max	Min	Max	
t_{WHQ7V}	Write Enable High to DQ7 Valid (Program, W Controlled)	10	2400	10	2400	ms
	Write Enable High to DQ7 Valid (Chip Erase, W Controlled)	1.0	30	1.0	30	sec
t_{EHQ7V}	Chip Enable High to DQ7 Valid (Program, E Controlled)	10	2400	10	2400	µs
	Chip Enable High to DQ7 Valid (Chip Erase, E Controlled)	1.0	30	1.0	30	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		50		55	ns
t_{WHQV}	Write Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Write Enable High to Output Valid (Chip Erase)	1.0	30	1.0	30	sec
t_{EHQV}	Chip Enable High to Output Valid (Program)	10	2400	10	2400	µs
	Chip Enable High to Output Valid (Chip Erase)	1.0	30	1.0	30	sec

Note: 1. All other timings are defined in Read AC Characteristics table.

Figure 10. Data Polling DQ7 AC Waveforms

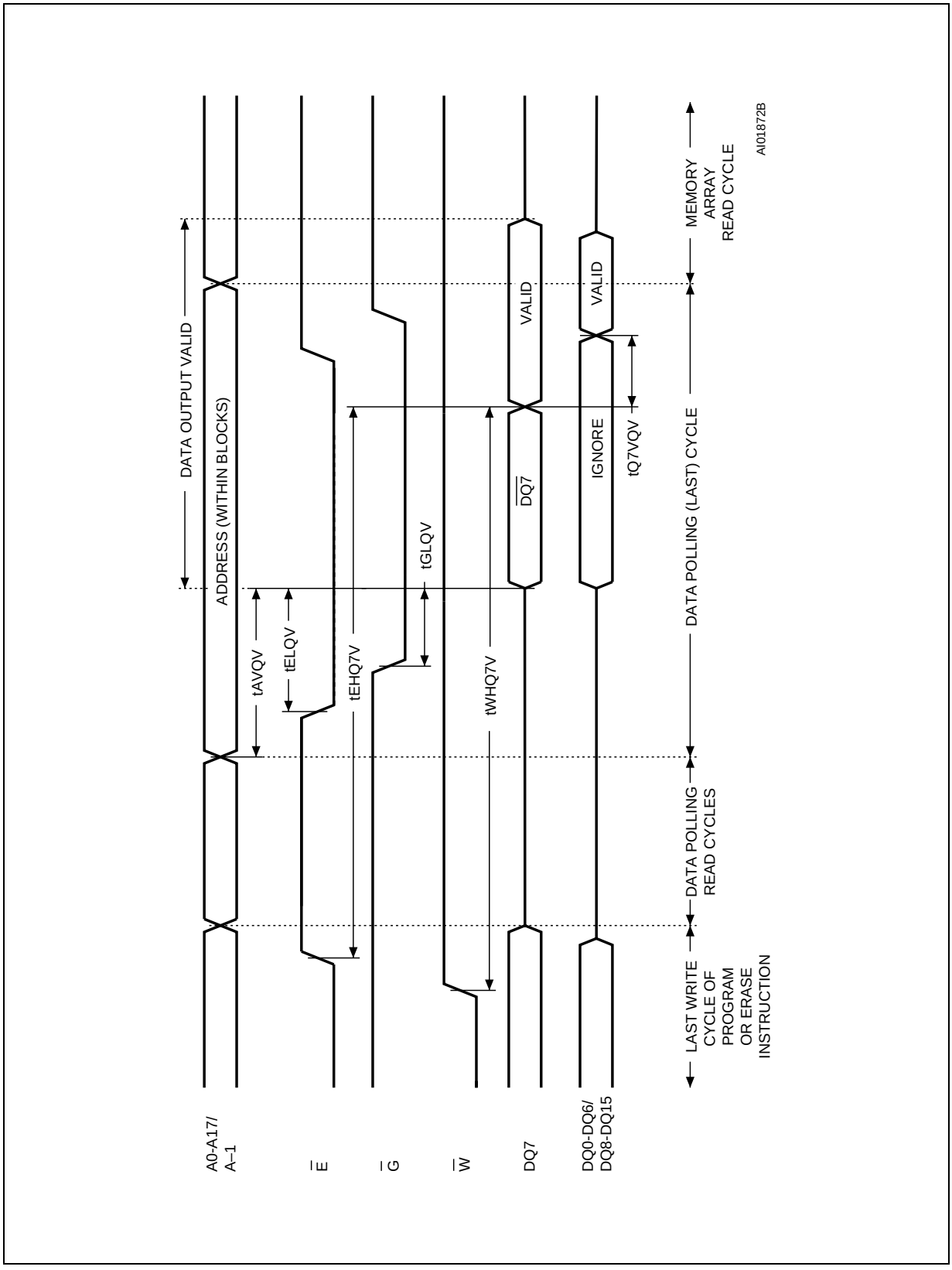


Figure 11. Data Polling Flowchart

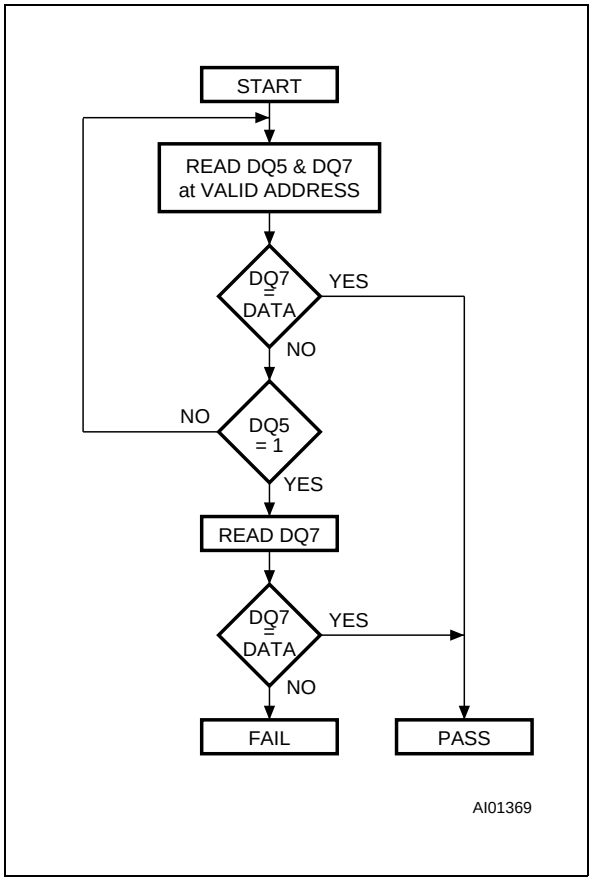


Figure 12. Data Toggle Flowchart

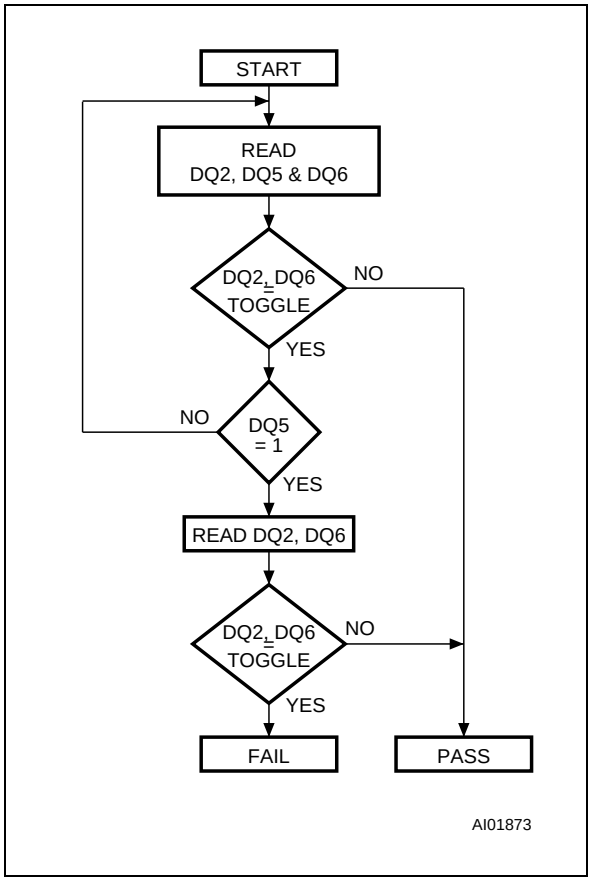
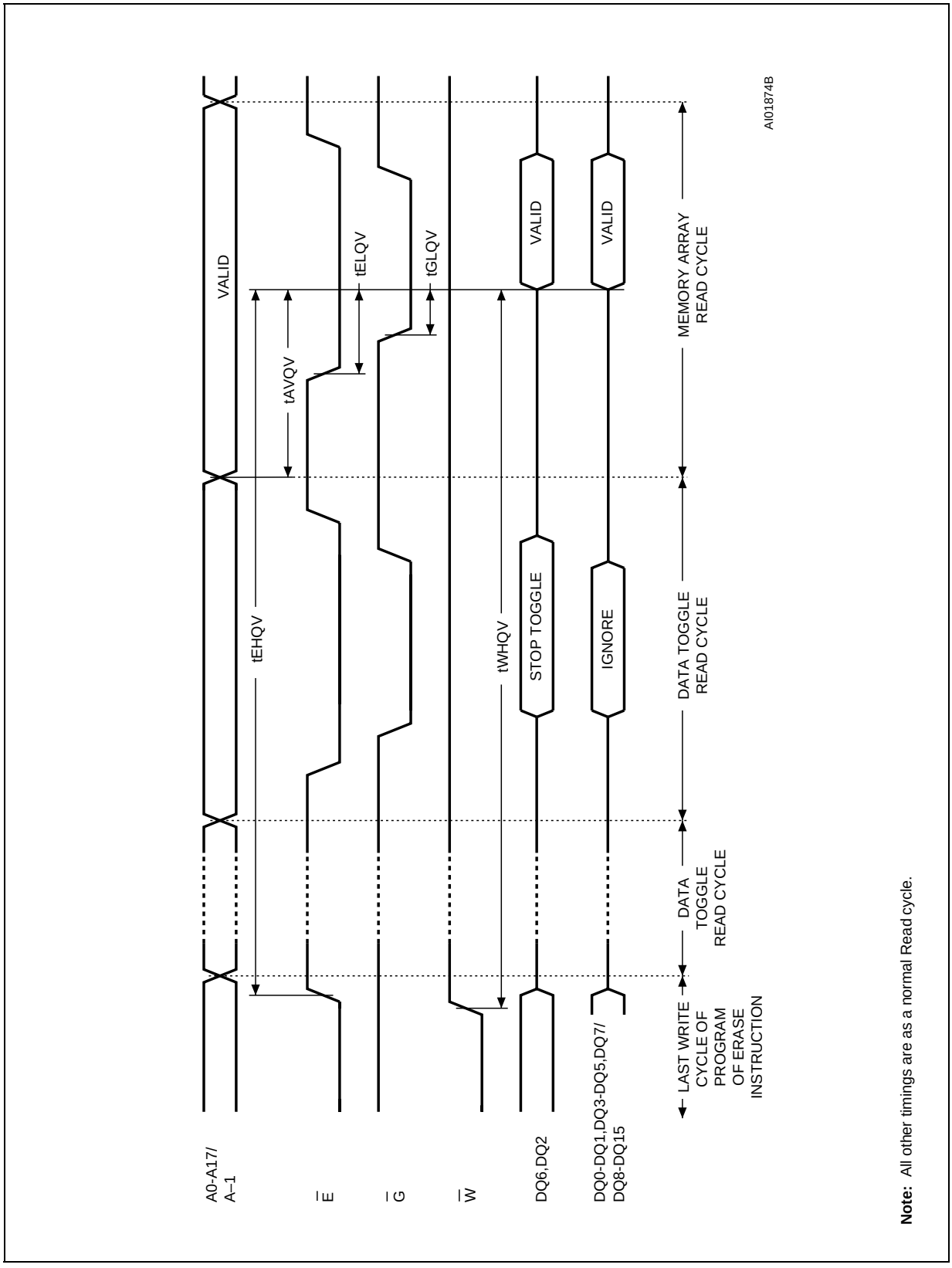


Table 18. Program, Erase Times and Program, Erase Endurance Cycles
(T_A = 0 to 70°C; V_{CC} = 2.7V to 3.6V)

Parameter	M29W400T / M29W400B			Unit
	Min	Typ	Typical after 100k W/E Cycles	
Chip Erase (Preprogrammed)		1.5	1.7	sec
Chip Erase		6.7	7.0	sec
Boot Block Erase		0.7		sec
Parameter Block Erase		0.6		sec
Main Block (32Kb) Erase		0.9		sec
Main Block (64Kb) Erase		1.4		sec
Chip Program (Byte)		7.5	7.5	sec
Byte Program		10	10	µs
Word Program		16	16	µs
Program/Erase Cycles (per Block)	100,000			cycles

Figure 13. Data Toggle DQ6, DQ2 AC Waveforms



Note: All other timings are as a normal Read cycle.

Figure 14. Block Protection Flowchart

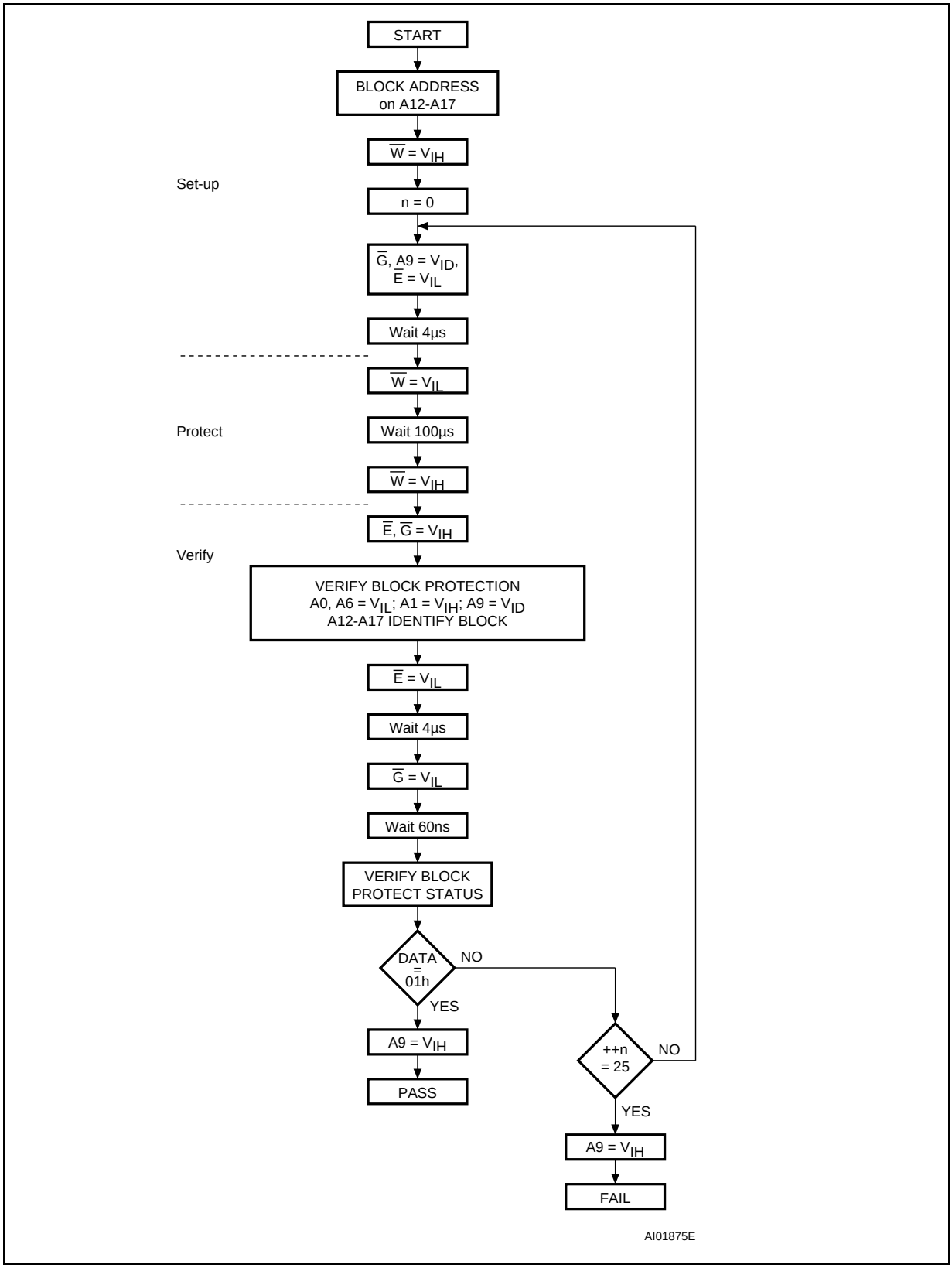
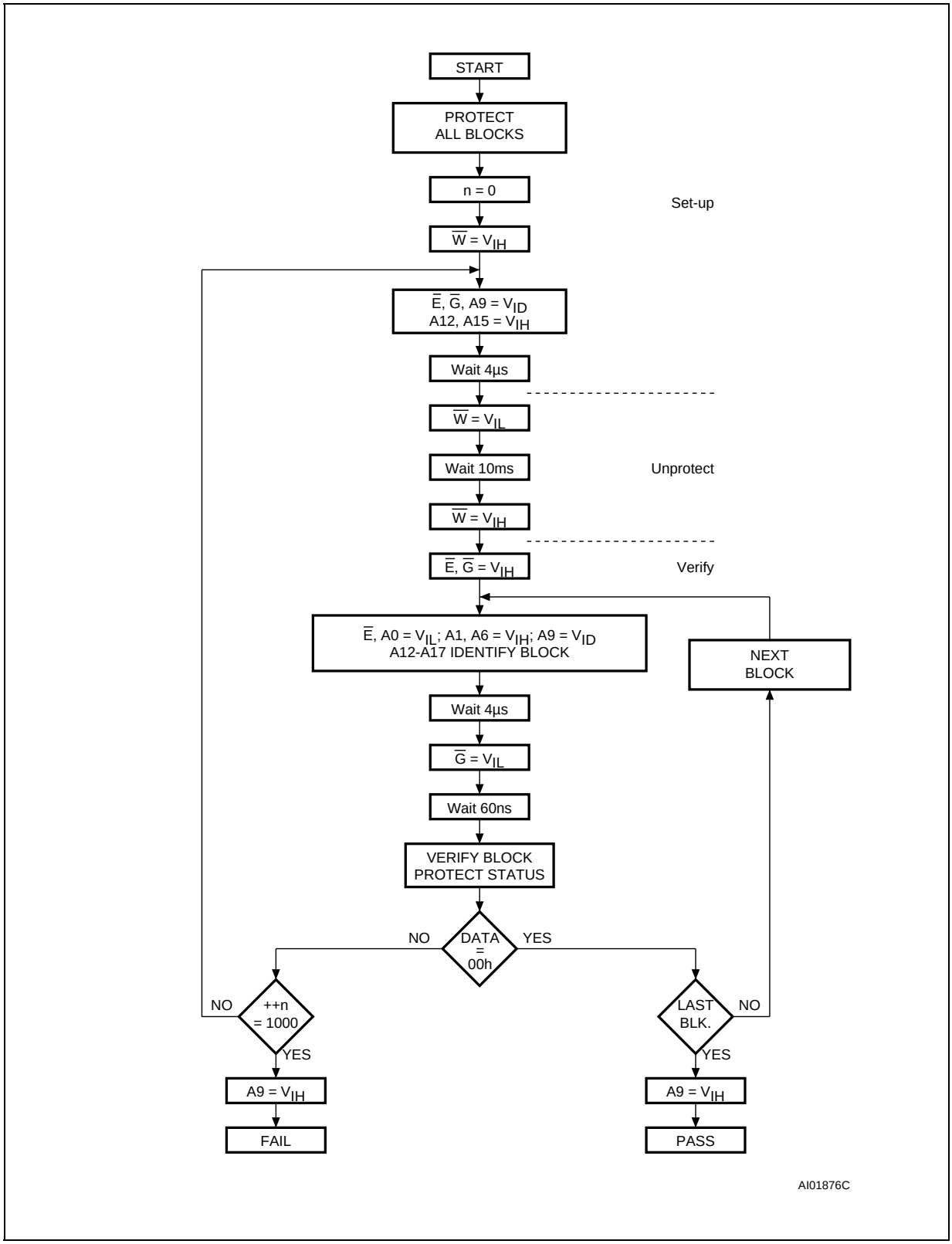
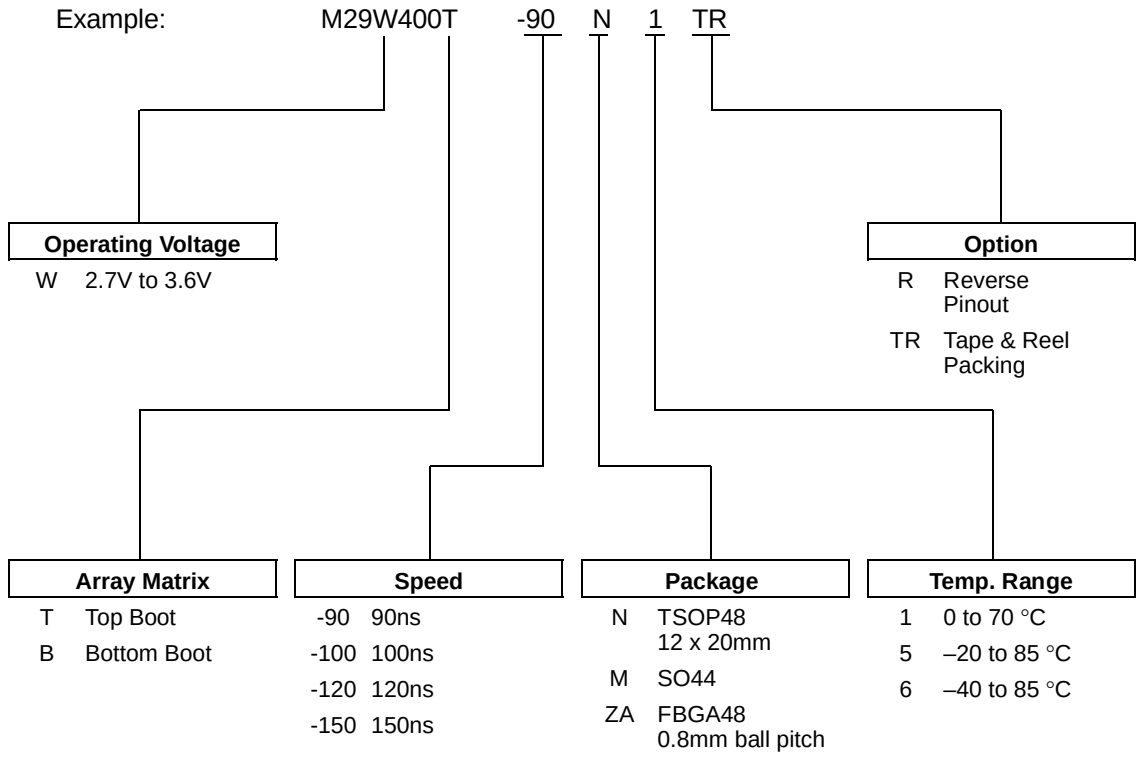


Figure 15. All Blocks Unprotecting Flowchart



ORDERING INFORMATION SCHEME



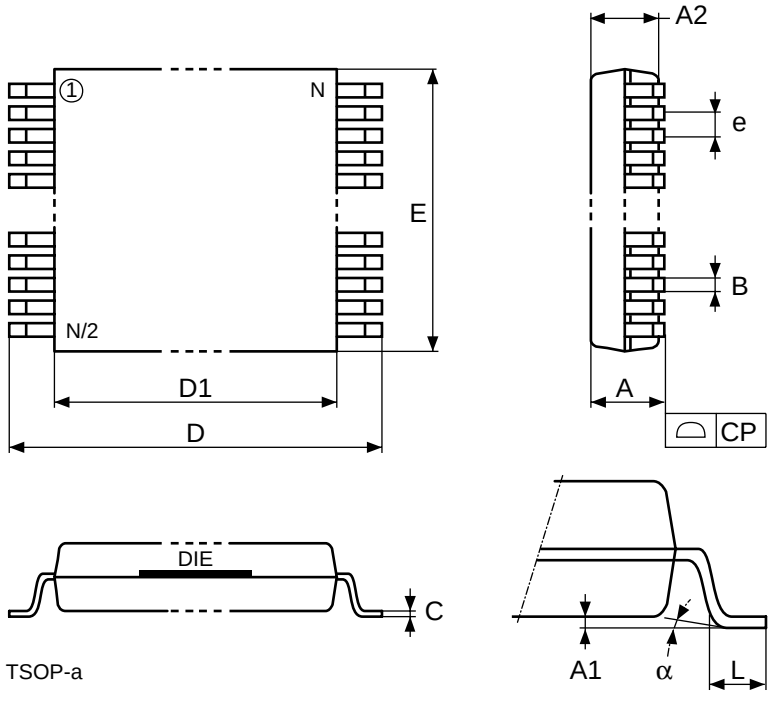
M29W400T and M29W400B are replaced respectively by the new version M29W400BT and M29W400BB

Devices are shipped from the factory with the memory content erased (to FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

TSOP48 Normal Pinout - 48 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		11.90	12.10		0.469	0.476
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.004

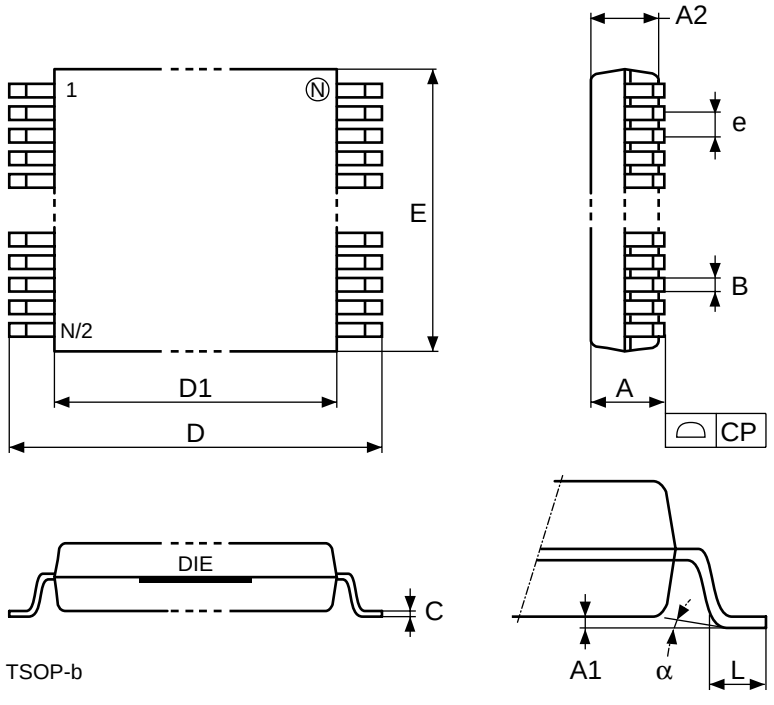


TSOP-a

Drawing is not to scale.

TSOP48 Reverse Pinout - 48 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		11.90	12.10		0.469	0.476
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.004

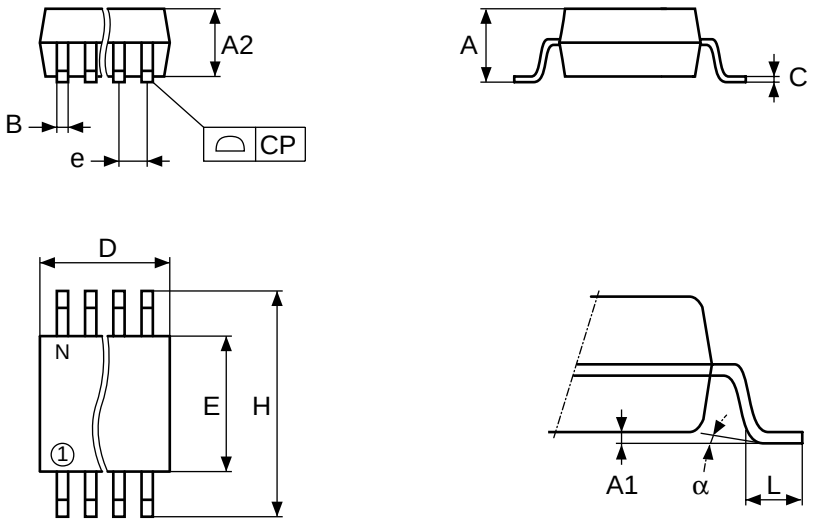


TSOP-b

Drawing is not to scale.

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27			0.050		
H		15.90	16.10		0.626	0.634
L	0.80			0.031		
α	3°			3°		
N	44			44		
CP			0.10			0.004

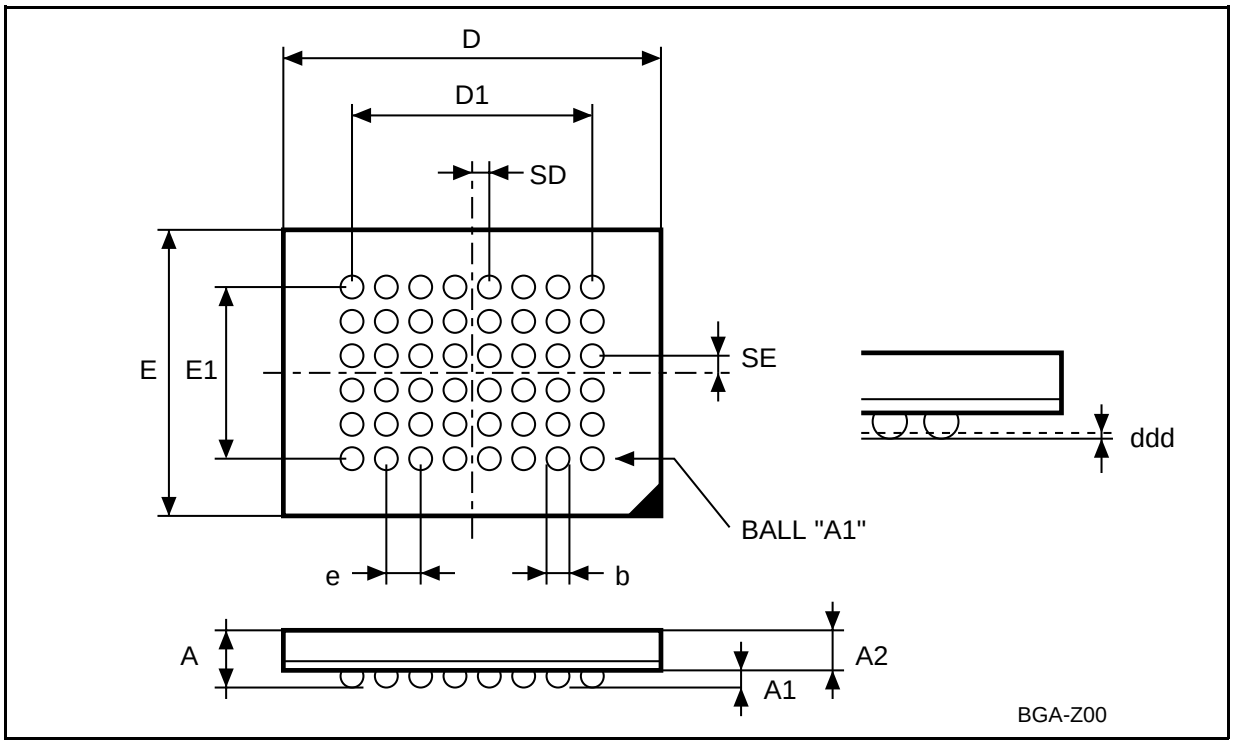


SO-b

Drawing is not to scale.

FBGA48 - 48 balls (8 x 6) Fine Pitch Ball Grid Array, 0.80mm pitch

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	1.250	1.150	1.350	0.049	0.045	0.053
A1	0.300	0.250	0.350	0.012	0.010	0.014
A2	0.950	–	–	0.037	–	–
b	0.400	0.350	0.450	0.016	0.014	0.018
ddd			0.150			0.006
D	9.000	8.800	9.200	0.354	0.346	0.362
D1	5.600	–	–	0.220	–	–
e	0.800	–	–	0.031	–	–
E	6.000	5.800	6.200	0.236	0.228	0.244
E1	4.000	–	–	0.157	–	–
SD	0.400	–	–	0.016	–	–
SE	0.400	–	–	0.016	–	–



Drawing is not to scale.