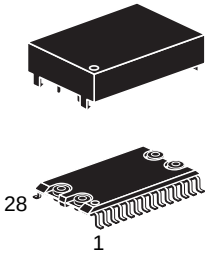
# M48T559Y

## 5.0V, 64 Kbit (8 Kbit x 8) TIMEKEEPER® SRAM WITH ADDRESS/ADDRESS/DATA MULTIPLEXED

### FEATURES SUMMARY

- SOFTWARE and HARDWARE RESET FOR WATCHDOG TIMER
- REGISTER COMPATIBLE WITH M48T59 TIMEKEEPER SRAM
- ADDRESS/ADDRESS/DATA MULTIPLEXED
- I/O PINS
- WATCHDOG TIMER - MONITORS OUT-OF-CONTROL PROCESSOR OR “HUNG” BUS
- ALARM WITH WAKE-UP IN BATTERY MODE
- INTEGRATED, ULTRA-LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- FREQUENCY TEST OUTPUT FOR REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- POWER-FAIL DESELECT VOLTAGE ($V_{PFD}$ = Power-fail Deselect Voltage):
  - M48T559Y: $V_{CC}$ = 4.5 to 5.5V; $4.2 \leq V_{PFD} \leq 4.5V$
- PACKAGING INCLUDES A 28-LEAD SOIC and SNAPHAT® TOP (to be Ordered Separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT TOP CONTAINS THE BATTERY and CRYSTAL
- MICROPROCESSOR POWER-ON RESET
- (Valid even during battery back-up mode)
- PROGRAMMABLE ALARM OUTPUT ACTIVE IN THE BATTERY BACK-UP MODE

**Figure 1. 28-pin SOIC Package**






Rev. 3.0

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## SUMMARY DESCRIPTION

The M48T559Y TIMEKEEPER® RAM is an 8 Kb x 8 non-volatile static RAM and real time clock. The monolithic chip is available in the SNAPHAT® package to provide a highly integrated battery backed-up memory and real time clock solution.

The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4T28-BR12SH” (see Table 17, page 24).

**Caution:** Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

**Figure 2. Logic Diagram**

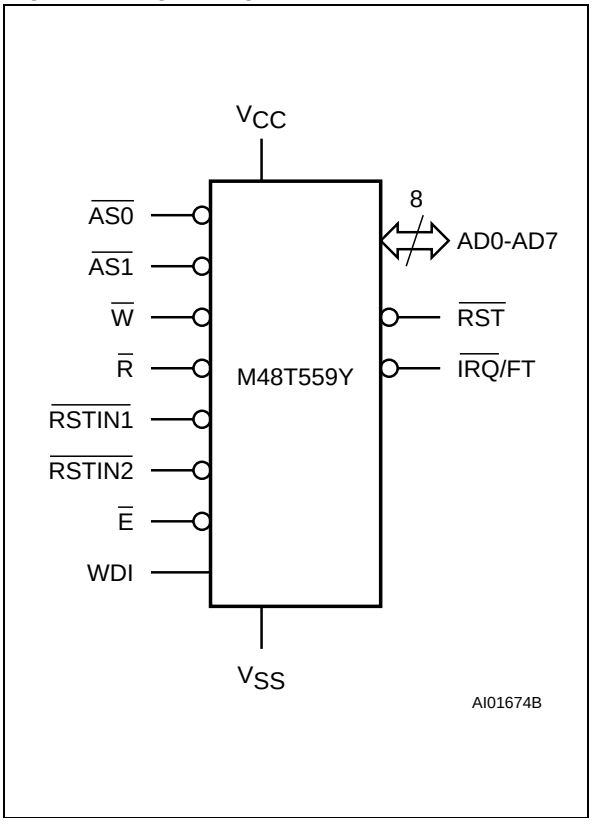



**Table 1. Signal Names**

| | |
|---|---|
| AD0 - AD7 | Address/Address/Data |
| $\overline{AS0}$ - $\overline{AS1}$ | Address Strobes |
| $\overline{W}$ | WRITE Enable |
| $\overline{R}$ | READ Enable |
| $\overline{E}$ | Chip Enable |
| WDI | Watchdog Input |
| $\overline{RST}$ | Reset Output (Open Drain) |
| $\overline{RSTIN1}$ | Reset 1 Input |
| $\overline{RSTIN2}$ | Reset 2 Input |
| $\overline{IRQ}$/FT | Interrupt/Frequency Test Output (Open Drain) |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |
| NC | Not Connected Internally |
| DU | Don’t Use; must be connected to $V_{CC}$ or $V_{SS}$ |

**Figure 3. SOIC Connections**

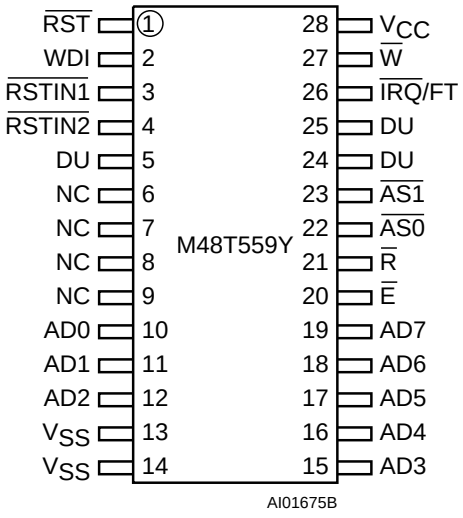
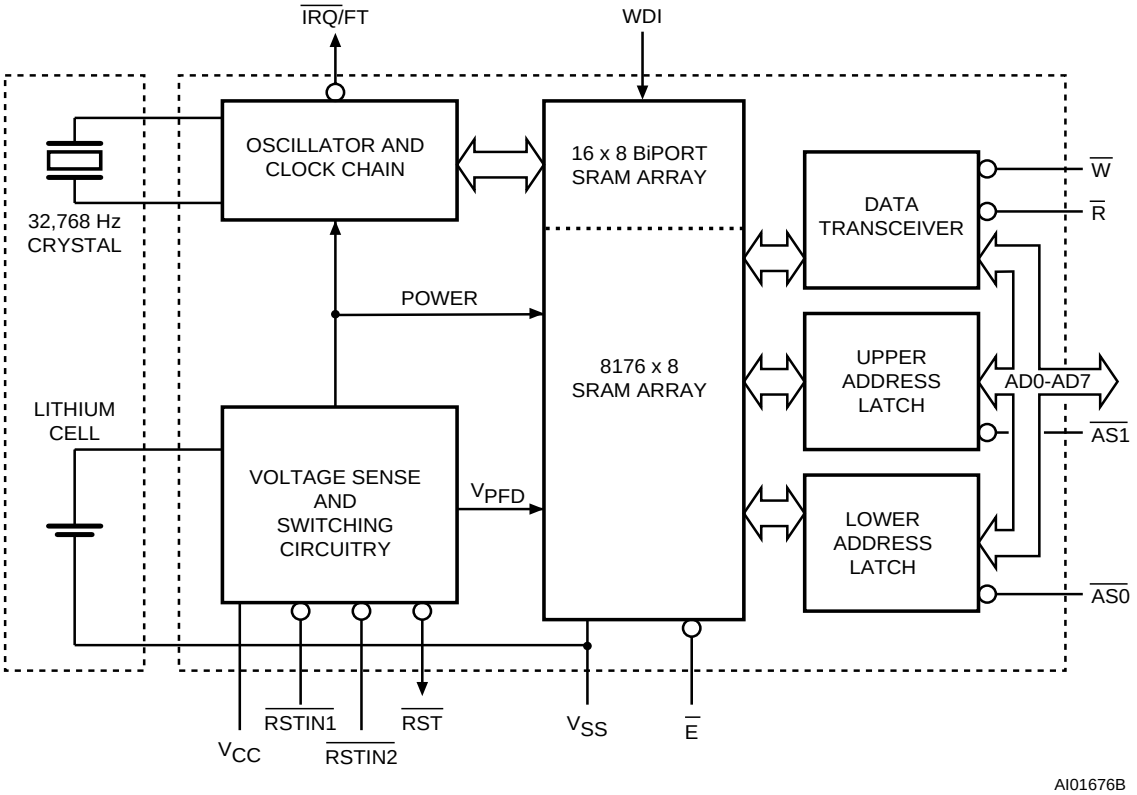



**Figure 4. Block Diagram**



## MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute Maximum Ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | | 0 to 70 | °C |
| $T_{STG}$ | Storage Temperature ($V_{CC}$ Off, Oscillator Off) | SNAPHAT® | –40 to 85 | °C |
| | | SOIC | 0 to 70 | °C |
| $T_{SLD}$(1) | Lead Solder Temperature for 10 seconds | | 260 | °C |
| $V_{IO}$ | Input or Output Voltage | | –0.3 to 7 | V |
| $V_{CC}$ | Supply Voltage | | –0.3 to 7 | V |
| $I_O$ | Output Current | | 20 | mA |
| $P_D$ | Power Dissipation | | 1 | W |

Note: 1. Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 to 120 seconds).

***CAUTION:*** *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

***CAUTION:*** *Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.*

## DC AND AC PARAMETERS

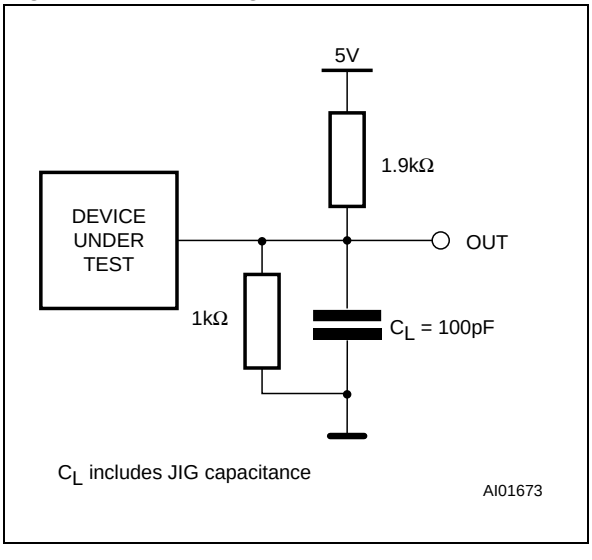
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

### Table 3. DC and AC Measurement Conditions

| Parameter | M48T559Y |
|---|---|
| $V_{CC}$ Supply Voltage | 4.5 to 5.5V |
| Ambient Operating Temperature | 0 to 70°C |
| Load Capacitance ($C_L$) | 100pF |
| Input Rise and Fall Times | ≤ 5ns |
| Input Pulse Voltages | 0 to 3V |
| Input and Output Timing Ref. Voltages | 1.5V |

Note: Output High Z is defined as the point where data is no longer driven.

### Figure 5. AC Testing Load Circuit




### Table 4. Capacitance

| Symbol | Parameter(1,2) | Min | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10 | pF |
| $C_{OUT}$(3) | Output Capacitance | | 10 | pF |

Note: 1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. At 25°C; f = 1MHz.
3. Outputs are deselected.

## Table 5. DC Characteristics

| Sym | Parameter | Test Condition(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | | ±1 | µA |
| $I_{LO}$(2) | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | | ±1 | µA |
| $I_{LRST}$(3) | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | | 100 | µA |
| $I_{CC}$ | Supply Current | Outputs open | | | 50 | mA |
| $I_{CC1}$ | Supply Current (Standby) TTL | $\overline{E} = V_{IH}$ | | | 10 | mA |
| $I_{CC2}$(4) | Supply Current (Standby) CMOS | $\overline{E} = V_{CC} - 0.2V$ | | | 7 | mA |
| $V_{IL}$(5) | Input Low Voltage | | –0.3 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | | $V_{CC} + 0.3$ | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 2.1mA$ | | | 0.4 | V |
| | Output Low Voltage ($\overline{IRQ}$/FT) (6) | $I_{OL} = 10mA$ | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OL} = –1mA$ | 2.4 | | | V |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).
2. Outputs Deselected.
3. Input leakage current on input $\overline{RSTIN1}$ and $\overline{RSTIN2}$ pins.
4. AD0-AD7, $\overline{AS0}$, $\overline{AS1}$ active when $\overline{E}$ is high and $V_{CC} > V_{PFD}$.
5. Negative spikes of –1V allowed for up to 10ns once per cycle.
6. For $\overline{IRQ}$/FT pin (Open Drain).

## OPERATION MODES

As Figure 4, page 5 shows, the static memory array and the quartz controlled clock oscillator of the M48T559Y are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year - valid until 2100), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ READ/WRITE memory cells.

The M48T559Y includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T559Y also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition.

When $V_{CC}$ is out-of-tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low $V_{CC}$. As $V_{CC}$ falls below the Battery Back-up Switchover Voltage ($V_{SO}$), the control circuitry connects the battery which maintains data and clock operation until valid power returns.

**Table 6. Operating Modes**

| Mode | $V_{CC}$ | $\overline{E}$ | $\overline{R}$ | $\overline{W}$ | AD0-AD7(2) | Power |
|---|---|---|---|---|---|---|
| Deselect | 4.5 to 5.5V | $V_{IH}$ | X | X | High Z | Standby |
| WRITE | | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $D_{IN}$ | Active |
| READ | | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | Active |
| READ | | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | High Z | Active |
| Deselect | $V_{SO}$ to $V_{PFD}$ (min)(1) | X | X | X | High Z | CMOS Standby |
| Deselect | $\leq V_{SO}$(1) | X | X | X | High Z | Battery Back-up Mode |

Note: X = $V_{IH}$ or $V_{IL}$; $V_{SO}$ = Battery Back-up Switchover Voltage
1. See Table 9, page 13 for details.
2. AD0-AD7, AS0, AS1 active when $\overline{E}$ is high and $V_{CC} > V_{PFD}$.

## RAM OPERATION

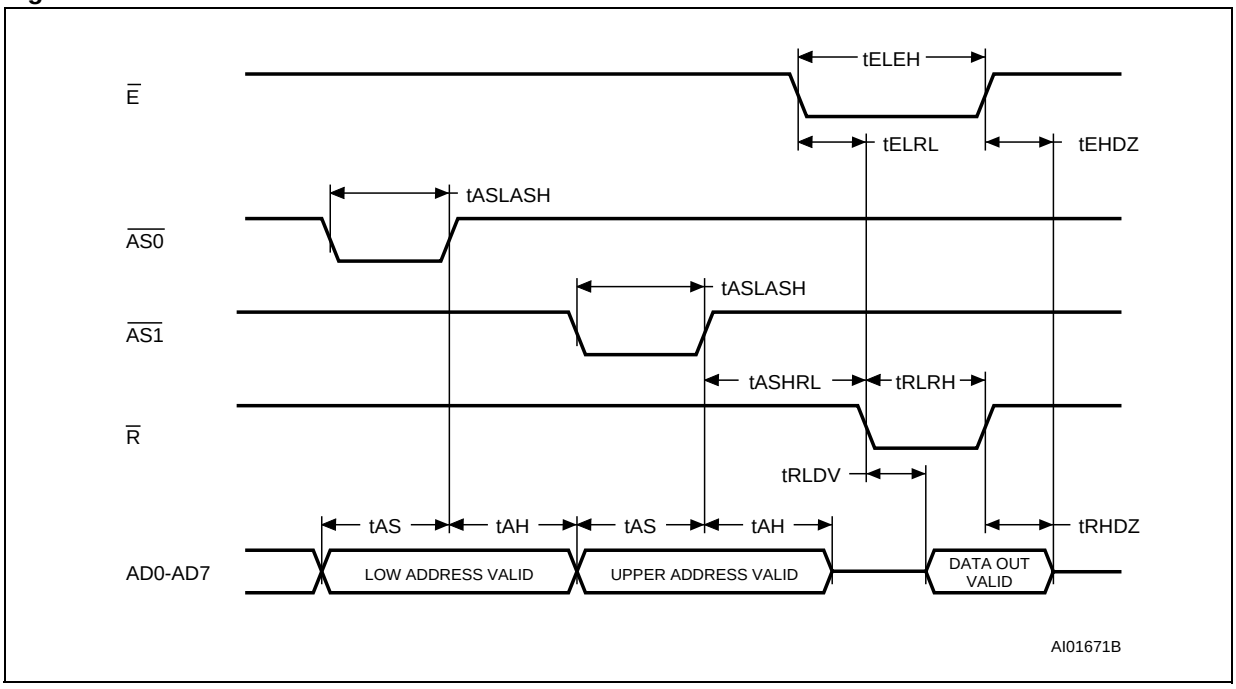
Four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{R}$ and $\overline{W}$, are used to access the M48T559Y. The address latches are loaded from the address/address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 ($\overline{AS1}$) signals. $\overline{AS0}$ is used to latch the lower 8 bits of address, and $\overline{AS1}$ is used to latch the upper 5 bits of address.

It is not however necessary to follow any particular order. The inputs are in parallel for the two address bytes (upper and lower) and can be latched in any order as long as the correct strobe is used. It is necessary to meet the set-up and hold times given in the AC specifications with valid address information in order to properly latch the address. If the upper and/or lower order addresses are correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A WRITE operation requires valid data to be placed on the bus (AD0-AD7), followed by the activation of the WRITE Enable ($\overline{W}$) line. Data on the bus will be written to the RAM, provided that the WRITE timing specifications are met. During a READ cycle, the READ Enable ($\overline{R}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM READ access timing specifications are met.

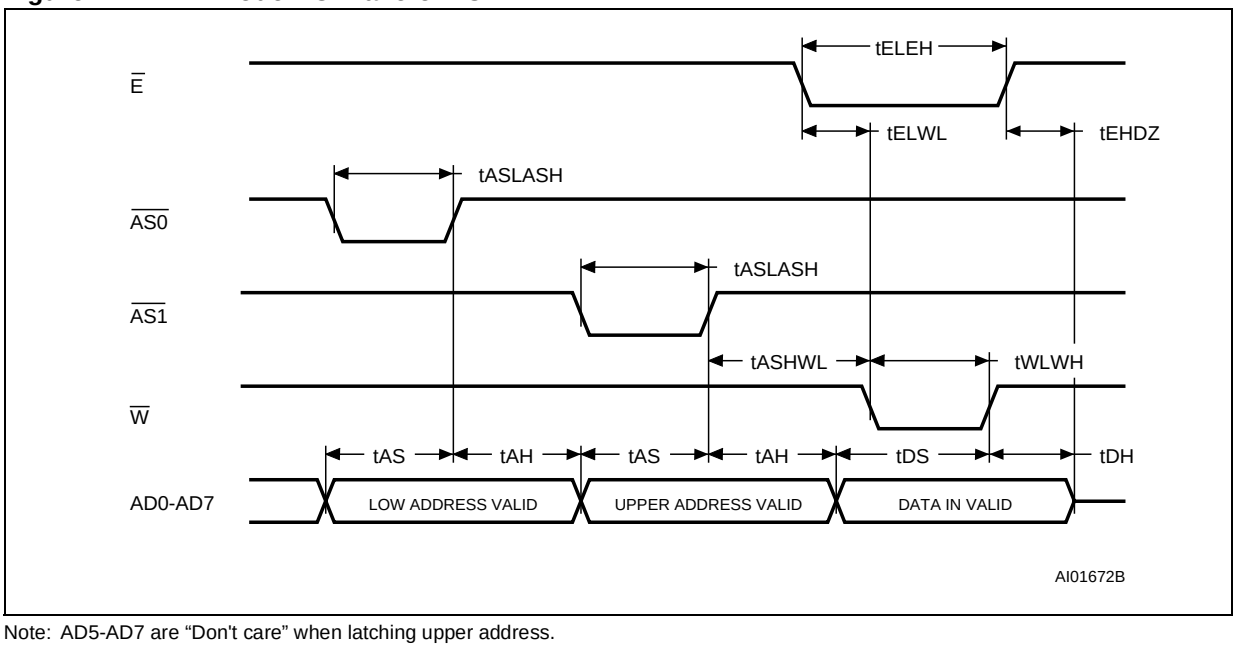
The $\overline{W}$ and $\overline{R}$ signals should never be active at the same time. In addition, $\overline{E}$ must be active before any control line is recognized (except for AD0-AD7 and $\overline{AS0}$, $\overline{AS1}$).

**Figure 6. READ Mode AC Waveforms**




Note: AD5-AD7 are “Don't care” when latching upper address.

## Figure 7. WRITE Mode AC Waveforms




Note: AD5-AD7 are “Don't care” when latching upper address.

## Table 7. AC Characteristics

| Symbol | Parameter(1) | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AS}$ | Address Setup Time | 20 | | ns |
| $t_{AH}$ | Address Hold Time | 0 | | ns |
| $t_{DS}$ | Data Setup Time | 60 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | ns |
| $t_{RLDV}$ | READ Enable Access Time | | 70 | ns |
| $t_{RLRH}$ | $\overline{R}$ Pulse Width Low | 70 | | ns |
| $t_{RHDZ}$ | READ Enable High to Output High Z | | 25 | ns |
| $t_{WLWH}$ | $\overline{W}$ Pulse Width Low | 50 | | ns |
| $t_{ELEH}$ | $\overline{E}$ Pulse Width Low | 50 | | ns |
| $t_{ASLASH}$ | $\overline{AS0}$, $\overline{AS1}$ Pulse Width Low | 15 | | ns |
| $t_{ASHRL}$ | $\overline{AS0}$, $\overline{AS1}$ High to $\overline{R}$ Low | 15 | | ns |
| $t_{ASHWL}$ | $\overline{AS0}$, $\overline{AS1}$ High to $\overline{W}$ Low | 15 | | ns |
| $t_{ELRL}$ | Chip Enable Low to READ Enable Low | 0 | | ns |
| $t_{EHDZ}$ | Chip Enable High to Data Output Hi-Z | 0 | | ns |
| $t_{ELWL}$ | Chip Enable Low to WRITE Enable Low | 0 | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).

### Data Retention Mode

Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when $V_{CC}$ falls within the $V_{PFD}$ (max), $V_{PFD}$ (min) window. All outputs become high impedance, and all inputs are treated as “Don't care.”

**Note:** A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below $V_{PFD}$ (min), the user can be assured the memory will be in a write protected state, provided the $V_{CC}$ fall time is not less than $t_F$.

The M48T559Y may respond to transient noise spikes on $V_{CC}$ that reach into the deselect window during the time the device is sampling $V_{CC}$. Therefore, decoupling of the power supply lines is recommended.

When $V_{CC}$ drops below $V_{SO}$, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T559Y for an accumulated period of at least 7 years when $V_{CC}$ is less than $V_{SO}$. As system power returns and $V_{CC}$ rises above $V_{SO}$, the battery is disconnected, and the power supply is switched to external $V_{CC}$. Write protection continues until $V_{CC}$ reaches $V_{PFD}$ (max) plus $t_{REC}$.

For more information on Battery Storage Life refer to the Application Note AN1012.

**Figure 8. Power Down/Up Mode AC Waveforms**

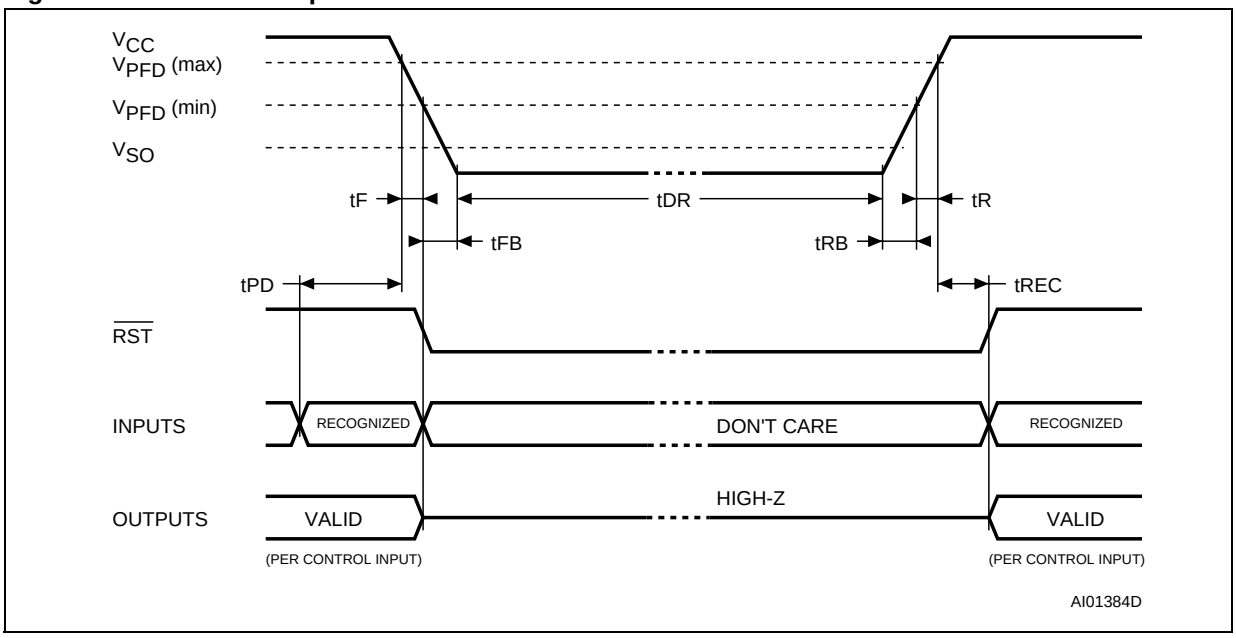



**Table 8. Power Down/Up AC Characteristics**

| Symbol | Parameter(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_F$(2) | $V_{PFD}$ (max) to $V_{PFD}$ (min) $V_{CC}$ Fall Time | 300 | | | µs |
| $t_{FB}$(3) | $V_{PFD}$ (min) to $V_{SS}$ $V_{CC}$ Fall Time | 10 | | | µs |
| $t_{PD}$ | $\overline{EX}$ at $V_{IH}$ before Power Down | 0 | | | µs |
| $t_R$ | $V_{PFD}$ (min) to $V_{PFD}$ (max) $V_{CC}$ Rise Time | 10 | | | µs |
| $t_{RB}$ | $V_{SS}$ to $V_{PFD}$ (min) $V_{CC}$ Rise Time | 1 | | | µs |
| $t_{REC}$ | $V_{PFD}$ (max) to $\overline{RST}$ High | 40 | | 200 | ms |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).
2. $V_{PFD}$ (max) to $V_{PFD}$ (min) fall time of less than $t_F$ may result in deselection/write protection not occurring until 200µs after $V_{CC}$ passes $V_{PFD}$ (min).
3. $V_{PFD}$ (min) to $V_{SS}$ fall time of less than $t_{FB}$ may cause corruption of RAM data.

**Table 9. Power Down/Up Trip Points DC Characteristics**

| Symbol | Parameter(1,2) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{PFD}$ | Power-fail Deselect Voltage | 4.2 | 4.35 | 4.5 | V |
| $V_{SO}$ | Battery Back-up Switchover Voltage | | 3.0 | | V |
| $t_{DR}$(3) | Expected Data Retention Time | 7 | | | YEARS |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).
2. All voltages referenced to $V_{SS}$.
3. At 25°C, $V_{CC}$ = 0V (when using SOH28 + M4T28-BR12SH SNAPHAT® top).

## CLOCK OPERATION

### Reading the Clock

Updates to the TIMEKEEPER® registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT™ TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ Bit, D6 in the Control register (1FF8h). As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0.'

### Setting the Clock

Bit D7 of the Control register (1FF8h) is the WRITE Bit. Setting the WRITE Bit to a '1,' like the READ Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10, page 14). Resetting the WRITE Bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE Bit is reset, the next clock update will occur in one second.

See the Application Note AN923, “TIMEKEEPER rolling into the 21st Century” for information on Century Rollover.

### Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP Bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T559Y is shipped from STMicroelectronics with the STOP Bit set to a '1.' When reset to a '0,' the M48T559Y oscillator starts within one second.

### Table 10. Register Map

| Address | Data | | | | | | | | Function/Range BCD Format | |
|---|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 1FFFh | 10 Years | | | | Year | | | | Year | 00-99 |
| 1FFEh | 0 | 0 | 0 | 10 M | Month | | | | Month | 01-12 |
| 1FFDh | 0 | 0 | 10 Date | | Date | | | | Date | 01-31 |
| 1FFCh | 0 | FT | 0 | 0 | 0 | Day | | | Day | 01-07 |
| 1FFBh | 0 | 0 | 10 Hours | | Hours | | | | Hours | 00-23 |
| 1FFAh | 0 | 10 Minutes | | | Minutes | | | | Minutes | 00-59 |
| 1FF9h | ST | 10 Seconds | | | Seconds | | | | Seconds | 00-59 |
| 1FF8h | W | R | S | Calibration | | | | | Control | |
| 1FF7h | WDS | BMB4 | BMB3 | BMB2 | BMB1 | BMB0 | RB1 | RB0 | Watchdog | |
| 1FF6h | AFE | Y | ABE | Y | Y | Y | Y | Y | Interrupts | |
| 1FF5h | RPT4 | Y | Al. 10 Date | | Alarm Date | | | | Alarm Date | 01-31 |
| 1FF4h | RPT3 | Y | Al. 10 Hours | | Alarm Hours | | | | Alarm Hours | 00-23 |
| 1FF3h | RPT2 | Alarm 10 Minutes | | | Alarm Minutes | | | | Alarm Minutes | 00-59 |
| 1FF2h | RPT1 | Alarm 10 Seconds | | | Alarm Seconds | | | | Alarm Seconds | 00-59 |
| 1FF1h | Y | Y | Y | Y | Y | Y | Y | Y | Unused | |
| 1FF0h | WDF | AF | Z | BL | Z | Z | Z | Z | Flags | |

Keys: S = SIGN Bit
FT = FREQUENCY TEST Bit
R = READ Bit
W =WRITE Bit
ST = STOP Bit
0 = Must be set to '0'
Y = '1' or '0'
Z = '0' and is Read only
AF = Alarm Flag (Read only)
BL = Battery Low Flag (Read only)
WDS = Watchdog Steering Bit
BMB0-BMB4 = Watchdog Multiplier Bits
RB0-RB1 = Watchdog Resolution Bits
AFE = Alarm Flag Enable Flag
ABE = Alarm in Battery Back-Up Mode Enable
RPT1-RPT4 = Alarm Repeat Mode Bits
WDF = Watchdog Flag (Read only)

### Calibrating the Clock

The M48T559Y is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not exceed +/–35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about +/–1.53 minutes per month. When the Calibration circuit is properly employed, accuracy improves to better than +1/–2 PPM at 25°C.

The oscillation rate of crystals changes with temperature (see Figure 12, page 19). Therefore, the M48T559Y design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 13, page 19. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration Bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration Bits occupy the five lower order bits (D4-D0) in the Control Register (1FF8h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign Bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T559Y may require:

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in Application Note AN934: TIMEKEEPER CALIBRATION. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the Calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{\text{IRQ}}$/FT pin. The pin will toggle at 512Hz, when the Stop Bit (ST, D7 of 1FF9h) is '0,' the Frequency Test Bit (FT, D6 of 1FFCh) is '1,' the Alarm Flag Enable Bit (AFE, D7 of 1FF6h) is '0,' and the Watchdog Steering Bit (WDS, D7 of 1FF7h) is '1' or the Watchdog Register (1FF7h = 0) is reset.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 PPM oscillator frequency error, requiring a –10 (XX001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The FT Bit is cleared on power-down.

For more information on calibration, see the Application Note AN934, “TIMEKEEPER Calibration”.

The $\overline{\text{IRQ}}$/FT pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time.

### Setting the Alarm Clock

Registers 1FF5h-1FF2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second or repeat every month, day, hour, minute, or second. It can also be programmed to go off while the M48T559Y is in the battery back-up to serve as a system wake-up call.

Bits RPT1–RPT4 put the alarm in the repeat mode of operation. Table 11, page 16 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

**Note:** User must transition address (or toggle chip enable) to see Flag Bit change.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT1–RPT4, the AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{\text{IRQ}}$/FT pin. To disable alarm, write '0' to the Alarm Date Register and to RPT1-RPT4. The Alarm Flag and the $\overline{\text{IRQ}}$/FT output are cleared by a READ to the Flags Register as shown in Figure 9, page 16. A subsequent READ to the Flags Register is necessary to see that the value of the Alarm Flag has been reset to '0.'

**Note:** If an alarm condition occurs while the Flags Register address is latched into the address buffer, the alarm flag will not be set until an address other than the Flags Register (1FF0h) is latched into the address buffer. This will insure that the alarm flag will not be inadvertently reset while reading the flag register. To properly check to see if an alarm condition has occurred while reading the flag register, the user is required to latch, read or write to an alternate address and then re-read the alarm flag.

The $\overline{IRQ}$/FT pin can also be activated in the battery back-up mode. The $\overline{IRQ}$/FT will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE Bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M48T559Y was in the deselect mode during power-up. Figure 10, page 17 illustrates the back-up mode alarm timing.

**Figure 9. Alarm Interrupt Reset Waveform**

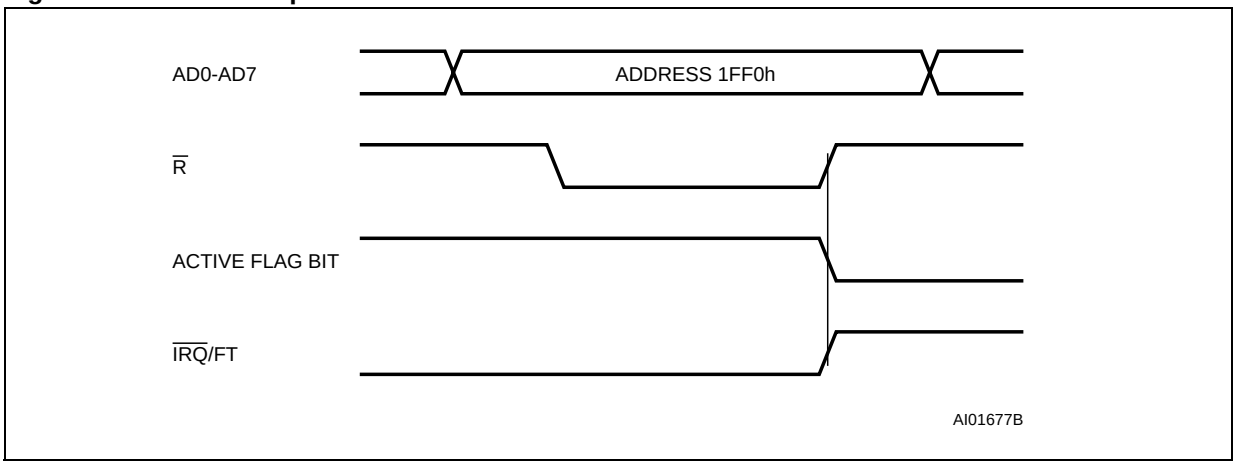
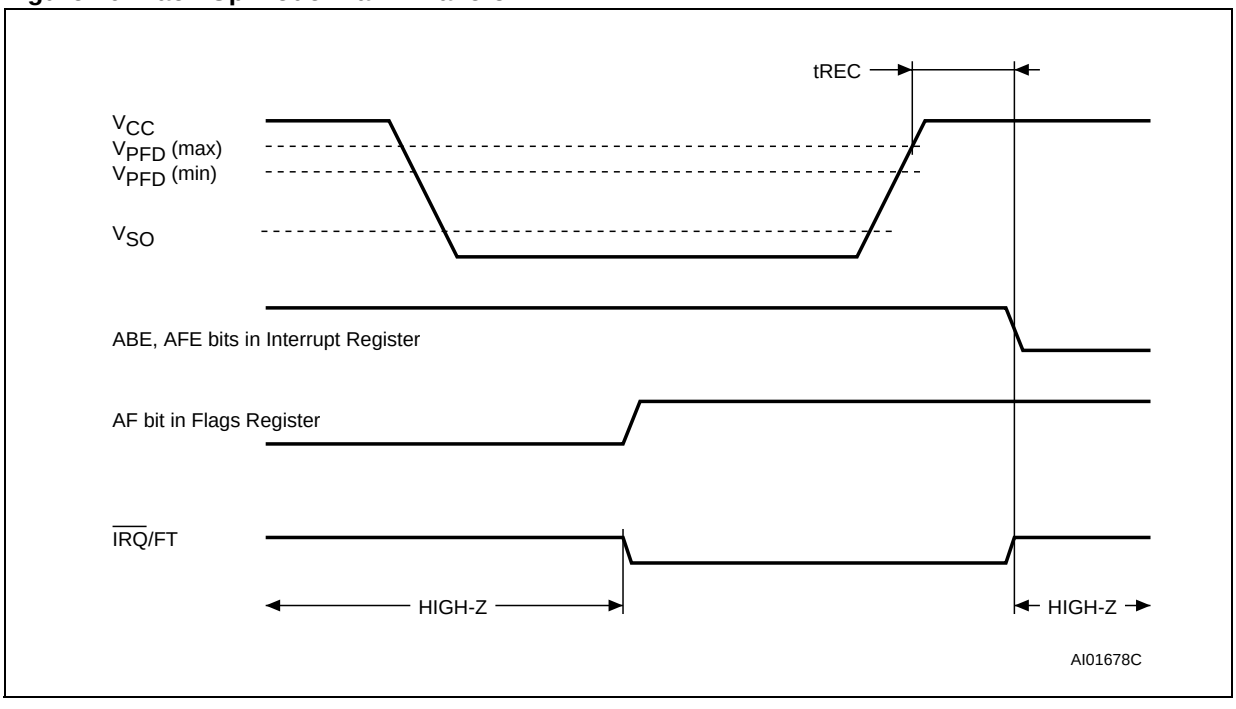



**Table 11. Alarm Repeat Modes**

| RPT4 | RPT3 | RPT2 | RPT1 | Alarm Activated |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | Once per Second |
| 1 | 1 | 1 | 0 | Once per Minute |
| 1 | 1 | 0 | 0 | Once per Hour |
| 1 | 0 | 0 | 0 | Once per Day |
| 0 | 0 | 0 | 0 | Once per Month |

**Figure 10. Back-Up Mode Alarm Waveform**




## Watchdog Timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the eight-bit Watchdog Register (Address 1FF7h). The five bits (BMB4-BMB0) store a binary multiplier and the two lower order bits (RB1-RB0) select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3 x 1 or 3 seconds).

**Note**: Accuracy of timer is within ± the selected resolution.

If the processor does not reset the timer within the specified period, the M48T559Y sets the WDF (Watchdog Flag) and generates a watchdog interrupt or a microprocessor reset. WDF is reset by reading the Flags Register (Address 1FF0h).

The most significant bit of the Watchdog Register is the Watchdog Steering Bit. When set to a '0,' the watchdog will activate the IRQ/FT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the RST pin for a duration of 40ms to 200ms. The Watchdog register, FT, AFE, and ABE bits will reset to a '0' at the end of a watchdog time-out when the WDS Bit is set to a '1.'

The watchdog timer can be reset by two methods:

– a transition (high-to-low or low-to-high) can be applied to the Watchdog input pin (WDI); or
– the microprocessor can perform a WRITE of the Watchdog Register. The time-out period then starts over. The WDI pin contains a pull-down resistor and therefore must be grounded if not used.

The watchdog timer will be reset on each transition (edge) seen by the WDI pin. In order to perform a software reset of the Watchdog timer, the original time-out period can be written into the Watchdog Register, effectively restarting the count-down cycle.

Should the watchdog timer time-out, and the WDS Bit is programmed to output an interrupt, a value of 00h needs to be written to the Watchdog Register in order to clear the IRQ/FT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the Flags Register will reset the Watchdog Flag (D7; Address 1FF0h).

The watchdog function is automatically disabled upon power-down and the Watchdog Register is cleared. If the watchdog function is set to output to the IRQ/FT pin and the frequency test function is activated, the watchdog or alarm function prevails and the frequency test function is denied.

### Power-on Reset

The M48T559Y continuously monitors $V_{CC}$. When $V_{CC}$ falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for 40ms to 200ms after $V_{CC}$ passes $V_{PFD}$ (max). An external pull-up resistor to $V_{CC}$ is required (1KΩ resistor is recommended). The reset pulse remains active with $V_{CC}$ at $V_{SS}$.

### Reset Inputs ($\overline{RSTIN1}$ & $\overline{RSTIN2}$)

The M48T559Y provides two independent inputs which can generate an output reset. The duration and function of these resets is identical to a reset generated by a power cycle. Table 12 and Figure 11 illustrate the AC reset characteristics of this function. Pulses shorter than $t_{R1}$ and $t_{R2}$ will not generate a reset condition. $\overline{RSTIN1}$ and $\overline{RSTIN2}$ are each internally pulled up to $V_{CC}$ through a 100kΩ resistor.

### Battery Low Warning

The M48T559Y checks its battery voltage on power-up. The BL (Battery Low) Bit (D4 of 1FF0h) will be set on power-up if the battery voltage is less than 2.5V (typical).

### Initial Power-on Defaults

Upon application of power to the device, the following register bits are set to a '0' state: WDS; BMB0-BMB4; RB0-RB1; AFE; ABE; W; R; and FT.

**Figure 11. $\overline{RSTIN1}$ & $\overline{RSTIN2}$ Timing Waveforms**

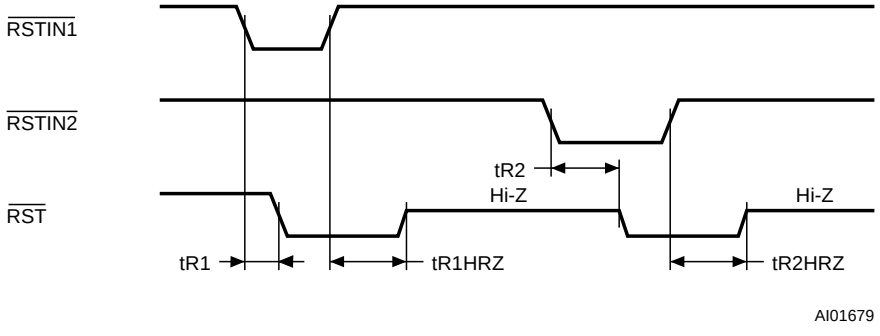



**Table 12. Reset AC Characteristics**

| Symbol | Parameter(1) | Min | Max | Unit |
|---|---|---|---|---|
| $t_{R1}$ | $\overline{RSTIN1}$ Low to $\overline{RST}$ Low | 50 | 200 | ns |
| $t_{R2}$ | $\overline{RSTIN2}$ Low to $\overline{RST}$ Low | 20 | 100 | ms |
| $t_{R1HRZ}$(2) | $\overline{RSTIN1}$ High to $\overline{RST}$ Hi-Z | 40 | 200 | ms |
| $t_{R2HRZ}$(2) | $\overline{RSTIN2}$ High to $\overline{RST}$ Hi-Z | 40 | 200 | ms |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).
2. $C_L$ = 5pF (see Figure 5, page 7).

**Figure 12. Crystal Accuracy Across Temperature**

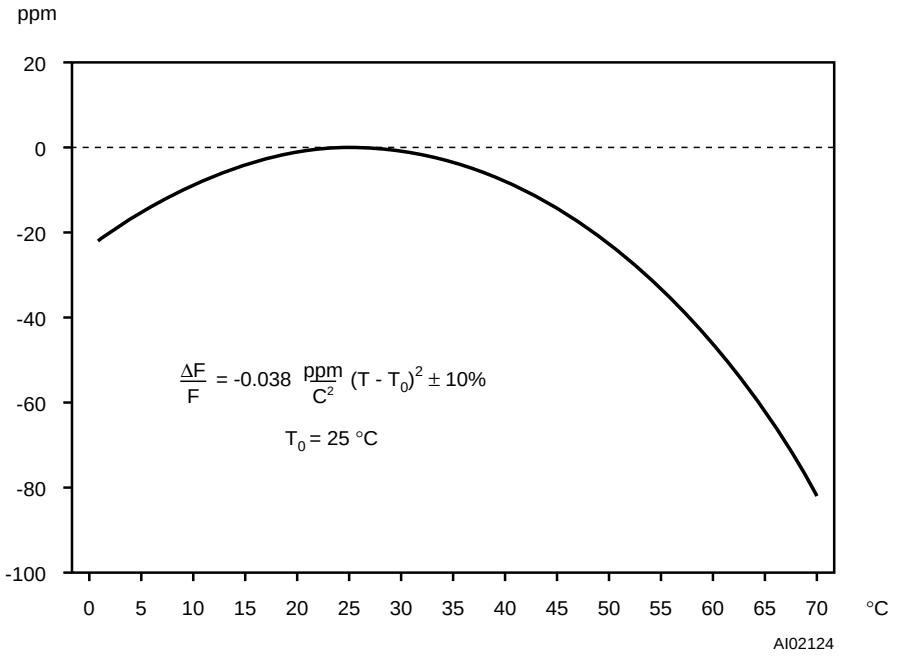
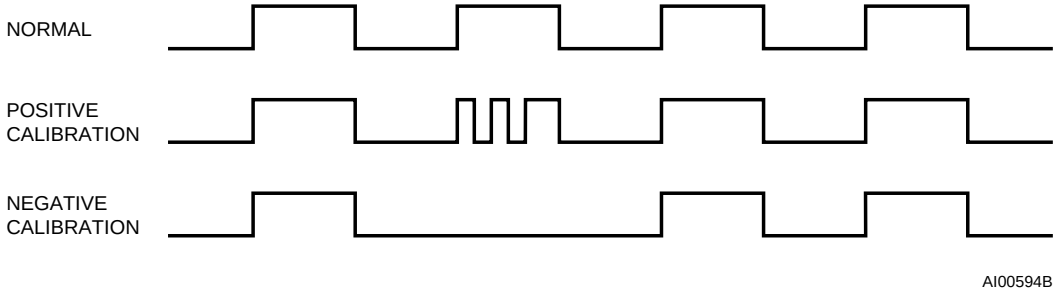



**Figure 13. Calibration Waveform**

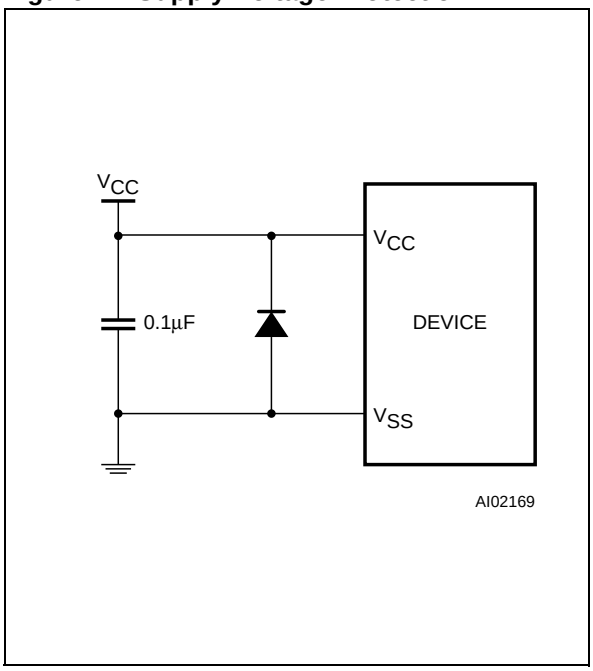


### $V_{CC}$ Noise And Negative Going Transients

$I_{CC}$ transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the $V_{CC}$ bus. These transients can be reduced if capacitors are used to store energy which stabilizes the $V_{CC}$ bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (as shown in Figure 14) is recommended in order to provide the needed filtering.

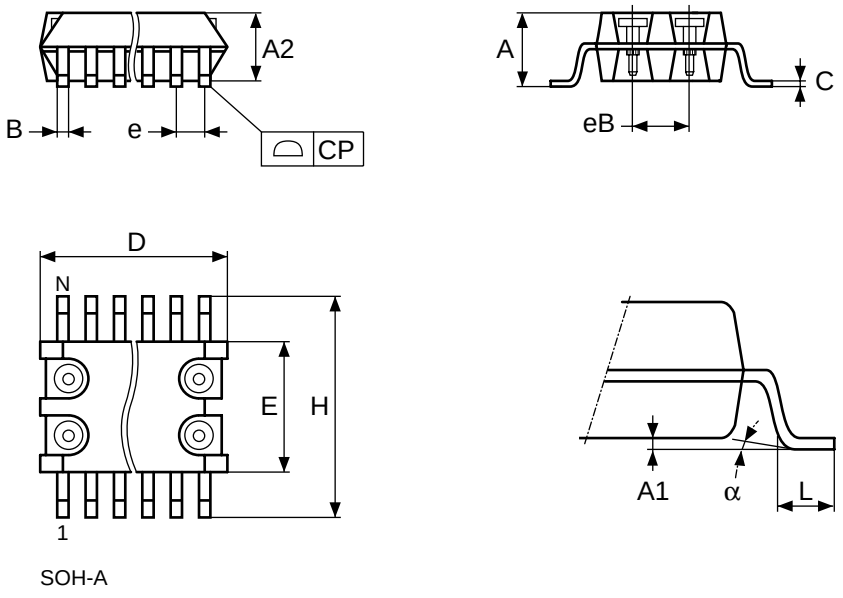
In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on $V_{CC}$ that drive it to values below $V_{SS}$ by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from $V_{CC}$ to $V_{SS}$ (cathode connected to $V_{CC}$, anode to $V_{SS}$). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

**Figure 14. Supply Voltage Protection**



## PACKAGE MECHANICAL INFORMATION

**Figure 15. SOH28 – 28-lead Plastic Small Outline, Battery SNAPHAT, Package Outline**

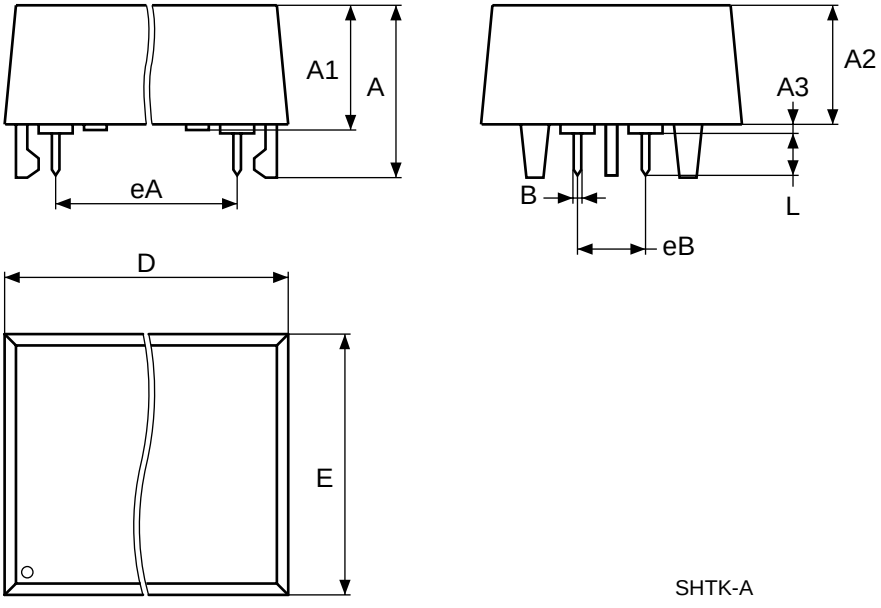



Note: Drawing is not to scale.

**Table 13. SOH28 – 28-lead Plastic Small Outline, battery SNAPHAT, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 3.05 | | | 0.120 |
| A1 | | 0.05 | 0.36 | | 0.002 | 0.014 |
| A2 | | 2.34 | 2.69 | | 0.092 | 0.106 |
| B | | 0.36 | 0.51 | | 0.014 | 0.020 |
| C | | 0.15 | 0.32 | | 0.006 | 0.012 |
| D | | 17.71 | 18.49 | | 0.697 | 0.728 |
| E | | 8.23 | 8.89 | | 0.324 | 0.350 |
| e | 1.27 | – | – | 0.050 | – | – |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| H | | 11.51 | 12.70 | | 0.453 | 0.500 |
| L | | 0.41 | 1.27 | | 0.016 | 0.050 |
| α | | 0° | 8° | | 0° | 8° |
| N | 28 | | | 28 | | |
| CP | | | 0.10 | | | 0.004 |

**Figure 16. SH – 4-pin SNAPHAT Housing for 48mAh Battery & Crystal, Package Outline**

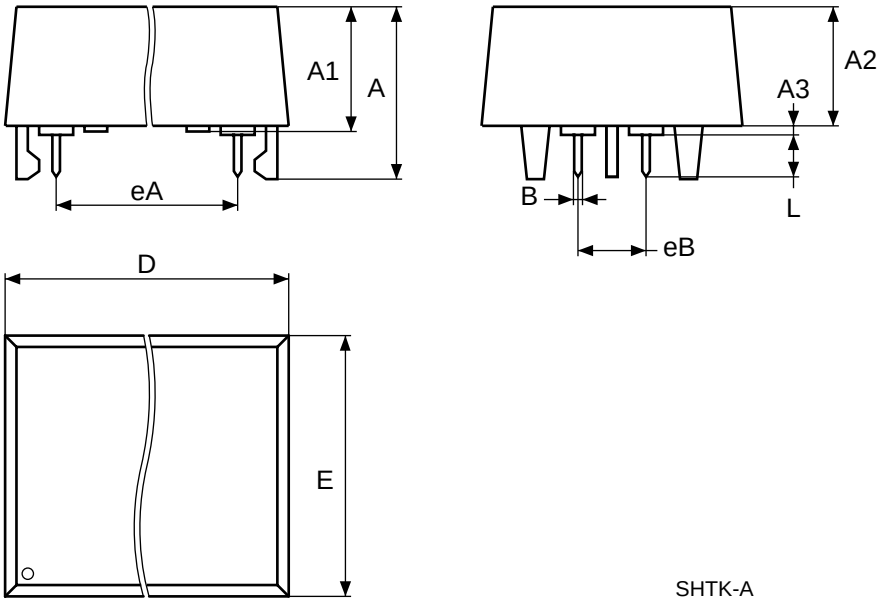



Note: Drawing is not to scale.

**Table 14. SH – 4-pin SNAPHAT Housing for 48mAh Battery & Crystal, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 9.78 | | | 0.385 |
| A1 | | 6.73 | 7.24 | | 0.265 | 0.285 |
| A2 | | 6.48 | 6.99 | | 0.255 | 0.275 |
| A3 | | | 0.38 | | | 0.015 |
| B | | 0.46 | 0.56 | | 0.018 | 0.022 |
| D | | 21.21 | 21.84 | | 0.835 | 0.860 |
| E | | 14.22 | 14.99 | | 0.560 | 0.590 |
| eA | | 15.55 | 15.95 | | 0.612 | 0.628 |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| L | | 2.03 | 2.29 | | 0.080 | 0.090 |

**Figure 17. SH – 4-pin SNAPHAT Housing for 120mAh Battery & Crystal, Package Outline**




Note: Drawing is not to scale.

**Table 15. SH – 4-pin SNAPHAT Housing for 120mAh Battery & Crystal, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 10.54 | | | 0.415 |
| A1 | | 8.00 | 8.51 | | 0.315 | 0.335 |
| A2 | | 7.24 | 8.00 | | 0.285 | 0.315 |
| A3 | | | 0.38 | | | 0.015 |
| B | | 0.46 | 0.56 | | 0.018 | 0.022 |
| D | | 21.21 | 21.84 | | 0.835 | 0.860 |
| E | | 17.27 | 18.03 | | 0.680 | 0.710 |
| eA | | 15.55 | 15.95 | | 0.612 | 0.628 |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| L | | 2.03 | 2.29 | | 0.080 | 0.090 |

## PART NUMBERING

### Table 16. Ordering Information Scheme

Example: M48T 559Y MH 6 TR

**Device Type**

M48T

**Supply Voltage and Write Protect Voltage**

559Y = $V_{CC}$ = 4.5 to 5.5V; $V_{PFD}$ = 4.2 to 4.5V

**Package**

MH(1) = SOH28

**Temperature Range**

1 = 0 to 70°C

**Shipping Method for SOIC**

blank = Tubes

TR = Tape & Reel

Note: 1. The 28-pin SOIC package (SOH28) requires the battery/crystal package (SNAPHAT®) which is ordered separately under the part number “M4TXX-BR12SHX” in plastic tube or “M4TXX-BR12SHXTR” in Tape & Reel form.

**Caution:** Do not place the SNAPHAT battery package “M4TXX-BR12SH” in conductive foam as it will drain the lithium button-cell battery.

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

### Table 17. SNAPHAT Battery Table

| Part Number | Description | Package |
|---|---|---|
| M4T28-BR12SH | Lithium Battery (48mAh) and Crystal SNAPHAT | SH |
| M4T32-BR12SH | Lithium Battery (120mAh) and Crystal SNAPHAT | SH |

## REVISION HISTORY

### Table 18. Document Revision History

| Date | Rev. # | Revision Details |
|---|---|---|
| June 1998 | 1.0 | First Issue |
| 07-Feb-00 | 1.1 | Description Paragraph changed; setting Alarm Clock paragraph changed; M4T28-BR12SH SNAPHAT Housing for 48mAh Battery & Crystal Package added (Table 14); Power Down/ Up Mode AC Waveforms changed (Figure 8); Back-up Mode Alarm Waveforms changed (Figure 10) |
| 13-Aug-01 | 2.0 | Reformatted; added temperature information (Tables 4, 5, 7, 8, 9) |
| 20-May-02 | 2.1 | Modify reflow time and temperature footnote (Table 2) |
| 31-Mar-03 | 3.0 | v2.2 template applied; data retention condition updated (Table 9) |

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