HM-6551

March 1997

256 x 4 CMOS RAM

Features

- **Low Power Standby. . . . . 50μW Max**
- **Low Power Operation . . . . . .20mW/MHz Max**
- **Fast Access Time . . . . . 220ns Max**
- **Data Retention . . . . . .at 2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 1 TTL Load**
- **Internal Latched Chip Select**
- **High Noise Immunity**
- **On-Chip Address Register**
- **Latched Outputs**
- **Three-State Output**

Description

The HM-6551 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

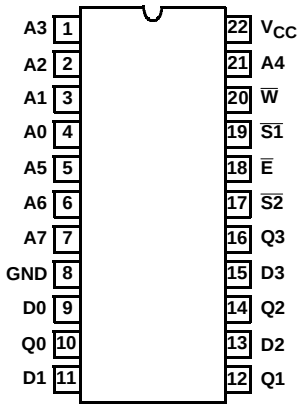
The HM-6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over-temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	220ns	300ns	PKG. NO.
Plastic DIP	-40^{o}C to +85^{o}C	HM3-6551B-9	HM3-6551-9	E22.4
CERDIP	-40^{o}C to +85^{o}C	HM1-6551B-9	HM1-6551-9	F22.4

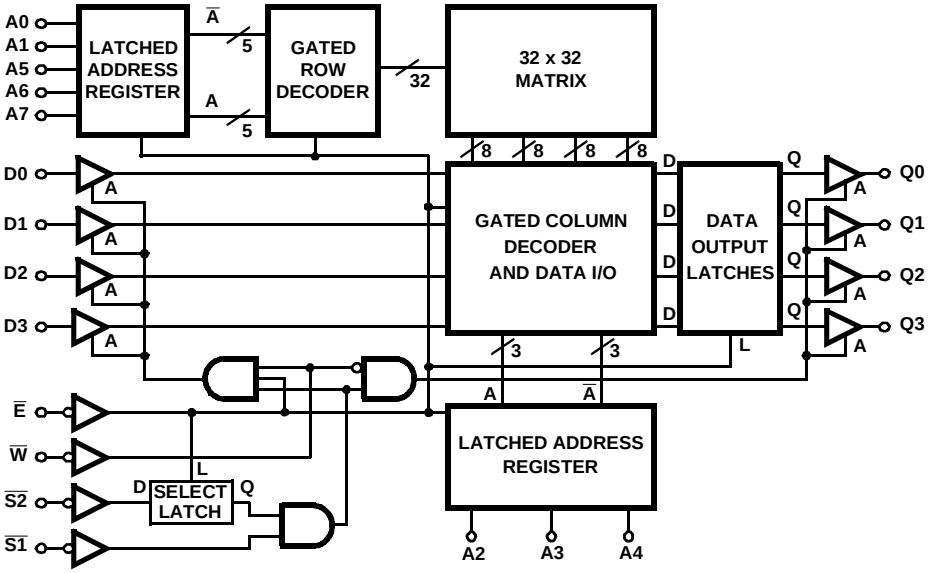
Pinout

HM-6551
(PDIP, CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write E5able
$\overline{S}$	Chip Select
D	Data Input
Q	Data Output

Functional Diagram



NOTES:

1. Select Latch: L Low $\rightarrow$ Q = D and Q latches on rising edge of L.
2. Address Latches And Gated Decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.
3. All lines positive logic-active high.
4. Three-State Buffers: A high $\rightarrow$ output active.
5. Data Latches: L High $\rightarrow$ Q = D and Q latches on falling edge of L.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-6551B-9, HM-6551-9 . . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
CERDIP Package	$60^oC/W$	$15^oC/W$
Plastic DIP Package	$75^oC/W$	N/A

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature
Ceramic Package . . . . . $+175^oC$
Plastic Package . . . . . $+150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 1930 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40^oC to $+85^oC$ (HM-6551B-9, HM-6551-9)

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
ICCSB	Standby Supply Current	-	10	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
ICCOP	Operating Supply Current (Note 1)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0mA, V_{CC} = 5.5V, VI = V_{CC} or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	10	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage	-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage	V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA, V_{CC} = 4.5V
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA, V_{CC} = 4.5V

Capacitance T_A = $+25^oC$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	f = 1MHz, All measurements are referenced to device GND
CO	Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 1.5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6551B-9, HM-6551-9)

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS
		HM-6551B-9		HM-6551-9			
		MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	220	-	300	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	220	-	300	ns	(Notes 1, 3, 4)
(3) TS1LQX	Chip Select 1 Output Enable Time	5	130	5	150	ns	(Notes 2, 3)
(4) TWLQZ	Write Enable Output Disable Time	-	130	-	150	ns	(Notes 2, 3)
(5) TS1HQZ	Chip Select 1 Output Disable Time	-	130	-	150	ns	(Notes 2, 3)
(6) TELEH	Chip Enable Pulse Negative Width	220	-	300	-	ns	(Notes 1, 3)
(7) TEHEL	Chip Enable Pulse Positive Width	100	-	100	-	ns	(Notes 1, 3)
(8) TAVEL	Address Setup Time	0	-	0	-	ns	(Notes 1, 3)
(9) TS2LEL	Chip Select 2 Output Disable Time	0	-	0	-	ns	(Notes 1, 3)
(10) TELAX	Address Hold Time	40	-	50	-	ns	(Notes 1, 3)
(11) TELS2X	Chip Select 2 Hold Time	40	-	50			(Notes 1, 3)
(12) TDVWH	Data Setup Time	100	-	150	-	ns	(Notes 1, 3)
(13) TWHDX	Data Hold Time	0	-	0	-	ns	(Notes 1, 3)
(14) TWLS1H	Chip Select 1 Write Pulse Setup Time	120	-	180	-	ns	(Notes 1, 3)
(15) TWLEH	Chip Enable Write Pulse Setup Time	120	-	180	-	ns	(Notes 1, 3)
(16) TS1LWH	Chip Select 1 Write Pulse Hold Time	120	-	180	-	ns	(Notes 1, 3)
(17) TELWH	Chip Enable Write Pulse Hold Time	120	-	180	-	ns	(Notes 1, 3)
(18) TWLWH	Write Enable Pulse Width	120	-	180	-	ns	(Notes 1, 3)
(19) TELEL	Read or Write Cycle Time	320	-	400	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

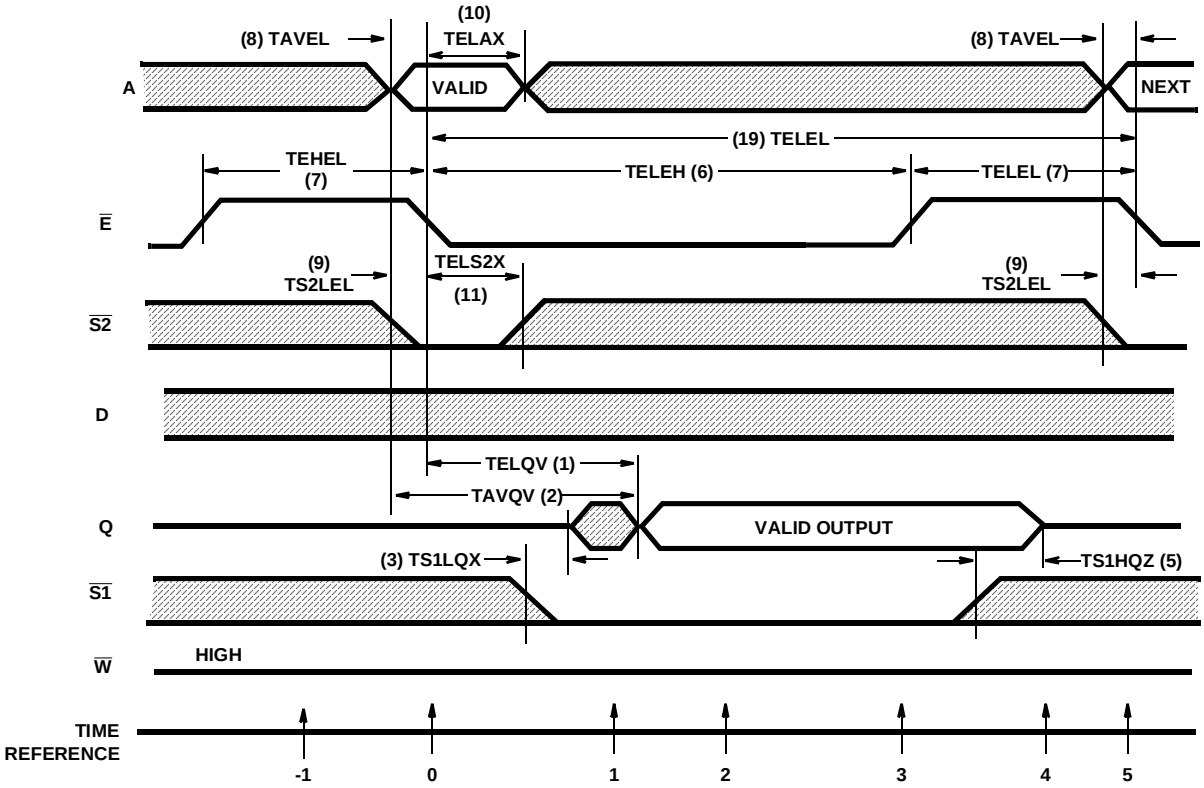


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	X	L	H	V	X	Z	Addresses and $\overline{S2}$ are Latched, Cycle Begins
1	L	L	X	H	X	X	X	Output Enabled but Undefined
2	L	L	X	H	X	X	V	Data Output Valid
3	↗	L	X	H	X	X	V	Outputs Latched, Valid Data, $\overline{S2}$ Unlatches
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The HM-6551 Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on chip registers, providing the minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV). The HM-6551 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Also on the rising edge of $\overline{E}$, $\overline{S2}$ unlatches and controls the outputs along with $\overline{S1}$. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

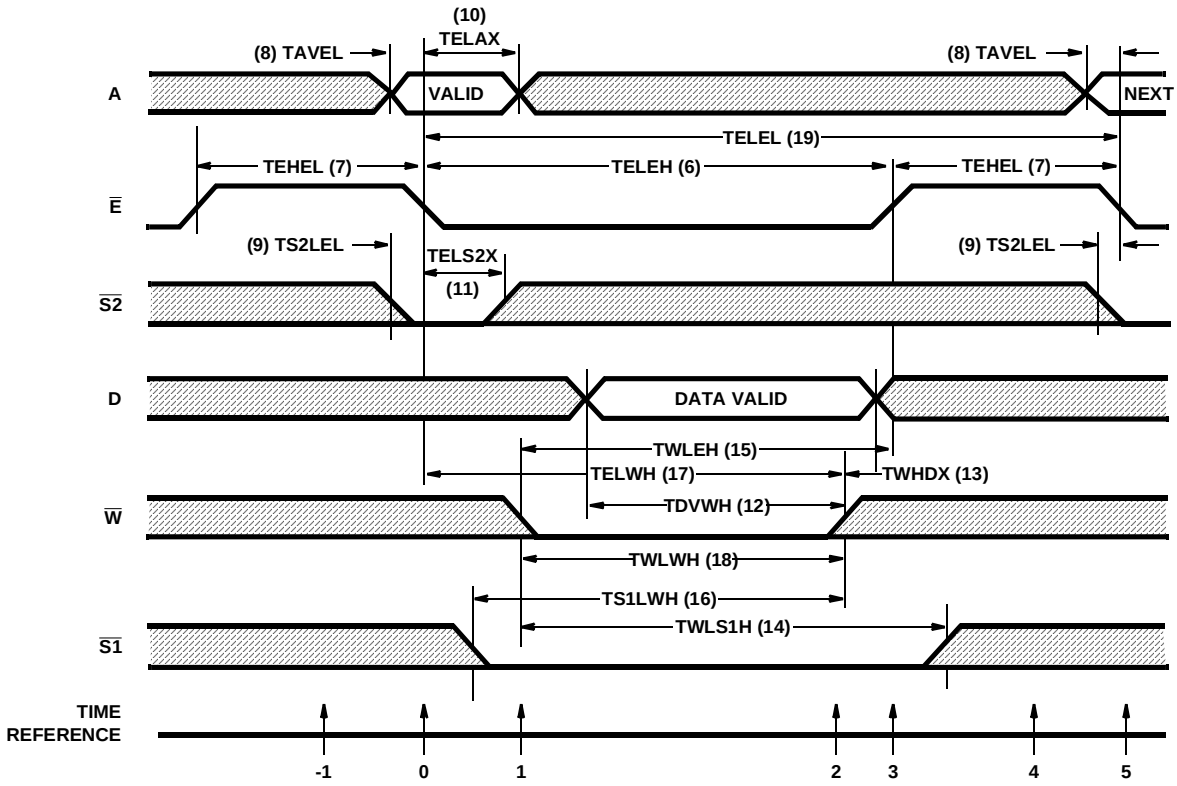


FIGURE 2. WRITE CYCLE

TRUTH TABLE

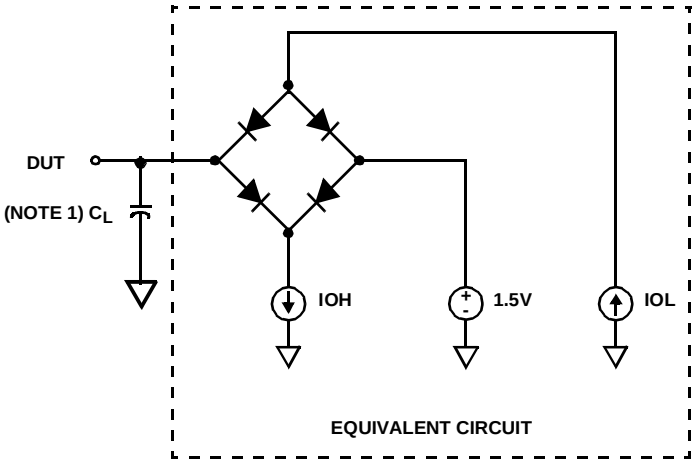
TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↓	X	L	X	V	X	Z	Cycle Begins, Addresses and $\overline{S2}$ are Latched
1	L	L	X	↓	X	X	Z	Write Period Begins
2	L	L	X	↑	X	V	Z	Data In is Written
3	↑	X	X	H	X	X	Z	Write is Completed
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	L	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched simultaneously. The $\overline{W}$ line may go low at any time during the cycle, providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HM-6551 may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.

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