250kSPS 16-BIT ADC in µSO

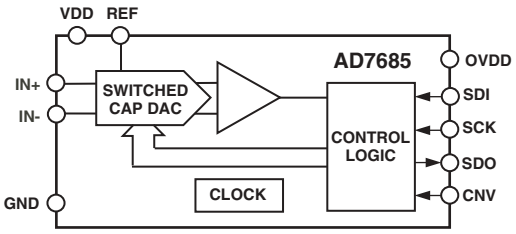
Preliminary Technical Data — AD7685*

FEATURES

16 Bits Resolution with No Missing 16-Bit Codes
Throughput: 250 kSPS
INL: ± 3LSB Max (±0.0046 % of Full-Scale)
S/(N+D): 89 dB Typ @ 10 kHz
THD: –95 dB Typ @ 10 kHz
Pseudo-Differential Analog input range:
0V to V_{REF} with V_{REF} up to VDD
No Pipeline Delay
Single Supply Operation 5V and 2.7V with 2.5V/3V/5V logic interface
Multiple ADCs Daisy Chain and Busy Indicator
Serial Interface SPI/QSPI/µWire/DSP compatible
20 mW @ 5V/250ksps, TBD @ 3V Typical Power Dissipation,
80 µW @ 1 kSPS
Stand-by current (acquisition phase): 1 µA Max
µ-SOIC Package (µ-SO8 size)
Pin-to-Pin Compatible with the AD7686, AD7687, AD7688

Battery Powered Equipment
Data Acquisition
Instrumentation
Medical Instruments
Process Control

FUNCTIONAL BLOCK DIAGRAM



µSO PulSAR 16 Bit ADC

Type / kSPS	100 kSPS	250 kSPS	380 - 550 kSPS
True Differential	AD7684	AD7687	AD7688
Pseudo Differential	AD7683	AD7685	AD7686
Unipolar	AD7680		

GENERAL DESCRIPTION

The AD7685 is a 16-bit, 250 kSPS, charge redistribution successive-approximation, Analog-to-Digital Converter which operates from a single power supply. It contains a high-speed 16-Bit sampling ADC with no missing codes, an internal conversion clock, error correction circuits and a flexible serial interface port. The part also contain a low noise, wide bandwidth, very short aperture delay track/hold circuit which can sample an analog input range from 0V to REF. The reference voltage REF is applied externally and can be set up to the supply voltage.

The serial interface features the capability to "Daisy chain" several ADCs on a single 3 wire bus and provides an optional Busy indicator.

The AD7685 is hardware factory calibrated. It is fabricated using CMOS process and is housed in 10-lead µSOIC package with operation specified from –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Superior INL
The AD7685 has a maximum integral non linearity of 3 LSB with no missing 16-bit code.

2. 2.7V or 5V Single Supply Operation
The AD7685 operates from a single supply, dissipates only TBD mW typical, and even lower when a reduced throughput is used. It consumes 1 µA maximum during the acquisition phase.

3.Fast Throughput.
The AD7685 is a high speed 250 kSPS, charge redistribution, 16-Bit SAR ADC with no pipeline delay.

4. Serial Interface with OVDD, Daisy Chain and Busy
2.5V, 3 V or 5 V logic 3-wire serial interface arrangement compatible with SPI and DSP host.

*Patent pending.

REV. Pr G

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AD7685–SPECIFICATIONS

(T_A = -40°C to +85°C, V_{REF} = 5V, VDD = 5 V, OVDD = 2.3V to 5.25V, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ - IN-	0		V_{REF}	V
Absolute Input Voltage	IN+	–0.1		VDD+0.3	V
	IN-	–0.1		TBD	V
Analog Input CMRR	f_{IN} = TBD kHz		TBD		dB
Leakage Current at 25 °C	250kSPS Throughput		TBD		nA
Input Impedance			See Analog Input Section		
THROUGHPUT SPEED					
Complete Cycle				4	µs
Throughput Rate		0		250	kSPS
DC ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error		–3		+3	LSB[1]
Transition Noise			0.7		LSB
Gain Error[2], T_{MIN} to T_{MAX}	REF = 5 V			±TBD	% of FSR
Gain Error Temperature Drift			±TBD		ppm/°C
Offset Error[2], T_{MIN} to T_{MAX}			±TBD	±TBD	LSB
Offset Temperature Drift			±TBD		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±TBD		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = TBD kHz	88	89		dB[3]
Spurious Free Dynamic Range	f_{IN} = TBD kHz		95		dB
Total Harmonic Distortion	f_{IN} = TBD kHz		–95	TBD	dB
Signal-to-(Noise+Distortion)	f_{IN} = TBD kHz	88	89		dB
	f_{IN} = TBD kHz, –60 dB Input		29		dB
Intermodulation Distortion					
Second Order Terms			TBD		dB
Third Order Terms			TBD		dB
–3 dB Input Bandwidth			2		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			1.5	µs
REFERENCE					
External Reference Voltage		0.5		VDD+0.3	V
External Reference Current Drain	250kSPS Throughput		TBD		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}	OVDD = 2.7V to 5.25V	+2.0		OVDD + 0.3	V
	OVDD = 2.3V to 5.25V	+1.7		OVDD + 0.3	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format			Serial 16-Bits Straight Binary		
Pipeline Delay			Conversion Results Available Immediately After Completed Conversion		
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = –500 µA	OVDD – 0.3			V

NOTES

[1]LSB means Least Significant Bit. With the 5 V input range, one LSB is 76.3 µV.

[2]See Definition of Specifications section. These specifications do include full temperature range variation but do not include the error contribution from the external reference.

[3]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.

Specifications subject to change without notice.

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
VDD	Specified Performance	4.75	5	5.25	V
VDD Range		2.7		5.25	V
OVDD		2.7		5.25	V
Operating Current	250 kSPS Throughput				
VDD	VDD = 5V		TBD		mA
OVDD			TBD		µA
Power Dissipation (VDD = 5V)	250 kSPS Throughput[4]		20	TBD	mW
	1 kSPS Throughput[4]		80		µW
	During acquisition phase[4]			TBD	µW
TEMPERATURE RANGE[5]					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES
[4]With all digital inputs forced to OVDD or GND respectively.
[5]Contact factory for extended temperature range.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (–40°C to +85°C, VDD = 4.75 V to 5.25V, OVDD = 2.7 V to 5.25 V, unless otherwise stated)

	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data available	t_{CONV}	1.1		2.5	µs
Acquisition Time	t_{ACQ}	1.5			µs
Time Between Conversions	t_{CYC}	4			µs
CNV Pulse width ($\overline{CS}$ mode)	t_{CNVH}	5			ns
SCK Period	t_{SCK}	15			ns
SCK Low Time	t_{SCKH}	7			ns
SCK High Time	t_{SCKL}	7			ns
SCK Falling Edge to Data remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid delay	t_{DSDO}				
OVDD above 4.75V				13	ns
OVDD above 3V				20	ns
OVDD above 2.7V				27	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ mode)	t_{EN}				
OVDD above 4.75V				15	ns
OVDD above 2.7V				30	ns
CNV or SDI High or last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ mode)	t_{DIS}			30	ns
SDI valid Setup Time from CNV rising edge ($\overline{CS}$ mode)	$t_{SSDICNV}$	8			ns
SDI valid Hold Time from CNV rising edge ($\overline{CS}$ mode)	$t_{HSDICNV}$	0			ns
SCK valid Setup Time from CNV rising edge (Chain mode)	$t_{SSCKCNV}$	8			ns
SCK valid Hold Time from CNV rising edge (Chain mode)	$t_{HSCKCNV}$	5			ns
SDI valid Setup Time from SCK falling edge (Chain mode)	$t_{SSDISCK}$	8			ns
SDI valid Hold Time from SCK falling edge (Chain mode)	$t_{HSDISCK}$	0			ns
SDI High to SDO High (Chain mode with Busy indicator)	$t_{DSDOSDI}$				
OVDD above 4.75V				15	ns
OVDD above 2.7V				30	ns

Specifications subject to change without notice.

AD7685–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
IN+[2], IN-[2], REF, ...GND –0.3 V to VDD + 0.3 V
Supply Voltages
VDD, OVDD to GND ..... -0.3 V to 7 V
VDD to OVDD .....±7 V
Digital Inputs to GND ..... –0.3 V to OVDD + 0.3 V
Digital Outputs to GND .... –0.3 V to OVDD + 0.3 V
Internal Power Dissipation[3] ..... 325 mW
Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature Range
(Soldering 10 sec) ..... 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]See Analog Input section.
[3]Specification is for device in free air: μSOIC-10: θ_{JA} = 200°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Brand
AD7685BRM	–40°C to +85°C	μSOIC-10	RM-10	C01
AD7685BRMRL7	–40°C to +85°C	μSOIC-10	RM-10 (reel)	C01
EVAL-AD7685CB[1]		Evaluation Board		
EVAL-CONTROL BRD2[2]		Controller Board		
EVAL-CONTROL BRD3[2]		Controller Board		

NOTES
[1]This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRDx for evaluation/demonstration purposes.
[2]These boards allow a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

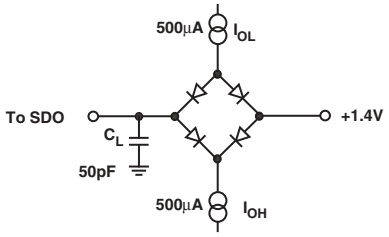


Figure 1. Load Circuit for Digital Interface Timing.

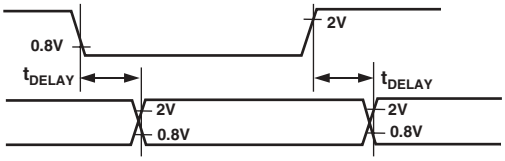
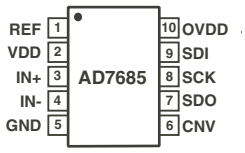


Figure 2. Voltage Reference Levels for Timing.

AD7685 PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7685 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin #	Mnemonic		Function
1	REF	AI	Reference Input Voltage. The REF range is from TBD to VDD. It is referred to the GND ground. This pin should be decoupled closely to the pin with a TBD µFcapacitor.
2	VDD	P	Input Power Supply.
3	IN+	AI	Analog Input. It is referred to IN-. The voltage range, difference between IN+ and IN-, is 0V to V_{REF}.
4	IN-	AI	Sense Analog Input Ground. To be connected to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions, it selects the interface mode of the part, Chain or $\overline{CS}$ mode, and in chain mode, it enables the busy indicator feature if SCK is high. In $\overline{CS}$ mode, it can enable the serial output signal when low. In Chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result or the programming configuration word are ouput on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: The Chain mode is selected if SDI is low during the CNV rising edge. In this Chain mode, SDI could be used as a data input to daisy chain the conversion results from two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. The $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this $\overline{CS}$ mode, either SDI or CNV can enable the serial output signals when low and if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply than the host inter face (2.5V, 3V or 5V).

NOTES
AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power

DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY ERROR (INL)

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale". The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

DIFFERENTIAL NONLINEARITY ERROR (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

GAIN ERROR

The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset has been adjusted out.

OFFSET ERROR

The first transition should occur at a level 1/2 LSB above analog ground (38.1 μV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

EFFECTIVE NUMBER OF BITS (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula:

$$ENOB = (S/[N+D]_{dB} - 1.76)/6.02)$$

and is expressed in bits.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

SIGNAL TO (NOISE + DISTORTION) RATIO (S/[N+D])

S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

APERTURE DELAY

Aperture delay is a measure of the acquisition performance and is measured from the rising edge of the CNV input to when the input signal is held for a conversion.

TRANSIENT RESPONSE

The time required for the AD7685 to achieve its rated accuracy after a full-scale step function is applied to its input.

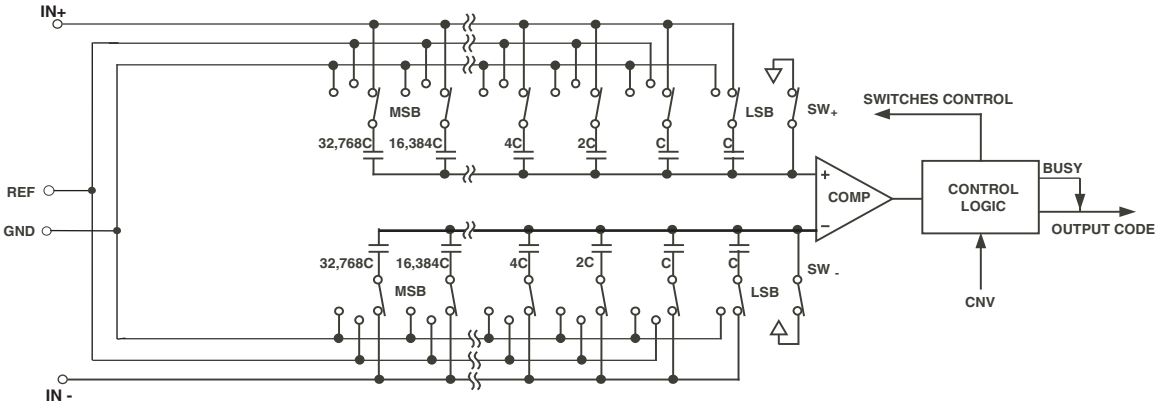


Figure 3. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7685 is a fast, low-power, single-supply, precise 16-bit analog-to-digital converter (ADC). The AD7685 is capable of converting 250,000 samples per second (250 kSPS) and allow power saving between conversions. When operating at 1kSPS, for example, it consumes typically 48 µW with a 3V supply, ideal for battery-powered applications.

The AD7685 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7685 can be operated from a single 2.7 V to 5.5V supply and be interfaced to either 5 V or 3.3 V or 2.5 V digital logic. It is housed in a 10-lead µSO package that combines space savings and allows flexible configurations. The AD7685 is pin-to-pin-compatible with the AD7686, the AD7687 and the AD7688.

The CNV rising edge is used as a sampling edge. It puts the track and hold in hold position and initiates the conversion process. Because the AD7685 has an on board conversion clock, the serial clock SCK is not required for the conversion process. When the conversion is complete and whatever the CNV state is, the part returns automatically in a power-down mode with the track and hold in track position.

CONVERTER OPERATION

The AD7685 is a successive approximation analog-to-digital converter based on a charge redistribution DAC. Figure 3 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW_+ and SW_-. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN- inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW_+ and SW_- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN- captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND or REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4 \ldots V_{REF}/65536$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and a BUSY signal indicator.

Transfer Functions

The ideal transfer characteristic for the AD7685 is shown in Figure 4 and Table I.

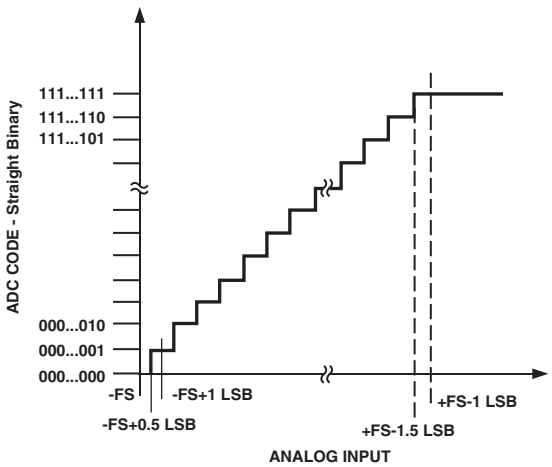


Figure 4. ADC Ideal Transfer Function

Table I. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5V	Digital Output Code Hexa
FSR –1 LSB	4.999924 V	FFFF[1]
Midscale + 1 LSB	2.500076 V	8001
Midscale	2.5 V	8000
Midscale – 1 LSB	2.499924V	7FFF
–FSR + 1 LSB	76.3µV	0001
–FSR	0 V	0000[2]

NOTES

[1]This is also the code for overrange analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{GND}).

[2]This is also the code for underrange analog input (V_{IN+} – V_{IN-} below V_{GND}).

DIGITAL INTERFACE

Though the AD7685 has a reduced number of pins, it offers flexibility in its serial interface modes:

The AD7685, used in "$\overline{CS}$ mode", is compatible to SPI, QSPI digital hosts and DSPs (e.g.:Blackfin ADSP-BF53x or ADSP-219x). This interface can use either 3 or 4 wires. Three wires interface using CNV, SCK and SDO signals, minimizes wiring connections useful, for instance, in isolated applications. Four wires interface using SDI, CNV, SCK and SDO signals allows CNV, used to initiate the conversions, to be independent of the reading timing (SDI). That is useful in, low jitter sampling or simultaneous sampling applications.

The AD7685, used in "Chain mode", provides a "daisy chain" feature using the SDI input for cascading multiple ADCs on a single data line.

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is always selected.

The AD7685 also offers the possibility, as an option and with both modes, to force a start bit in front of the 16 data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading.

The busy indicator is output or not depending on the mode as follows:
In $\overline{CS}$ mode, the busy indicator occurs if CNV or SDI is low when the ADC conversion ends.
In Chain mode, the busy indicator will be outputed if SCK is high during the CNV rising edge.

$\overline{CS}$ MODE 3 wires without Busy indicator

This mode is usually used when a single AD7685 is connected to an SPI compatible digital host. The connection diagram is shown in figure 5 and the corresponding timing is given in figure 6.
With SDI tied to OVDD, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode and forces SDO in high impedance. Once a conversion is initiated, it will be processed until completion whatever the state of CNV is. For instance, it could be useful to bring CNV low to select other SPI devices such as analog multiplexers but CNV must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7685 enters in acquisition phase and in reduced power mode. When CNV goes low, the MSB is output on SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host with acceptable hold time using the SCK falling edge will allow a faster reading rate. After the 16th SCK falling edge or when CNV goes high, whichever is the earliest, SDO returns to high impedance.

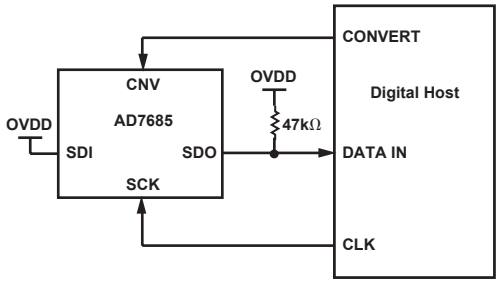


Figure 5. $\overline{CS}$ mode 3 wires without busy indicator Connection Diagram (SDI high).

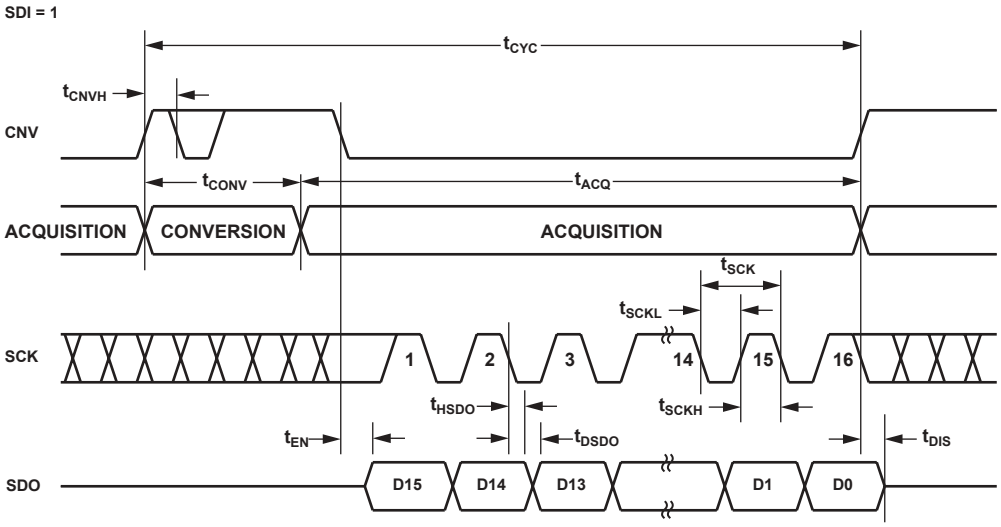


Figure 6. $\overline{CS}$ mode 3 wires without busy indicator Serial InterfaceTiming (SDI high).

$\overline{CS}$ MODE 3 wires with Busy indicator

This mode is usually used when a single AD7685 is connected to an SPI compatible digital host having an interrupt input.
The connection diagram is shown in figure 7 and the corresponding timing is given in figure 8.
With SDI tied to OVDD, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode and forces SDO in high impedance. SDO is maintained in high impedance until the completion of the conversion whatever the state of CNV is. Prior to the minimum conversion time, CNV could be used to select other SPI devices such as analog multiplexers but CNV must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on SDO line, this transition can be used as an interrupt signal to trigger the data reading controlled by the digital host. The AD7685 also enters in acquisition phase and in reduced power mode. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host with acceptable hold time using the SCK falling edge will allow a faster reading rate. After the optional 17th SCK falling edge or when CNV goes high whichever is the earliest, SDO returns to high impedance.

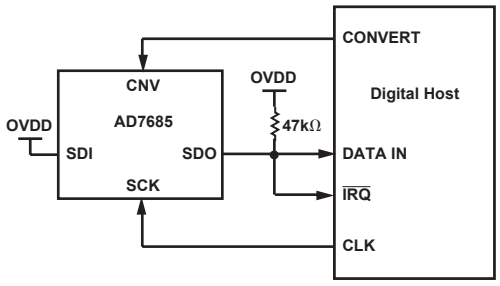


Figure 7. $\overline{CS}$ mode 3 wires with busy indicator Connection Diagram (SDI high).

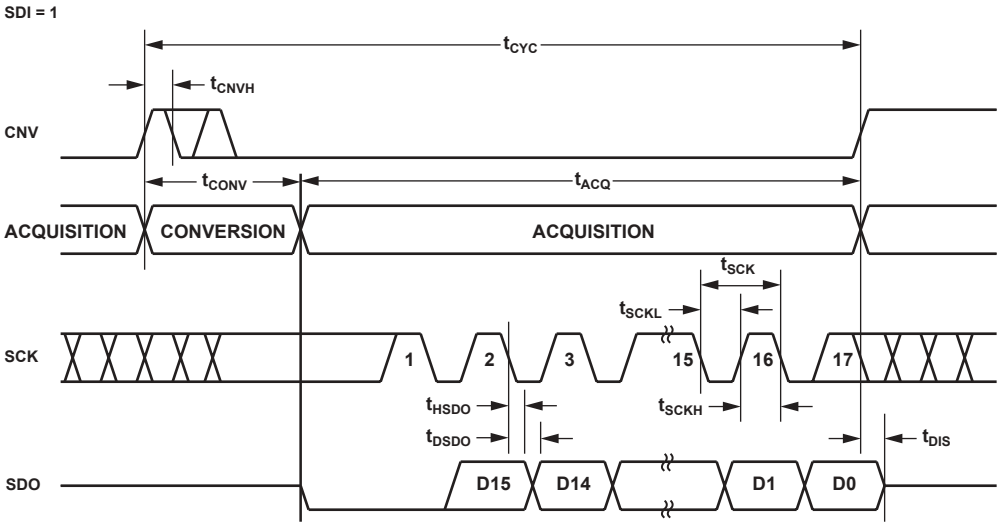


Figure 8. $\overline{CS}$ mode 3 wires with busy indicator Serial Interface Timing (SDI high).

$\overline{CS}$ MODE 4 wires without Busy indicator

This mode is usually used when multiple AD7685's are connected to an SPI compatible digital host.
A connection diagram example using two AD7685's is shown in figure 9 and the corresponding timing is given in figure 10.
With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode and forces SDO in high impedance. In this mode, CNV is held high during the conversion phase and the subsequent data reading. SDI must be high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7685 enters in acquisition phase and in reduced power mode. Each ADC result can be read by bringing low its SDI input which outputs the MSB on SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host with acceptable hold time using the SCK falling edge will allow a faster reading rate and more AD7685s on a single SPI port. After the 16th SCK falling edge or when SDI goes high whichever is the earliest, SDO returns to high impedance and another AD7685 can be read.

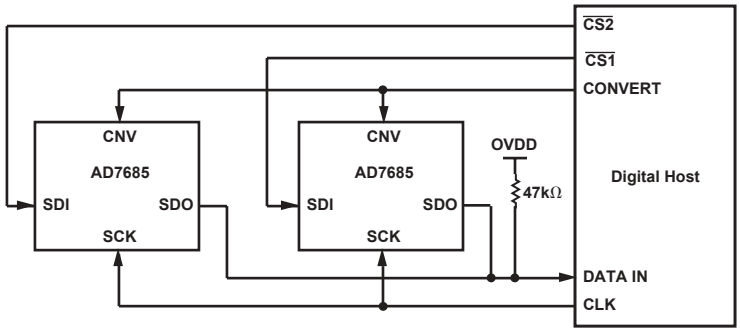


Figure 9. $\overline{CS}$ mode 4 wires without busy indicator Connection Diagram.

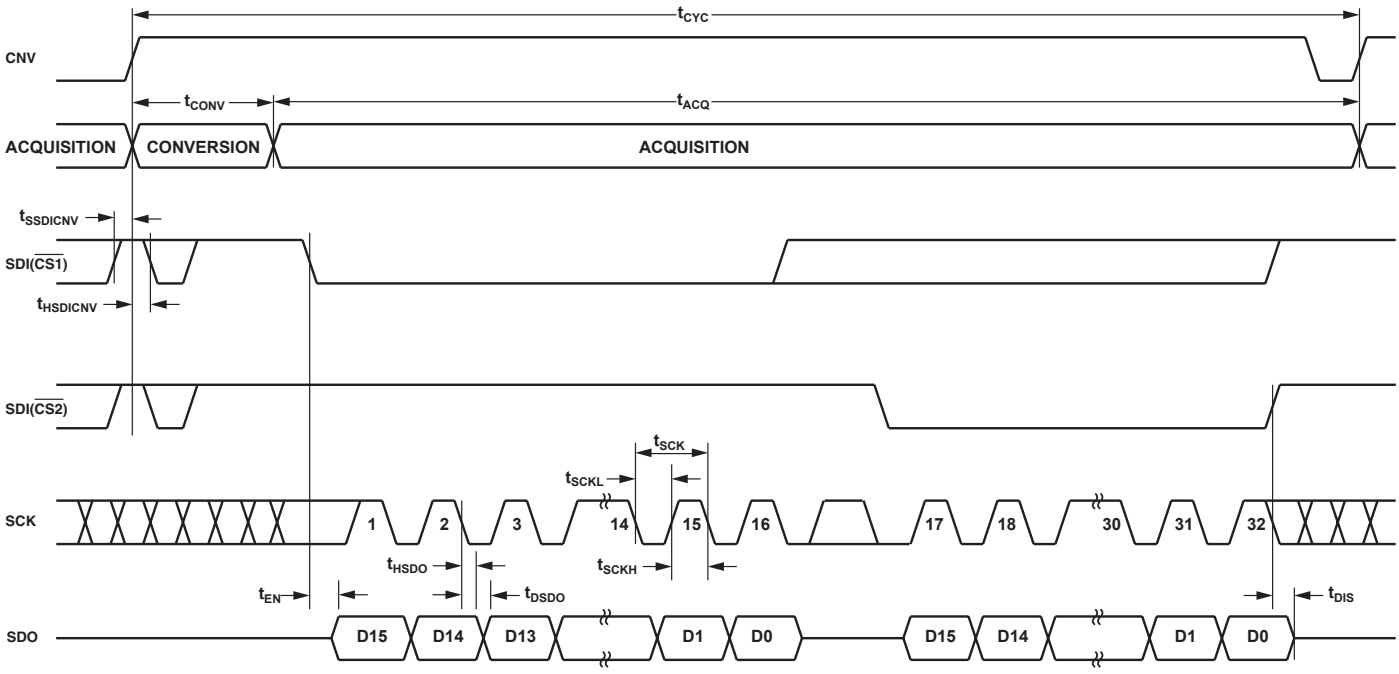


Figure 10. $\overline{CS}$ mode 4 wires without busy indicator Serial InterfaceTiming.

$\overline{CS}$ MODE 4 wires with Busy indicator

This mode is usually used when a single AD7685 is connected to an SPI compatible digital host having an interrupt input and it is desired to keep CNV, used to sample the analog input, independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in figure 11 and the corresponding timing is given in figure 12.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode and forces SDO in high impedance. In this mode, CNV is held high during the conversion phase and the subsequent data reading. Prior to the minimum conversion time, SDI could be used to select other SPI devices such as analog multiplexers but SDI must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low. With a pull-up on SDO line, this transition can be used as an interrupt signal to trigger the data reading controlled by the digital host. The AD7685 also enters in acquisition phase and in reduced power mode. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host with acceptable hold time using the SCK falling edge will allow a faster reading rate. After the 17th otional SCK falling edge or SDI goes high whichever is the earliest, the SDO returns to high impedance.

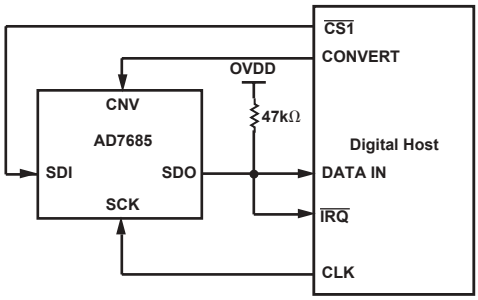


Figure 11. $\overline{CS}$ mode 4 wires with busy indicator Connection Diagram .

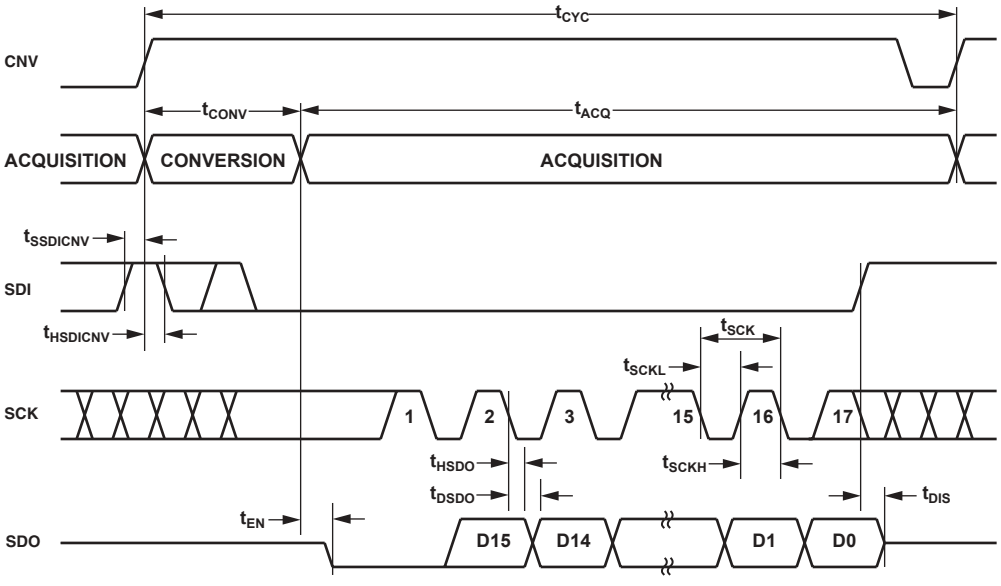


Figure 12. $\overline{CS}$ mode 4 wires with busy indicator Serial Interface Timing.

Chain MODE without Busy indicator

This mode can be used to "daisy-chain" multiple AD7685's on a single 3 wire serial interface. This feature is useful for reducing component count and wiring connections when desired as, for instance, in isolated multiconverter application or for systems with a limited capacity for interfacing to a large number of converters. A connection diagram example using two AD7685's is shown in figure 13 and the corresponding timing is given in figure 14.

With SDI tied to ground, SDO is low when CNV is low. With SCK low, a rising edge on CNV initiates a conversion, selects the Chain mode and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data reading. When the conversion is complete, the MSB is output on SDO, the AD7685 enters in acquisition phase and in reduced power mode. The remaining data bits stored in the internal output data shift register are then clocked by subsequent SCK falling edges. This internal output data shift register is also filled in on each SCK falling edge by the SDI data. By connecting SDO output of an "upstream" device to the SDI input of a "downstream" device, after the 16th SCK falling edge, the MSB of the "upstream" device is output on SDO and, consequently, the result of all devices in the chain is output serially on the SDO output of the last "downstream" device. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host with acceptable hold time using the SCK falling edge will allow a faster reading rate and more AD7685s in the chain. For instance, with a 5ns digital host set-up time and 5V interface, up to five AD7685's running at the maximum conversion rate of 250 kSPS can be "daisy-chain" to a single 3 wire port.

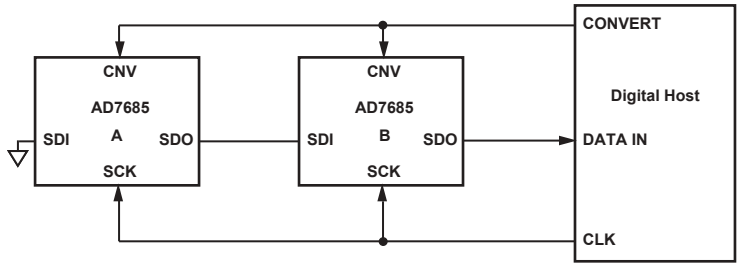


Figure 13. Chain mode without busy indicator Connection Diagram .

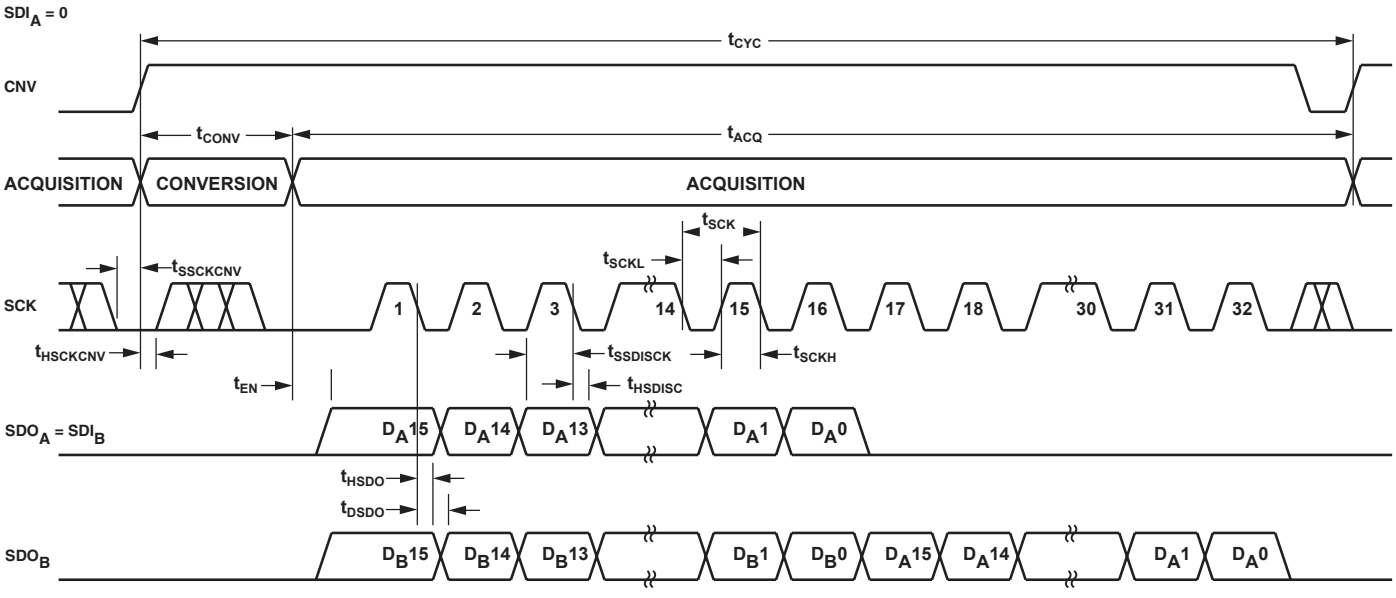


Figure 14. Chain mode without busy indicator Serial InterfaceTiming.

Chain MODE with Busy indicator

This mode can also be used to "daisy-chain" multiple AD7685's on a single 3 wire serial interface while providing a busy indicator.
A connection diagram example using three AD7685's is shown in figure 15 and the corresponding timing is given in figure 16.
With SDI and CNV tied together, SDO is low when CNV is low. With SCK high, a rising edge on CNV/SDI initiates a conversion, selects the Chain mode and enables the busy indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data reading. When the conversion is complete and SDI is high, SDO goes high, this transition on SDO can be used as an interrupt signal to trigger the data reading controlled by the digital host. The AD7685 also enters in acquisition phase and in reduced power mode. The data bits stored in the internal output data shift register are then clocked out, MSB first, by subsequent SCK falling edges. This internal output data shift register is also filled in by the SDI data on each SCK falling edge except the first one. By connecting SDO output of an "upstream" device to the SDI input of a "downstream" device, after the 17th SCK falling edge, the MSB of the "upstream" device is output on SDO and, consequently, the result of all devices in the chain is output serially on the SDO output of the last "downstream" device. Similarly, the busy indicator propagates through the chain such that SDO goes high only when all upstream devices conversions are complete. Although the rising edge can be used to capture the data, a digital host with acceptable hold time using the SCK falling edge will allow a faster reading rate and more AD7685s in the chain. For instance, with a 5ns digital host set-up time and 5V interface, up to five AD7685's running at the maximum conversion rate of 250 kSPS can be "daisy-chain" to a single 3 wire port.

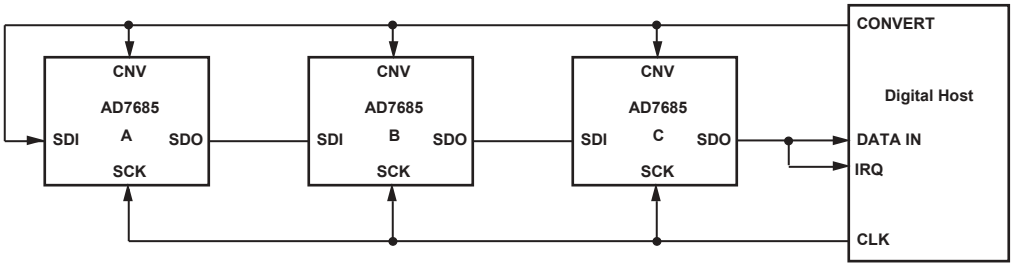


Figure 15. Chain mode with busy indicator Connection Diagram .

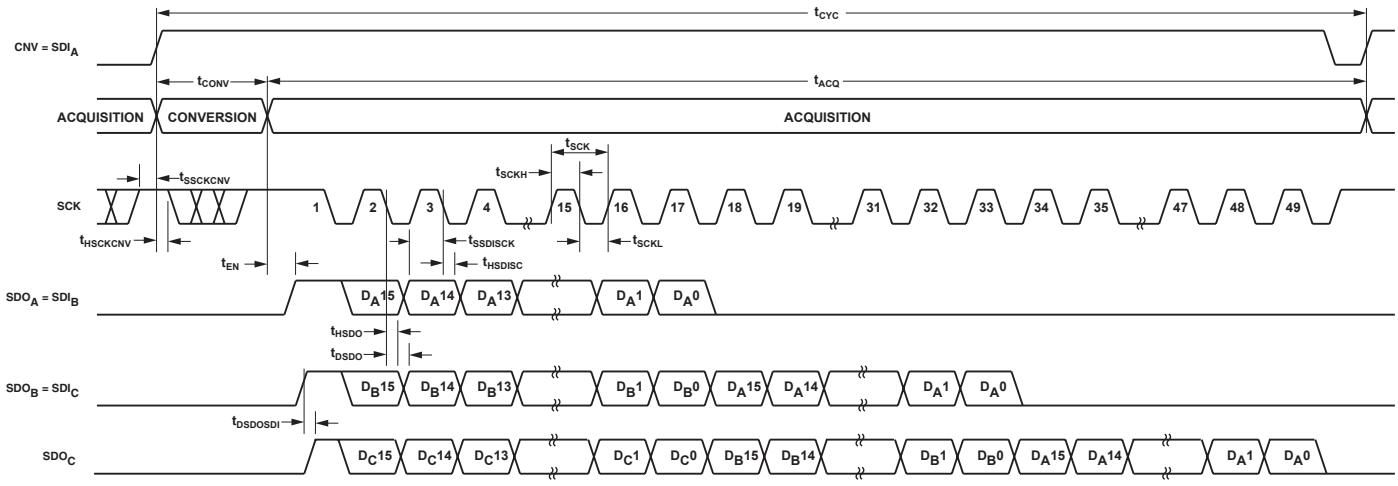


Figure 16. Chain mode with busy indicator Serial Interface Timing.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

10-Lead μSOIC
(RM-10)