Low Distortion 1.0 GHz Differential Amplifier

AD8350

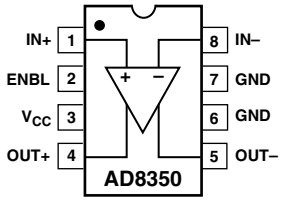
FEATURES

High Dynamic Range
Output IP3: +28 dBm: Re 50 Ω @ 250 MHz
Low Noise Figure: 5.9 dB @ 250 MHz
Two Gain Versions:
AD8350-15: 15 dB
AD8350-20: 20 dB
–3 dB Bandwidth: 1.0 GHz
Single Supply Operation: 5 V to 10 V
Supply Current: 28 mA
Input/Output Impedance: 200 Ω
Single-Ended or Differential Input Drive
8-Lead SOIC Package and 8-Lead microSOIC Package

APPLICATIONS

Cellular Base Stations
Communications Receivers
RF/IF Gain Block
Differential A-to-D Driver
SAW Filter Interface
Single-Ended-to-Differential Conversion
High Performance Video
High Speed Data Transmission

FUNCTIONAL BLOCK DIAGRAM
8-Lead SOIC and μSOIC Packages (with Enable)



PRODUCT DESCRIPTION

The AD8350 series are high performance fully-differential amplifiers useful in RF and IF circuits up to 1000 MHz. The amplifier has excellent noise figure of 5.9 dB at 250 MHz. It offers a high output third order intercept (OIP3) of +28 dBm at 250 MHz. Gain versions of 15 dB and 20 dB are offered.

The AD8350 is designed to meet the demanding performance requirements of communications transceiver applications. It enables a high dynamic range differential signal chain, with exceptional linearity and increased common-mode rejection. The device can be used as a general purpose gain block, an A-to-D driver, and high speed data interface driver, among other functions. The AD8350 input can also be used as a single-ended-to-differential converter.

The amplifier can be operated down to 5 V with an OIP3 of +28 dBm at 250 MHz and slightly reduced distortion performance. The wide bandwidth, high dynamic range and temperature stability make this product ideal for the various RF and IF frequencies required in cellular, CATV, broadband, instrumentation and other applications.

The AD8350 is offered in an 8-lead single SOIC package and μSOIC package. It operates from 5 V and 10 V power supplies, drawing 28 mA typical. The AD8350 offers a power enable function for power-sensitive applications. The AD8350 is fabricated using Analog Devices' proprietary high speed complementary bipolar process. The device is available in the industrial (–40°C to +85°C) temperature range.

REV. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703 **© Analog Devices, Inc., 2001**

AD8350—SPECIFICATIONS (@ 25°C, V_S = 5 V, G = 15 dB, unless otherwise noted. All specifications refer to differential inputs and differential outputs unless noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	V_S = 5 V, V_{OUT} = 1 V p-p		0.9		GHz
	V_S = 10 V, V_{OUT} = 1 V p-p		1.1		GHz
Bandwidth for 0.1 dB Flatness	V_S = 5 V, V_{OUT} = 1 V p-p		90		MHz
	V_S = 10 V, V_{OUT} = 1 V p-p		90		MHz
Slew Rate	V_{OUT} = 1 V p-p		2000		V/µs
Settling Time	0.1%, V_{OUT} = 1 V p-p		10		ns
Gain (S21)[1]	V_S = 5 V, f = 50 MHz	14	15	16	dB
Gain Supply Sensitivity	V_S = 5 V to 10 V, f = 50 MHz		0.003		dB/V
Gain Temperature Sensitivity	T_{MIN} to T_{MAX}		–0.002		dB/°C
Isolation (S12)[1]	f = 50 MHz		–18		dB
NOISE/HARMONIC PERFORMANCE					
50 MHz Signal					
Second Harmonic	V_S = 5 V, V_{OUT} = 1 V p-p		–66		dBc
	V_S = 10 V, V_{OUT} = 1 V p-p		–67		dBc
Third Harmonic	V_S = 5 V, V_{OUT} = 1 V p-p		–65		dBc
	V_S = 10 V, V_{OUT} = 1 V p-p		–70		dBc
Output Second Order Intercept[2]	V_S = 5 V		58		dBm
	V_S = 10 V		58		dBm
Output Third Order Intercept[2]	V_S = 5 V		28		dBm
	V_S = 10 V		29		dBm
250 MHz Signal					
Second Harmonic	V_S = 5 V, V_{OUT} = 1 V p-p		–48		dBc
	V_S = 10 V, V_{OUT} = 1 V p-p		–49		dBc
Third Harmonic	V_S = 5 V, V_{OUT} = 1 V p-p		–52		dBc
	V_S = 10 V, V_{OUT} = 1 V p-p		–61		dBc
Output Second Order Intercept[2]	V_S = 5 V		39		dBm
	V_S = 10 V		40		dBm
Output Third Order Intercept[2]	V_S = 5 V		24		dBm
	V_S = 10 V		28		dBm
1 dB Compression Point (RTI)[2]	V_S = 5 V		2		dBm
	V_S = 10 V		5		dBm
Voltage Noise (RTI)	f = 150 MHz		1.7		nV/√Hz
Noise Figure	f = 150 MHz		6.8		dB
INPUT/OUTPUT CHARACTERISTICS					
Differential Offset Voltage (RTI)	$V_{OUT+} - V_{OUT-}$		±1		mV
Differential Offset Drift	T_{MIN} to T_{MAX}		0.02		mV/°C
Input Bias Current			15		µA
Input Resistance	Real		200		Ω
CMRR	f = 50 MHz		–67		dB
Output Resistance	Real		200		Ω
POWER SUPPLY					
Operating Range		4		11.0	V
Quiescent Current	Powered Up, V_S = 5 V	25	28	32	mA
	Powered Down, V_S = 5 V	3	3.8	5.5	mA
	Powered Up, V_S = 10 V	27	30	34	mA
	Powered Down, V_S = 10 V	3	4	6.5	mA
Power-Up/Down Switching			15		ns
Power Supply Rejection Ratio	f = 50 MHz, V_S Δ = 1 V p-p		–58		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTES
[1]See Tables II–III for complete list of S-Parameters.
[2]Re: 50 Ω.

Specifications subject to change without notice.

AD8350-20–SPECIFICATIONS

(@ 25°C, V_S = 5 V, G = 20 dB, unless otherwise noted. All specifications refer to differential inputs and differential outputs unless noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	V_S = 5 V, V_{OUT} = 1 V p-p		0.7		GHz
	V_S = 10 V, V_{OUT} = 1 V p-p		0.9		GHz
Bandwidth for 0.1 dB Flatness	V_S = 5 V, V_{OUT} = 1 V p-p		90		MHz
	V_S = 10 V, V_{OUT} = 1 V p-p		90		MHz
Slew Rate	V_{OUT} = 1 V p-p		2000		V/µs
Settling Time	0.1%, V_{OUT} = 1 V p-p		15		ns
Gain (S21)[1]	V_S = 5 V, f = 50 MHz	19	20	21	dB
Gain Supply Sensitivity	V_S = 5 V to 10 V, f = 50 MHz		0.003		dB/V
Gain Temperature Sensitivity	T_{MIN} to T_{MAX}		–0.002		dB/°C
Isolation (S12)[1]	f = 50 MHz		–22		dB
NOISE/HARMONIC PERFORMANCE					
50 MHz Signal					
Second Harmonic	V_S = 5 V, V_{OUT} = 1 V p-p		–65		dBc
	V_S = 10 V, V_{OUT} = 1 V p-p		–66		dBc
Third Harmonic	V_S = 5 V, V_{OUT} = 1 V p-p		–66		dBc
	V_S = 10 V, V_{OUT} = 1 V p-p		–70		dBc
Output Second Order Intercept[2]	V_S = 5 V		56		dBm
	V_S = 10 V		56		dBm
Output Third Order Intercept[2]	V_S = 5 V		28		dBm
	V_S = 10 V		29		dBm
250 MHz Signal					
Second Harmonic	V_S = 5 V, V_{OUT} = 1 V p-p		–45		dBc
	V_S = 10 V, V_{OUT} = 1 V p-p		–46		dBc
Third Harmonic	V_S = 5 V, V_{OUT} = 1 V p-p		–55		dBc
	V_S = 10 V, V_{OUT} = 1 V p-p		–60		dBc
Output Second Order Intercept[2]	V_S = 5 V		37		dBm
	V_S = 10 V		38		dBm
Output Third Order Intercept[2]	V_S = 5 V		24		dBm
	V_S = 10 V		28		dBm
1 dB Compression Point (RTI)[2]	V_S = 5 V		–2.6		dBm
	V_S = 10 V		1.8		dBm
Voltage Noise (RTI)	f = 150 MHz		1.7		nV/√Hz
Noise Figure	f = 150 MHz		5.6		dB
INPUT/OUTPUT CHARACTERISTICS					
Differential Offset Voltage (RTI)	$V_{OUT+} - V_{OUT-}$		±1		mV
Differential Offset Drift	T_{MIN} to T_{MAX}		0.02		mV/°C
Input Bias Current			15		µA
Input Resistance	Real		200		Ω
CMRR	f = 50 MHz		–52		dB
Output Resistance	Real		200		Ω
POWER SUPPLY					
Operating Range		4		11.0	V
Quiescent Current	Powered Up, V_S = 5 V	25	28	32	mA
	Powered Down, V_S = 5 V	3	3.8	5.5	mA
	Powered Up, V_S = 10 V	27	30	34	mA
	Powered Down, V_S = 10 V	3	4	6.5	mA
Power-Up/Down Switching			15		ns
Power Supply Rejection Ratio	f = 50 MHz, V_S Δ = 1 V p-p		–45		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

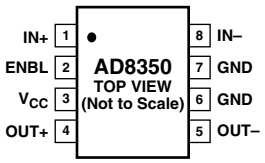
NOTES
[1]See Tables II–III for complete list of S-Parameters.
[2]Re: 50 Ω.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage, V_S . . . . . 11 V
Input Power Differential . . . . . +8 dBm
Internal Power Dissipation . . . . . 400 mW
θ_{JA} SOIC (R) . . . . . 100°C/W
θ_{JA} µSOIC (RM) . . . . . 133°C/W
Maximum Junction Temperature . . . . . 125°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Function	Description
1, 8	IN+, IN–	Differential Inputs. IN+ and IN– should be ac-coupled (pins have a dc bias of midsupply). Differential input impedance is 200 Ω.
2	ENBL	Power-up Pin. A high level (5 V) enables the device; a low level (0 V) puts device in sleep mode.
3	V_{CC}	Positive Supply Voltage. 5 V to 10 V.
4, 5	OUT+, OUT–	Differential Outputs. OUT+ and OUT– should be ac-coupled (pins have a dc bias of midsupply). Differential input impedance is 200 Ω.
6, 7	GND	Common External Ground Reference.

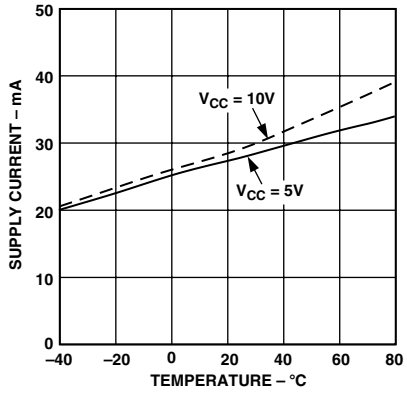
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Brand Code
AD8350AR15	–40°C to +85°C	8-Lead SOIC	SO-8	Standard
AD8350AR15-REEL	–40°C to +85°C	8-Lead SOIC 13" Reel	SO-8	Standard
AD8350AR15-REEL7	–40°C to +85°C	8-Lead SOIC 7" Reel	SO-8	Standard
AD8350ARM15	–40°C to +85°C	8-Lead microSOIC	RM-8	J2N
AD8350ARM15-REEL	–40°C to +85°C	8-Lead microSOIC 13" Reel	RM-8	J2N
AD8350ARM15-REEL7	–40°C to +85°C	8-Lead microSOIC 7" Reel	RM-8	J2N
AD8350AR20	–40°C to +85°C	8-Lead SOIC	SO-8	Standard
AD8350AR20-REEL	–40°C to +85°C	8-Lead SOIC 13" Reel	SO-8	Standard
AD8350AR20-REEL7	–40°C to +85°C	8-Lead SOIC 7" Reel	SO-8	Standard
AD8350ARM20	–40°C to +85°C	8-Lead microSOIC	RM-8	J2P
AD8350ARM20-REEL	–40°C to +85°C	8-Lead microSOIC 13" Reel	RM-8	J2P
AD8350ARM20-REEL7	–40°C to +85°C	8-Lead microSOIC 7" Reel	RM-8	J2P
AD8350-EVAL		SOIC Evaluation Board		

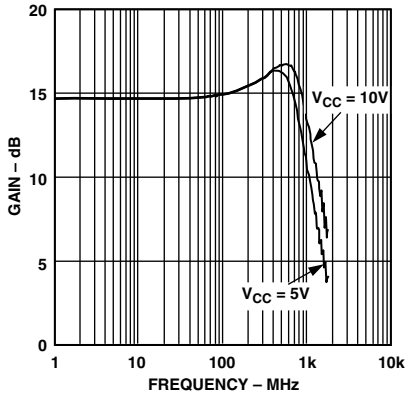
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8350 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

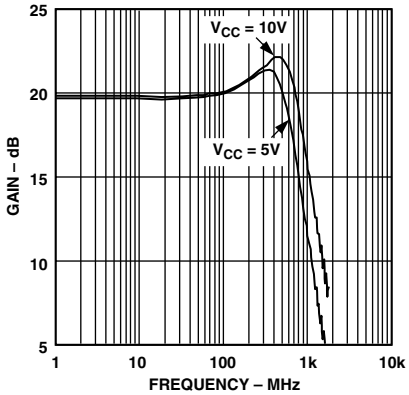
Typical Performance Characteristics–AD8350



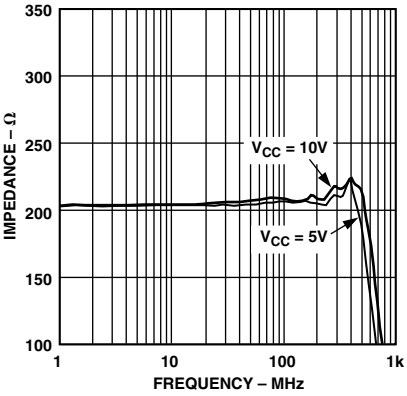
TPC 1. Supply Current vs. Temperature



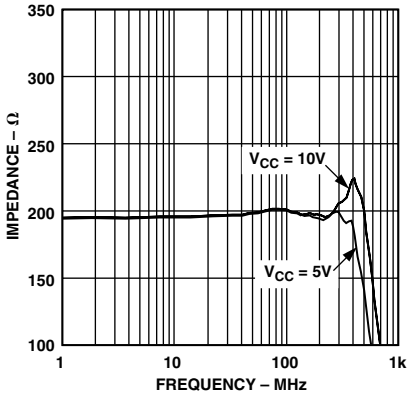
TPC 2. AD8350-15 Gain (S21) vs. Frequency



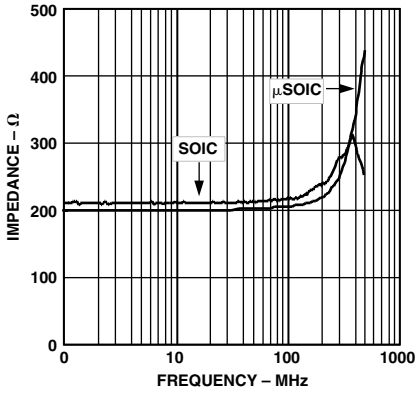
TPC 3. AD8350-20 Gain (S21) vs. Frequency



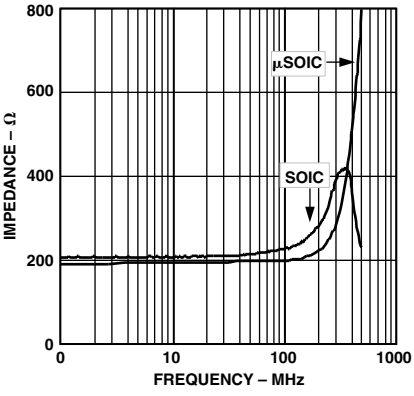
TPC 4. AD8350-15 Input Impedance vs. Frequency



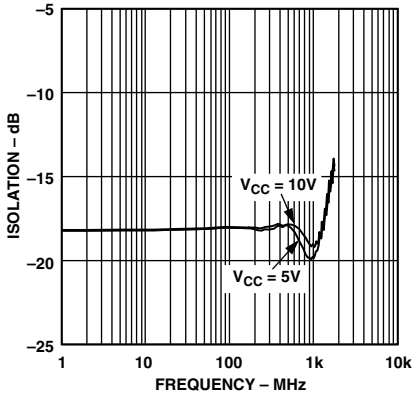
TPC 5. AD8350-20 Input Impedance vs. Frequency



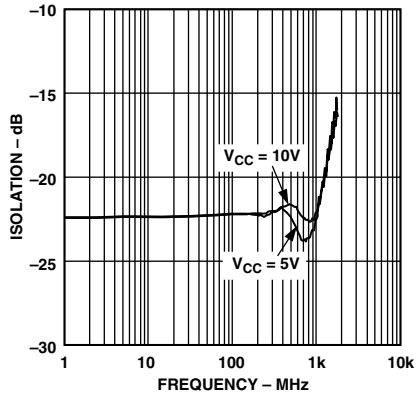
TPC 6. AD8350-15 Output Impedance vs. Frequency



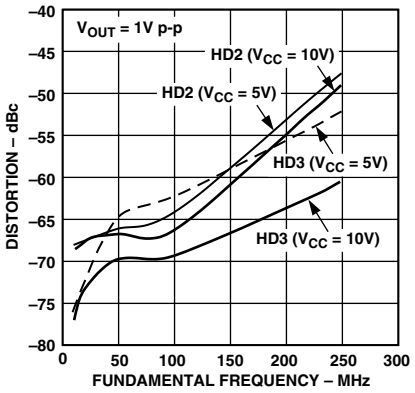
TPC 7. AD8350-20 Output Impedance vs. Frequency



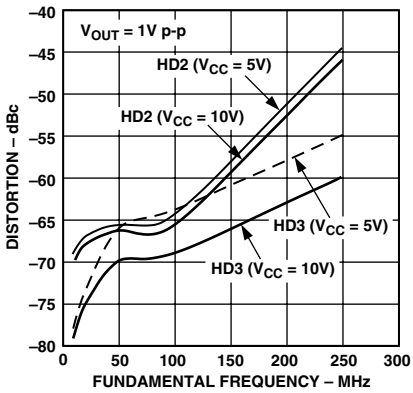
TPC 8. AD8350-15 Isolation (S12) vs. Frequency



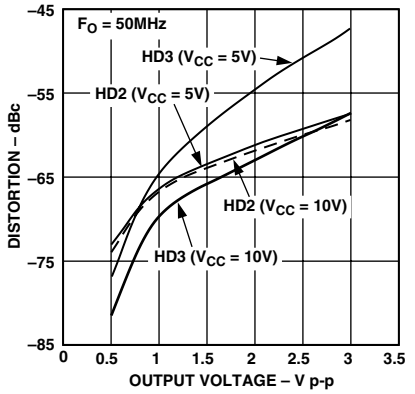
TPC 9. AD8350-20 Isolation (S12) vs. Frequency



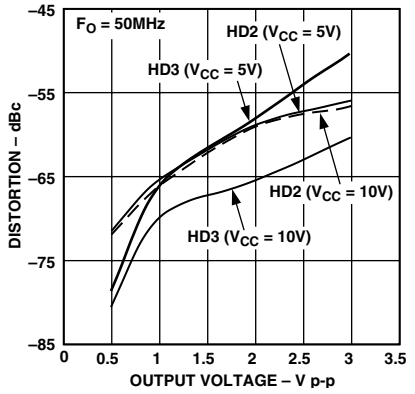
TPC 10. AD8350-15 Harmonic Distortion vs. Frequency



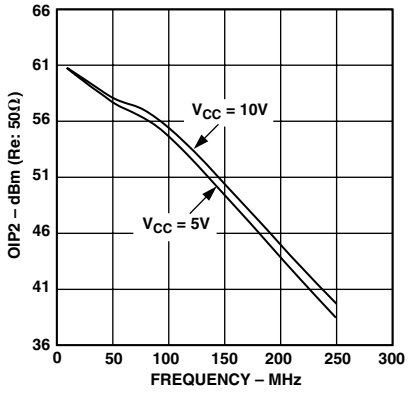
TPC 11. AD8350-20 Harmonic Distortion vs. Frequency



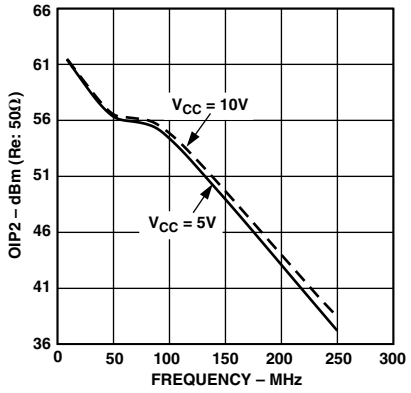
TPC 12. AD8350-15 Harmonic Distortion vs. Differential Output Voltage



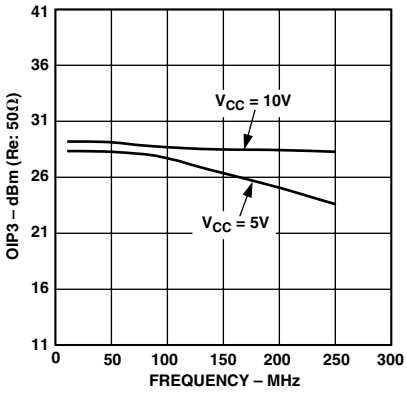
TPC 13. AD8350-20 Harmonic Distortion vs. Differential Output Voltage



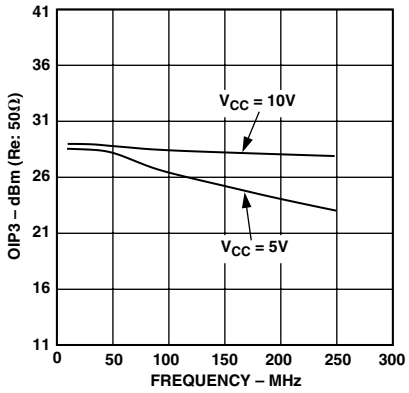
TPC 14. AD8350-15 Output Referred IP2 vs. Frequency



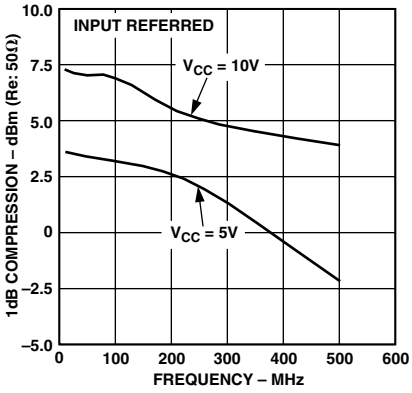
TPC 15. AD8350-20 Output Referred IP2 vs. Frequency



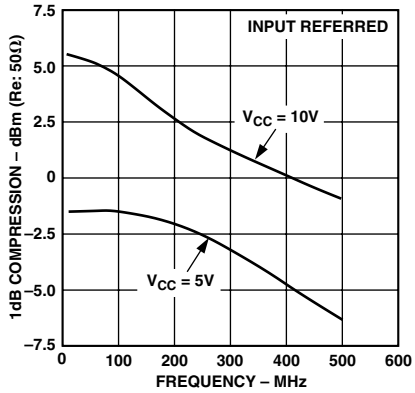
TPC 16. AD8350-15 Output Referred IP3 vs. Frequency



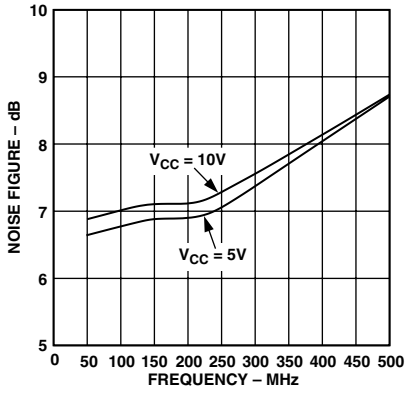
TPC 17. AD8350-20 Output Referred IP3 vs. Frequency



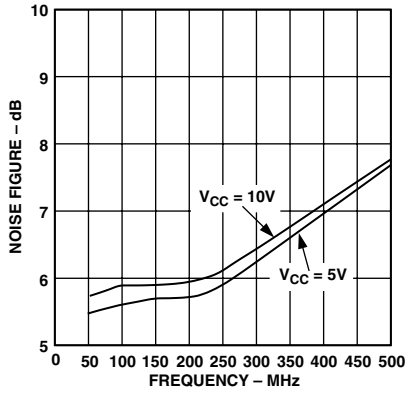
TPC 18. AD8350-15 1 dB Compression vs. Frequency



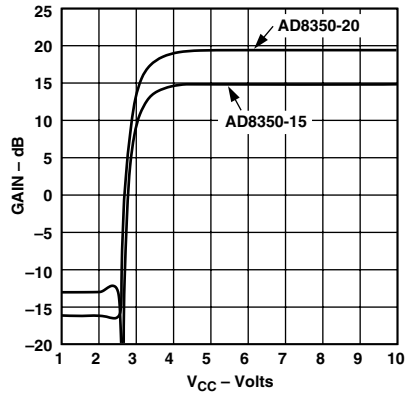
TPC 19. AD8350-20 1 dB Compression vs. Frequency



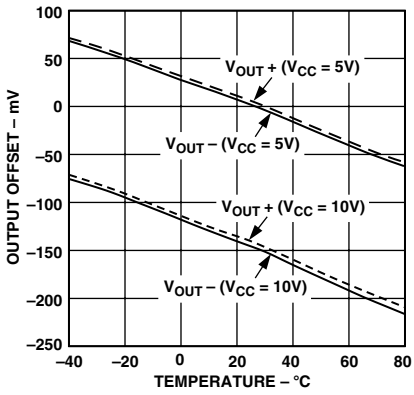
TPC 20. AD8350-15 Noise Figure vs. Frequency



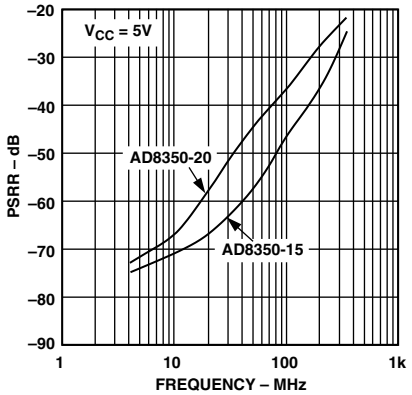
TPC 21. AD8350-20 Noise Figure vs. Frequency



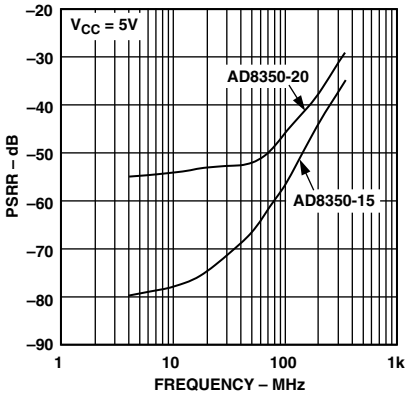
TPC 22. AD8350 Gain (S21) vs. Supply Voltage



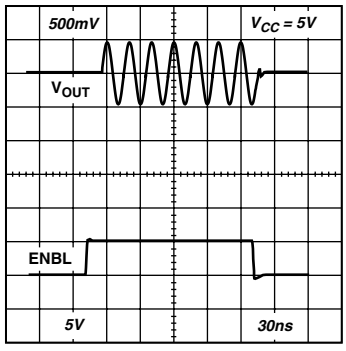
TPC 23. AD8350 Output Offset Voltage vs. Temperature



TPC 24. AD8350 PSRR vs. Frequency



TPC 25. AD8350 CMRR vs. Frequency



TPC 26. AD8350 Power-Up/Down Response Time

APPLICATIONS

Using the AD8350

Figure 1 shows the basic connections for operating the AD8350. A single supply in the range 5 V to 10 V is required. The power supply pin should be decoupled using a 0.1 μF capacitor. The ENBL pin is tied to the positive supply or to 5 V (when V_{CC} = 10 V) for normal operation and should be pulled to ground to put the device in sleep mode. Both the inputs and the outputs have dc bias levels at midsupply and should be ac-coupled.

Also shown in Figure 1 are the impedance balancing requirements, either resistive or reactive, of the input and output. With an input and output impedance of 200 Ω, the AD8350 should be driven by a 200 Ω source and loaded by a 200 Ω impedance. A reactive match can also be implemented.

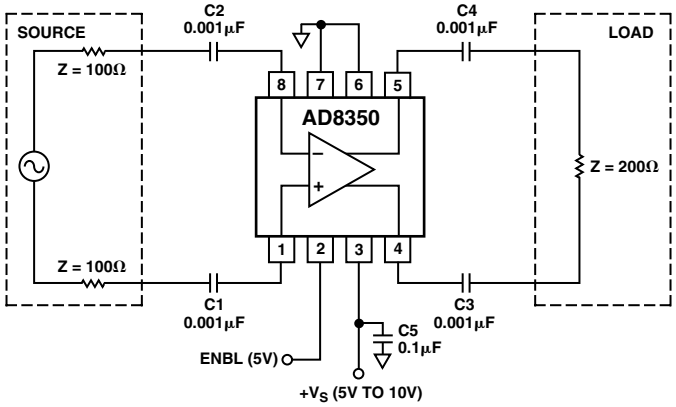


Figure 1. Basic Connections for Differential Drive

Figure 2 shows how the AD8350 can be driven by a single-ended source. The unused input should be ac-coupled to ground. When driven single-endedly, there will be a slight imbalance in the differential output voltages. This will cause an increase in the second order harmonic distortion (at 50 MHz, with V_{CC} = 10 V and V_{OUT} = 1 V p-p, –59 dBc was measured for the second harmonic on AD8350-15).

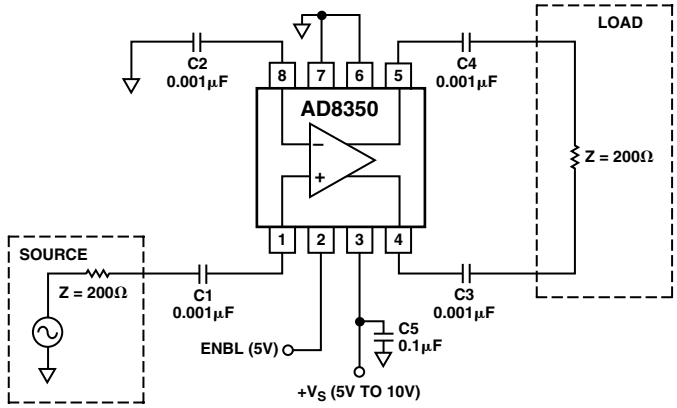


Figure 2. Basic Connections for Single-Ended Drive

Reactive Matching

In practical applications, the AD8350 will most likely be matched using reactive matching components as shown in Figure 3. Matching components can be calculated using a Smith Chart or by using a resonant approach to determine the matching network that results in a complex conjugate match. In either situation, the circuit can be analyzed as a single-ended equivalent circuit to ease calculations as shown in Figure 4.

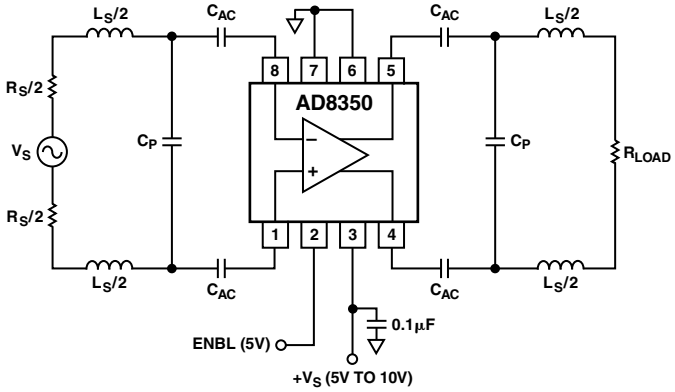


Figure 3. Reactively Matching the Input and Output

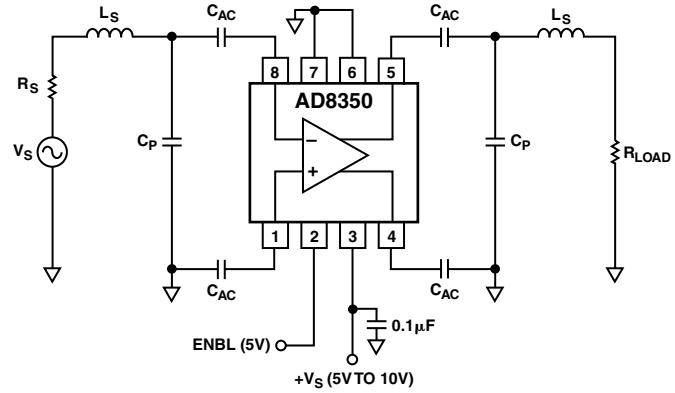


Figure 4. Single-Ended Equivalent Circuit

When the source impedance is smaller than the load impedance, a step-up matching network is required. A typical step-up network is shown on the input of the AD8350 in Figure 3. For purely resistive source and load impedances the resonant approach may be used. The input and output impedance of the AD8350 can be modeled as a real 200 Ω resistance for operating frequencies less than 100 MHz. For signal frequencies exceeding 100 MHz, classical Smith Chart matching techniques should be invoked in order to deal with the complex impedance relationships. Detailed S parameter data measured differentially in a 200 Ω system can be found in Tables II and III.

For the input matching network the source resistance is less than the input resistance of the AD8350. The AD8350 has a nominal 200 Ω input resistance from Pins 1 to 8. The reactance of the ac-coupling capacitors, C_{AC}, should be negligible if 100 nF capacitors are used and the lowest signal frequency is greater than 1 MHz. If the series reactance of the matching network inductor is defined to be $X_S = 2\pi f L_S$, and the shunt reactance of the matching capacitor to be $X_P = (2\pi f C_P)^{-1}$, then:

$$X_S = \frac{R_S \times R_{LOAD}}{X_P} \text{ where } X_P = R_{LOAD} \times \sqrt{\frac{R_S}{R_{LOAD} - R_S}} \quad (1)$$

For a 70 MHz application with a 50 Ω source resistance, and assuming the input impedance is 200 Ω, or $R_{LOAD} = R_{IN}$ = 200 Ω, then X_P = 115.5 Ω and X_S = 86.6 Ω, which results in the following component values:

$$C_P = (2\pi \times 70 \times 10^6 \times 115.5)^{-1} = 19.7\ pF \text{ and}$$

$$L_S = 86.6 \times (2\pi \times 70 \times 10^6)^{-1} = 197\ nH$$

For the output matching network, if the output source resistance of the AD8350 is greater than the terminating load resistance, a step-down network should be employed as shown on the output of Figure 3. For a step-down matching network, the series and parallel reactances are calculated as:

$$X_S = \frac{R_S \times R_{LOAD}}{X_P} \text{ where } X_P = R_S \times \sqrt{\frac{R_{LOAD}}{R_S - R_{LOAD}}} \qquad (2)$$

For a 10 MHz application with the 200 Ω output source resistance of the AD8350, R_S = 200 Ω, and a 50 Ω load termination, R_{LOAD} = 50 Ω, then X_P = 115.5 Ω and X_S = 86.6 Ω, which results in the following component values:

$$C_P = (2\pi \times 10 \times 10^6 \times 115.5)^{-1} = 138\ pF \text{ and}$$

$$L_S = 86.6 \times (2\pi \times 10 \times 10^6)^{-1} = 1.38\ \mu H$$

The same results can be obtained using the plots in Figure 5 and Figure 6. Figure 5 shows the normalized shunt reactance versus the normalized source resistance for a step-up matching network, $R_S < R_{LOAD}$. By inspection, the appropriate reactance can be found for a given value of R_S/R_{LOAD}. The series reactance is then calculated using $X_S = R_S R_{LOAD}/X_P$. The same technique can be used to design the step-down matching network using Figure 6.

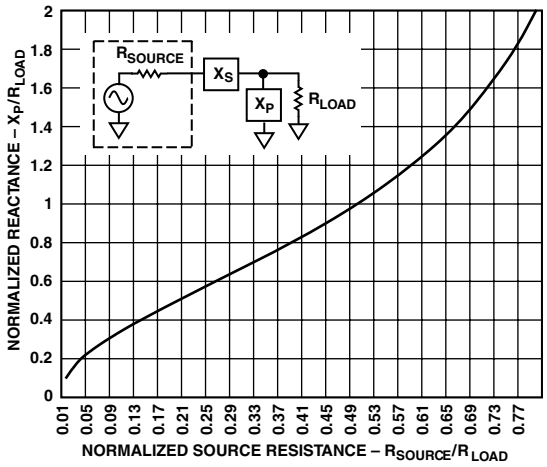


Figure 5. Normalized Step-Up Matching Components

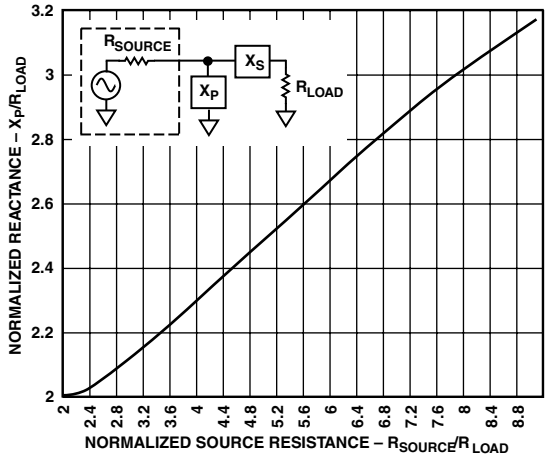


Figure 6. Normalized Step-Down Matching Components

The same results could be found using a Smith Chart as shown in Figure 7. In this example, a shunt capacitor and a series inductor are used to match the 200 Ω source to a 50 Ω load. For a frequency of 10 MHz, the same capacitor and inductor values previously found using the resonant approach will transform the 200 Ω source to match the 50 Ω load. At frequencies exceeding 100 MHz, the S parameters from Tables II and III should be used to account for the complex impedance relationships.

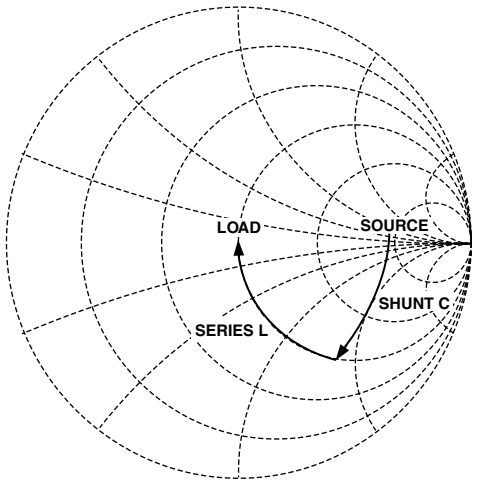


Figure 7. Smith Chart Representation of Step-Down Network

After determining the matching network for the single-ended equivalent circuit, the matching elements need to be applied in a differential manner. The series reactance needs to be split such that the final network is balanced. In the previous examples, this simply translates to splitting the series inductor into two equal halves as shown in Figure 3.

Gain Adjustment

The effective gain of the AD8350 can be reduced using a number of techniques. Obviously a matched attenuator network will reduce the effective gain, but this requires the addition of a separate component which can be prohibitive in size and cost. The attenuator will also increase the effective noise figure resulting in an SNR degradation. A simple voltage divider can be implemented using the combination of the driving impedance of the previous stage and a shunt resistor across the inputs of the AD8350 as shown in Figure 8. This provides a compact solution but suffers from an increased noise spectral density at the input of the AD8350 due to the thermal noise contribution of the shunt resistor. The input impedance can be dynamically altered through the use of feedback resistors as shown in Figure 9. This will result in a similar attenuation of the input signal by virtue of the voltage divider established from the driving source impedance and the reduced input impedance of the AD8350. Yet this technique does not significantly degrade the SNR with the unnecessary increase in thermal noise that arises from a truly resistive attenuator network.

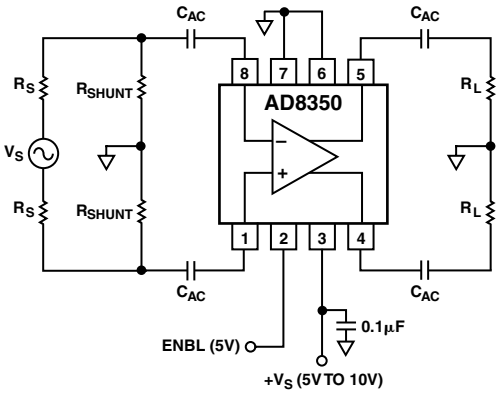


Figure 8. Gain Reduction Using Shunt Resistor

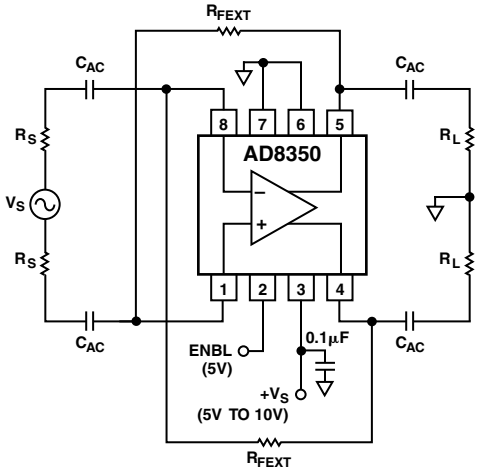


Figure 9. Dynamic Gain Reduction

Figure 8 shows a typical implementation of the shunt divider concept. The reduced input impedance that results from the parallel combination of the shunt resistor and the input impedance of the AD8350 adds attenuation to the input signal effectively reducing the gain. For frequencies less than 100 MHz, the input impedance of the AD8350 can be modeled as a real 200 Ω resistance (differential). Assuming the frequency is low enough to ignore the shunt reactance of the input, and high enough such that the reactance of moderately sized ac-coupling capacitors can be considered negligible, the insertion loss, IL, due to the shunt divider can be expressed as:

$$IL(dB) = 20 \times Log_{10}\left[\frac{\frac{R_{IN}}{(R_{IN}+R_S)}}{\frac{R_{IN}\|R_{SHUNT}}{(R_{IN}\|R_{SHUNT}+R_S)}}\right] \quad (3)$$

where

$$R_{IN}\|R_{SHUNT} = \frac{R_{IN}\times R_{SHUNT}}{R_{IN}+R_{SHUNT}} \text{ and } R_{IN} = 100\,\Omega \textit{ single-ended}$$

The insertion loss and the resultant power gain for multiple shunt resistor values is summarized in Table I. The source resistance and input impedance need careful attention when using Equation 1. The reactance of the input impedance of the AD8350 and the ac-coupling capacitors need to be considered before assuming they have negligible contribution. Figure 10 shows the effective power gain for multiple values of R_{SHUNT} for the AD8350-15 and AD8350-20.

Table I. Gain Adjustment Using Shunt Resistor, R_S = 100 Ω and R_{IN} = 100 Ω Single-Ended

R_{SHUNT}–Ω	IL–dB	Power Gain–dB AD8350-15	Power Gain–dB AD8350-20
50	6.02	8.98	13.98
100	3.52	11.48	16.48
200	1.94	13.06	18.06
300	1.34	13.66	18.66
400	1.02	13.98	18.98

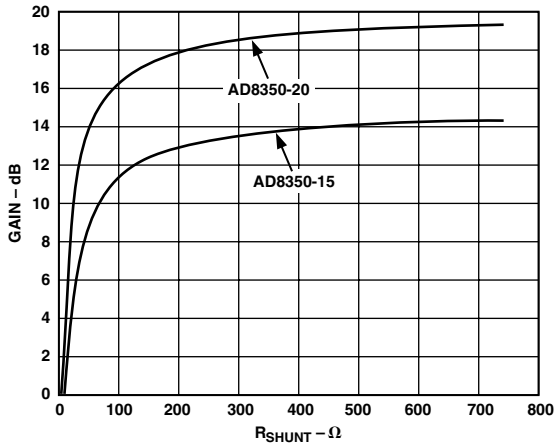


Figure 10. Gain for Multiple Values of Shunt Resistance for Circuit in Figure 8

The gain can be adjusted dynamically by employing external feedback resistors as shown in Figure 9. The effective attenuation is a result of the lowered input impedance as with the shunt resistor method, yet there is no additional noise contribution at the input of the device. It is necessary to use well-matched resistors to minimize common-mode offset errors. Quality 1% tolerance resistors should be used along with a symmetric board layout to help guarantee balanced performance. The effective gain for multiple values of external feedback resistors is shown in Figure 11.

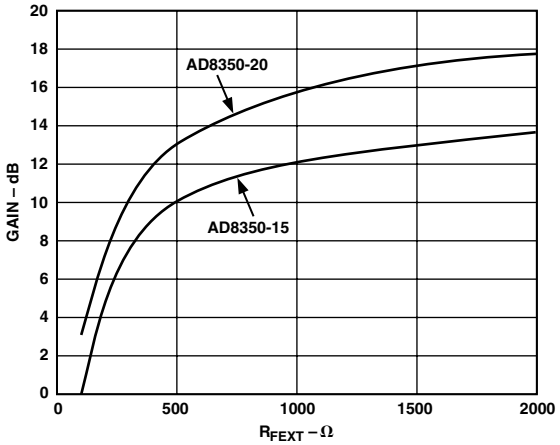


Figure 11. Power Gain vs. External Feedback Resistors for the AD8350-15 and AD8350-20 with R_S = 100 Ω and R_L = 100 Ω

The power gain of any two-port network is dependent on the source and load impedance. The effective gain will change if the differential source and load impedance is not 200 Ω. The single-ended input and output resistance of the AD8350 can be modeled using the following equations:

$$R_{IN} = \frac{R_F + R_L}{\left(\frac{R_F + R_L}{R_{INT}}\right) + 1 + g_m \times R_L} \tag{4}$$

and

$$R_{OUT} = \frac{R_F + \frac{1}{\frac{1}{R_S} + \frac{1}{R_{INT}}}}{1 + g_m \times \left(\frac{1}{\frac{1}{R_S} + \frac{1}{R_{INT}}}\right)} \approx \frac{R_F + R_S}{1 + g_m \times R_S} \text{ for } R_S \le 1\,k\Omega \tag{5}$$

where

R_F = R_{FEXT}//R_{FINT}
R_{FEXT} = R Feedback External
R_{FINT} = 662 Ω for the AD8350-15
= 1100 Ω for the AD8350-20
R_{INT} = 25000 Ω
g_m = 0.066 mhos for the AD8350-15
= 0.110 mhos for the AD8350-20
R_S = R Source (Single-Ended)
R_L = R Load (Single-Ended)
R_{IN} = R Input (Single-Ended)
R_{OUT} = R Output (Single-Ended)

The resultant single-ended gain can be calculated using the following equation:

$$G_V = \frac{R_L \times \left(g_m \times R_F - 1\right)}{R_L + R_S + R_F + R_L \times R_S \times g_m} \tag{6}$$

Driving Lighter Loads

It is not necessary to load the output of the AD8350 with a 200 Ω differential load. Often it is desirable to try to achieve a complex conjugate match between the source and load in order to minimize reflections and conserve power. But if the AD8350 is driving a voltage responding device, such as an ADC, it is no longer necessary to maximize power transfer. The harmonic distortion performance will actually improve when driving loads greater than 200 Ω. The lighter load requires less current driving capability on the output stages of the AD8350 resulting in improved linearity. Figure 12 shows the improvement in second and third harmonic distortion for increasing differential load resistance.

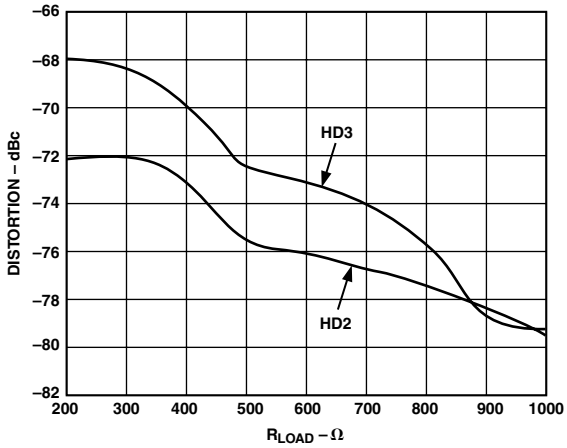


Figure 12. Second and Third Harmonic Distortion vs. Differential Load Resistance for the AD8350-15 with V_S = 5 V, f = 70 MHz, and V_{OUT} = 1 V p-p

EVALUATION BOARD

Figure 13 shows the schematic of the AD8350 evaluation board, for SOIC, as it is shipped from the factory. The board is configured to allow easy evaluation using single-ended 50 Ω test equipment. The input and output transformers have a 4-to-1 impedance ratio and transform the AD8350's 200 Ω input and output impedances to 50 Ω. In this mode, 0 Ω resistors (R1 and R4) are required.

To allow compensation for the insertion loss of the transformers, a calibration path is provided at Test In and Test Out. This consists of two transformers connected back to back.

To drive and load the board differentially, transformers T1 and T2 should be removed and replaced with four 0 Ω resistors (0805 size); Resistors R1 and R4 (0 Ω) should also be removed. This yields a circuit with a broadband input and output impedance of 200 Ω. To match to impedances other than this, matching components (0805 size) can be placed on pads C1, C2, C3, C4, L1, and L2.

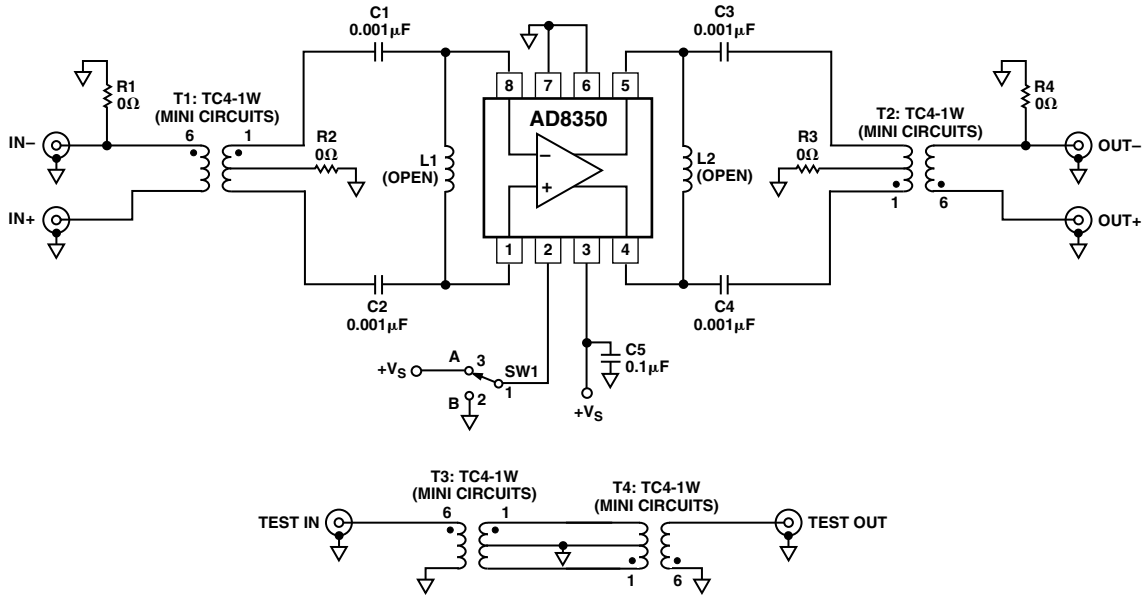


Figure 13. Evaluation Board

Table II. Typical Scattering Parameters for the AD8350-15: V_{CC} = 5 V, Differential Input and Output, Z_{SOURCE}(diff) = 200 Ω, Z_{LOAD}(diff) = 200 Ω

Frequency – MHz	S11	S12	S21	S22
25	0.015∠–48.8°	0.119∠176.3°	5.60∠–4.3°	0.034∠–4.8°
50	0.028∠–65.7°	0.119∠171.1°	5.61∠–8.9°	0.032∠–14.3°
75	0.043∠–75.3°	0.119∠166.9°	5.61∠–13.5°	0.036∠–30.2°
100	0.057∠–87.5°	0.120∠163.5°	5.61∠–17.9°	0.043∠–39.6°
125	0.073∠–91.8°	0.119∠159.8°	5.65∠–22.6°	0.053∠–40.6°
150	0.080∠–95.6°	0.120∠154.8°	5.68∠–27.0°	0.058∠–37°
175	0.100∠–97.4°	0.117∠151.2°	5.73∠–31.8°	0.072∠–45.1°
200	0.111∠–99.1°	0.121∠147.3°	5.78∠–36.3°	0.077∠–47.7°
225	0.128∠–103.2°	0.120∠143.7°	5.83∠–41.0°	0.091∠–52.5°
250	0.141∠–106.7°	0.120∠140.3°	5.90∠–45.6°	0.104∠–55.1°
275	0.151∠–109.7°	0.120∠136.6°	6.02∠–50.2°	0.108∠–54.2°
300	0.161∠–111.9°	0.123∠132.9°	6.14∠–55.1°	0.122∠–51.5°
325	0.179∠–114.7°	0.121∠130.7°	6.19∠–60.2°	0.135∠–55.6°
350	0.187∠–117.4°	0.122∠126.6°	6.27∠–65.0°	0.150∠–56.9°
375	0.194∠–121°	0.123∠123.6°	6.43∠–70.1°	0.162∠–60.9°
400	0.199∠–121.2°	0.124∠120.1°	6.61∠–75.8°	0.187∠–60.3°
425	0.215∠–122.6°	0.126∠117.2°	6.77∠–81.7°	0.215∠–63.3°
450	0.225∠–127.0°	0.126∠113.9°	6.91∠–87.6°	0.242∠–63.9°
475	0.225∠–127.7°	0.126∠112°	7.06∠–93.8°	0.268∠–65.2°
500	0.244∠–129.9°	0.128∠108.1°	7.27∠–99.8°	0.304∠–68.2°

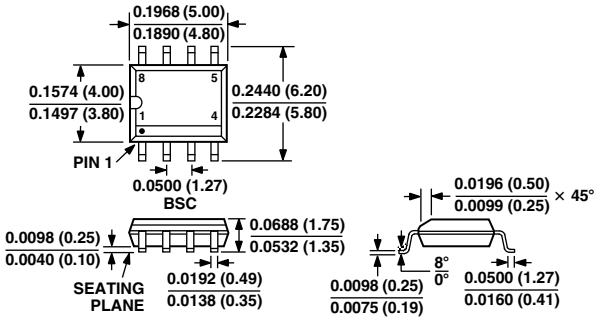
Table III. Typical Scattering Parameters for the AD8350-20: V_{CC} = 5 V, Differential Input and Output, Z_{SOURCE}(diff) = 200 Ω, Z_{LOAD}(diff) = 200 Ω

Frequency – MHz	S11	S12	S21	S22
25	0.017∠–142.9°	0.074∠174.9°	9.96∠–4.27°	0.023–16.6°
50	0.033∠–114.9°	0.074∠171.0°	9.98∠–8.9°	0.022∠–2.7°
75	0.055∠–110.6°	0.075∠167.0°	9.98∠–13.3°	0.023∠–23.5°
100	0.073∠–109.4°	0.075∠163.1°	10.00∠–17.7°	0.029∠–22.7°
125	0.089∠–112.1°	0.075∠159.2°	10.12∠–22.1°	0.037∠–18.0°
150	0.098∠–116.5°	0.076∠153.8°	10.20∠–26.4°	0.045∠–3.2°
175	0.124∠–118.1°	0.075∠150.2°	10.34∠–30.9°	0.055∠–15.7°
200	0.141∠–119.4°	0.076∠147.2°	10.50∠–35.6°	0.065∠–15.6°
225	0.159∠–122.6°	0.077∠142.2°	10.65∠–40.1°	0.080∠–17.7°
250	0.170∠–128.5°	0.078∠139.5°	10.80∠–44.7°	0.085∠–22.4°
275	0.186∠–131.6°	0.078∠135.8°	11.14∠–49.3°	0.096∠–23.5°
300	0.203∠–132.9°	0.080∠132.5°	11.45∠–54.7°	0.116∠–25.9°
325	0.215∠–135.0°	0.080∠129.3°	11.70∠–60.3°	0.139∠–29.6°
350	0.222∠–136.9°	0.082∠125.9°	11.93∠–65.0°	0.161∠–32.2°
375	0.242∠–142.4°	0.082∠123.6°	12.39∠–70.3°	0.173∠–38.6°
400	0.240∠–145.2°	0.084∠120.3°	12.99∠–76.8°	0.207∠–37.6°
425	0.267∠–146.7°	0.084∠117.3°	13.34∠–84.0°	0.241∠–48.1°
450	0.266∠–150.7°	0.086∠115.1°	13.76∠–90.1°	0.265∠–49.7°
475	0.267∠–153.7°	0.087∠112.8°	14.34∠–97.5°	0.317∠–53.5°
500	0.285∠–161.1°	0.088∠110.9°	14.89∠–105.0°	0.359∠–59.2°

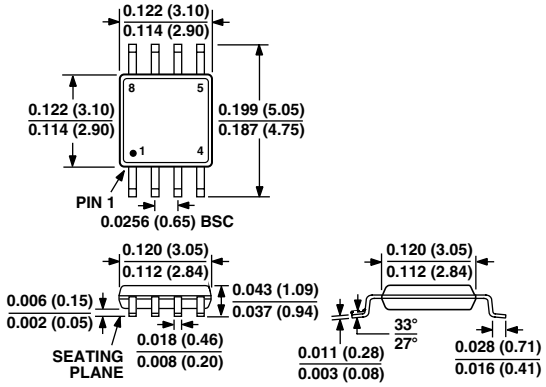
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic SOIC
(SO-8)



8-Lead microSOIC Package
(RM-8)



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