High Performance, 145 MHz *Fast FET*™ Op Amps

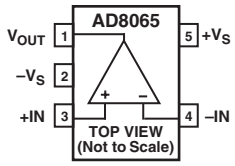
AD8065/AD8066*

FEATURES
FET Input Amplifier
1 pA Input Bias Current
Low Cost
High Speed
145 MHz, –3 dB Bandwidth (G = +1)
180 V/ms Slew Rate (G = +2)
Low Noise
7 nV/√Hz (f = 10 kHz)
0.6 fA/√Hz (f = 10 kHz)
Wide Supply Voltage Range
5 V to 24 V
Single-Supply and Rail-to-Rail Output
Low Offset Voltage 1.5 mV Max
High Common-Mode Rejection Ratio
–100 dB
Excellent Distortion Specifications
SFDR –88 dB @ 1 MHz
Low Power
6.4 mA/Amplifier Typical Supply Current
No Phase Reversal
Small Packaging
SOIC-8, SOT-23-5, and MSOP

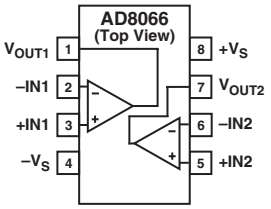
APPLICATIONS
Instrumentation
Photodiode Preamp
Filters
A/D Driver
Level Shifting
Buffering

CONNECTION DIAGRAMS

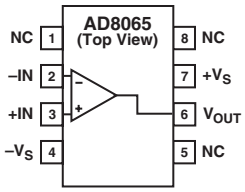
SOT-23-5 (RT)



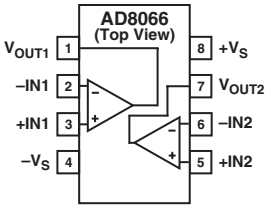
SOIC-8 (R)



SOIC-8 (R)



SOIC-8 (R) and MSOP-8 (RM)



GENERAL DESCRIPTION

The AD8065/AD8066 Fast FET amplifiers are voltage feedback amplifiers with FET inputs offering very high performance and ease of use. The AD8065 is a single amplifier and the AD8066 is a dual amplifier. The Fast FET amplifiers in ADI's proprietary XFCB process allow exceptionally low noise operation (7.0 nV/√Hz and 0.6 fA/√Hz) as well as very high input impedance.

With a wide supply voltage range from 5 V to 24 V, the ability to operate on single supplies, and a bandwidth of 145 MHz, the AD8065/AD8066 are designed to work in a variety of applications. For added versatility, the amplifiers also contain rail-to-rail outputs.

Despite being low cost, the amplifiers provide excellent overall performance. The differential gain and phase errors of 0.02% and 0.02°, respectively, along with 0.1 dB flatness out to 7 MHz, make these amplifiers ideal for video applications. Additionally, they offer a high slew rate of 180 V/µs, excellent distortion (SFDR –88 dB @ 1 MHz), extremely high common-mode rejection of –100 dB, and a low input offset voltage of 1.5 mV max under warmed up conditions. The AD8065/AD8066 operate using only a 6.4 mA/amplifier typical supply current, and are capable of delivering up to 30 mA of load current.

The AD8065/AD8066 are high performance, high speed, FET input amplifiers available in small packages: SOIC-8, MSOP, and SOT-23-5. They are rated to work over the industrial temperature range of -40°C to +85°C.

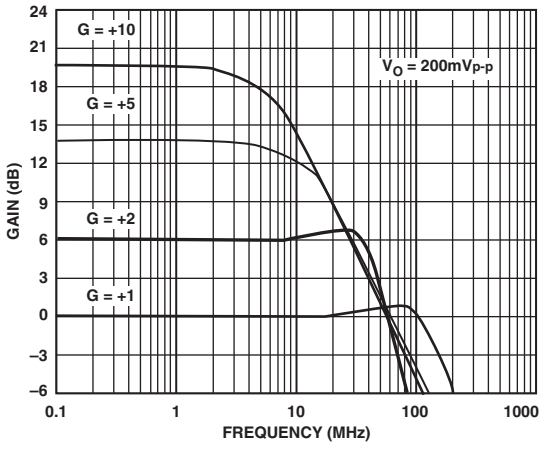


Figure 1. Small Signal Frequency Response

*Protected by U.S. Patent No. 6,262,633

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AD8065/AD8066—SPECIFICATIONS (@ T_A = 25°C, V_S = ±5 V, R_L = 1 kΩ, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.2 V p-p (AD8065)	100	145		MHz
	G = +1, V_O = 0.2 V p-p (AD8066)	100	120		MHz
	G = +2, V_O = 0.2 V p-p		50		MHz
	G = +2, V_O = 2 V p-p		42		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		7		MH
Input Overdrive Recovery Time	G = +1, –5.5 V to +5.5 V		175		ns
Output Recovery Time	G = -1, –5.5 V to +5.5 V		170		ns
Slew Rate	G = +2, V_O = 4 V Step	130	180		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		55		ns
	G = +2, V_O = 8 V Step		205		ns
NOISE/HARMONIC PERFORMANCE					
SFDR	f_C = 1 MHz, G = +2, V_O = 2 V p-p		–88		dBc
	f_C = 5 MHz, G = +2, V_O = 2 V p-p		–67		dBc
	f_C = 1 MHz, G = +2, V_O = 8 V p-p		–73		dBc
Third Order Intercept	f_C = 10 MHz, R_L = 100 Ω		24		dBm
Input Voltage Noise	f = 10 kHz		7		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz		0.6		$fA/\sqrt{Hz}$
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.02		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.02		Degree
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 0 V, SOIC Package		0.4	1.5	mV
Input Offset Voltage Drift			1	17	µV/°C
Input Bias Current	SOIC Package		2	6	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			1	10	pA
	T_{MIN} to T_{MAX}		1		pA
Open-Loop Gain	V_O = ±3 V, R_L = 1 kΩ	100	113		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000 ‖ 2.1		GΩ ‖ pF
Differential Input Impedance			1000 ‖ 4.5		GΩ ‖ pF
Input Common-Mode Voltage Range					
FET Input Range		–5 to +1.7	–5.0 to +2.4		V
Usable Range	See Theory of Operation section		–5.0 to +5.0		V
Common-Mode Rejection Ratio	V_{CM} = –1 V to +1 V	–85	–100		dB
	V_{CM} = –1 V to +1 V (SOT-23)	-82	–91		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	–4.88 to +4.90	–4.94 to +4.95		V
	R_L = 150 Ω		–4.8 to +4.7		V
Output Current	V_O = 9 V p-p,				
	SFDR ≥ –60 dBc, f = 500 kHz		35		mA
Short Circuit Current			90		mA
Capacitive Load Drive	30% Overshoot G = +1		20		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current per Amplifier			6.4	7.2	mA
Power Supply Rejection Ratio	±PSRR	–85	–100		dB

Specifications subject to change without notice.

SPECIFICATIONS (@ T_A = 25°C, V_S = ±12 V, R_L = 1 kΩ, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.2 V p-p (AD8065)	100	145		MHz
	G = +1, V_O = 0.2 V p-p (AD8066)	100	115		MHz
	G = +2, V_O = 0.2 V p-p		50		MHz
	G = +2, V_O = 2 V p-p		40		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		7		MHz
Input Overdrive Recovery	G = +1, –12.5 V to +12.5 V		175		ns
Output Overdrive Recovery	G = -1, –12.5 V to +12.5 V		170		ns
Slew Rate	G = +2, V_O = 4 V Step	130	180		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		55		ns
	G = +2, V_O = 10 V Step		250		ns
NOISE/HARMONIC PERFORMANCE					
SFDR	f_C = 1 MHz, G = +2, V_O = 2 V p-p		–100		dBc
	f_C = 5 MHz, G = +2, V_O = 2 V p-p		–67		dBc
	f_C = 1 MHz, G = +2, V_O = 10 V p-p		–85		dBc
Third Order Intercept	f_C = 10 MHz, R_L = 100 Ω		24		dBm
Input Voltage Noise	f = 10 kHz		7		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz		1		$fA/\sqrt{Hz}$
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.04		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.03		Degree
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 0 V, SOIC Package		0.4	1.5	mV
Input Offset Voltage Drift			1	17	µV/°C
Input Bias Current	SOIC Package		3	7	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			2	10	pA
	T_{MIN} to T_{MAX}		2		pA
Open-Loop Gain	V_O = ±10 V, R_L = 1 kΩ	103	114		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000 ‖ 2.1		GΩ ‖ pF
Differential Input Impedance			1000 ‖ 4.5		GΩ ‖ pF
Input Common-Mode Voltage Range					
FET Input Range		–12 to +8.5	–12.0 to +9.5		V
Usable Range	See Theory of Operation section		–12.0 to +12.0		V
Common-Mode Rejection Ratio	V_{CM} = –1 V to +1 V	–85	–100		dB
	V_{CM} = –1 V to +1 V (SOT-23)	–82	–91		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	–11.8 to +11.8	–11.9 to +11.9		V
	R_L = 350 Ω		–11.25 to +11.5		V
Output Current	V_O = 22 V p-p,				
	SFDR ≥ –60 dBc, f = 500 kHz		30		mA
Short Circuit Current			120		mA
Capacitive Load Drive	30% Overshoot G = +1		25		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current per Amplifier			6.6	7.4	mA
Power Supply Rejection Ratio	±PSRR	–84	–93		dB

Specifications subject to change without notice.

AD8065/AD8066 SPECIFICATIONS (continued) (@ T_A = 25°C, V_S = 5 V, R_L = 1 kΩ, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.2 V p-p (AD8065)	125	155		MHz
	G = +1, V_O = 0.2 V p-p (AD8066)	110	130		MHz
	G = +2, V_O = 0.2 V p-p		50		MHz
	G = +2, V_O = 2 V p-p		43		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		6		MHz
Input Overdrive Recovery Time	G = +1, –0.5 V to +5.5 V		175		ns
Output Recovery Time	G = –1, –0.5 V to +5.5 V		170		ns
Slew Rate	G = +2, V_O = 2 V Step	105	160		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		60		ns
NOISE/HARMONIC PERFORMANCE					
SFDR	f_C = 1 MHz, G = +2, VO = 2 V p-p		–65		dBc
	f_C = 5 MHz, G = +2, VO = 2 V p-p		–50		dBc
Third Order Intercept	f_C = 10 MHz, R_L = 100Ω		22		dBm
Input Voltage Noise	f = 10 kHz		7		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz		0.6		$fA/\sqrt{Hz}$
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.13		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.16		Degree
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 1.0 V, SOIC Package		0.4	1.5	mV
Input Offset Voltage Drift			1	17	µV/°C
Input Bias Current	SOIC Package		1	5	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			1	5	pA
	T_{MIN} to T_{MAX}		1		pA
Open-Loop Gain	V_O = 1 V to 4 V (AD8065)	100	113		dB
	V_O = 1 V to 4 V (AD8066)	90	103		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000 ‖ 2.1		GΩ ‖ pF
Differential Input Impedance			1000 ‖ 4.5		GΩ ‖ pF
Input Common-Mode Voltage Range					
FET Input Range		0 to 1.7	0 to 2.4		V
Usable Range	See Theory of Operation section		0 to 5.0		V
Common-Mode Rejection Ratio	V_{CM} = 1 V to 4 V	–74	–100		dB
	V_{CM} = 1 V to 2 V (SOT-23)	–78	–91		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	0.1 to 4.85	0.03 to 4.95		V
	R_L = 150 Ω		0.07 to 4.83		V
Output Current	V_O = 4 V p-p,				
	SFDR ≥ –60 dBc, f = 500 kHz		35		mA
Short Circuit Current			75		mA
Capacitive Load Drive	30% Overshoot G = +1		5		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current per Amplifier		5.8	6.4	7.0	mA
Power Supply Rejection Ratio	±PSRR	–78	–100		dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 26.4 V
Power Dissipation . . . . . See Figure 2
Common-Mode Input Voltage . . . . . V_{EE} – 0.5 V to VCC + 0.5 V
Differential Input Voltage . . . . . 1.8 V
Storage Temperature . . . . . –65°C to +125°C
Operating Temperature Range . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8065/AD8066 packages is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die will locally reach the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic will change its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8065 AD8066. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as follows:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, then the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = quiescent\ power + \left(total\ drive\ power - load\ power\right)$$

$$P_D = \left(V_S \times I_S\right) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to V_S-, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, then consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = \left(V_S \times I_S\right) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to V_S-, worst case is $V_{OUT} = V_S/2$.

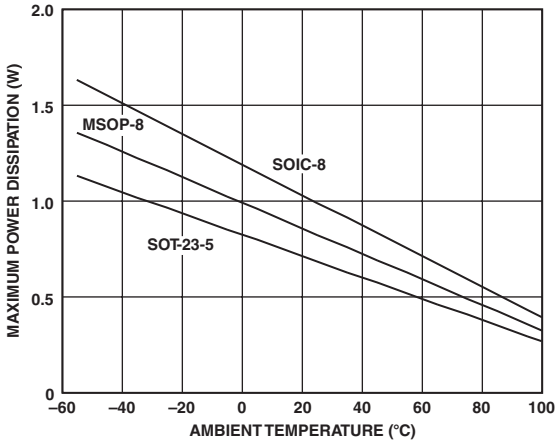


Figure 2. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

Airflow will increase heat dissipation effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes will reduce the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps as discussed in the Layout, Grounding, and Bypass Considerations section.

Figure 2 shows the maximum safe power dissipation in the package versus the ambient temperature for the SOIC-8 (125°C/W), SOT-23-5 (180°C/W), and MSOP-8 (150°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current for the AD8065/AD8066 will likely cause catastrophic failure.

ORDERING GUIDE

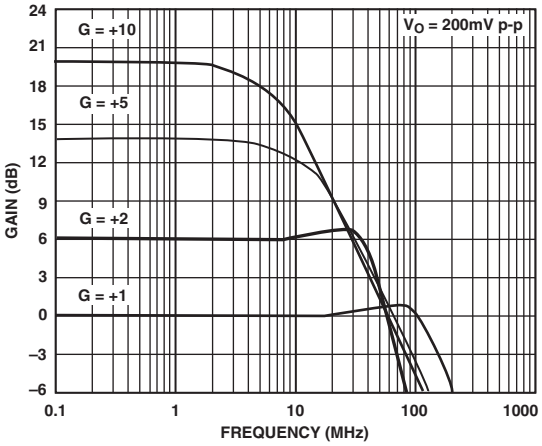
Model	Temperature Range	Package Description	Package Outline	Branding Information
AD8065AR	–40°C to +85°C	8-Lead SOIC	R-8	
AD8065AR-REEL	–40°C to +85°C	8-Lead SOIC	R-8	
AD8065AR-REEL7	–40°C to +85°C	8-Lead SOIC	R-8	
AD8065ART-REEL	–40°C to +85°C	8-Lead SOIC SOT-23	RT-5	HRA
AD8065ART-REEL7	–40°C to +85°C	8-Lead SOIC SOT-23	RT-5	HRA
AD8065AR	–40°C to +85°C	8-Lead SOIC	R-8	
AD8066AR-REEL	–40°C to +85°C	8-Lead SOIC	R-8	
AD8066AR-REEL7	–40°C to +85°C	8-Lead SOIC	R-8	
AD8066ARM-REEL	–40°C to +85°C	8-Lead SOIC MSOP-8	RM-8	H1B
AD8066ARM-REEL7	–40°C to +85°C	8-Lead SOIC MSOP-8	RM-8	H1B

CAUTION

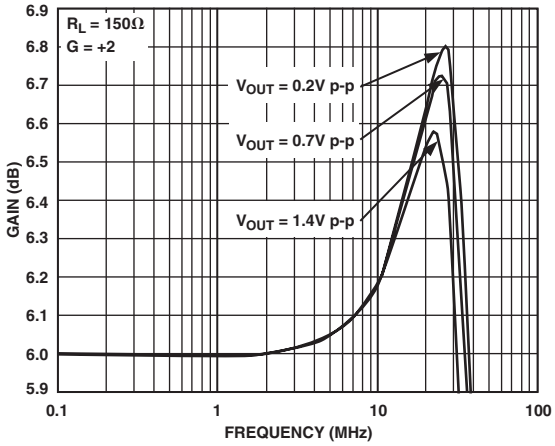
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8065/AD8066 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD8065/AD8066–Typical Performance Characteristics

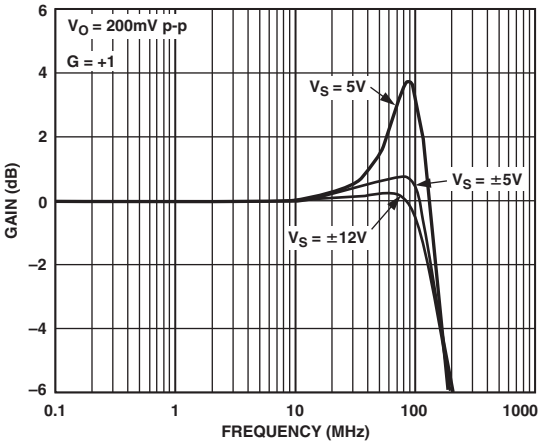
(Default Conditions: ±5 V, C_L = 5 pF, R_L = 1kΩ, V_{OUT} = 2 V p-p, Temperature = 25°C)



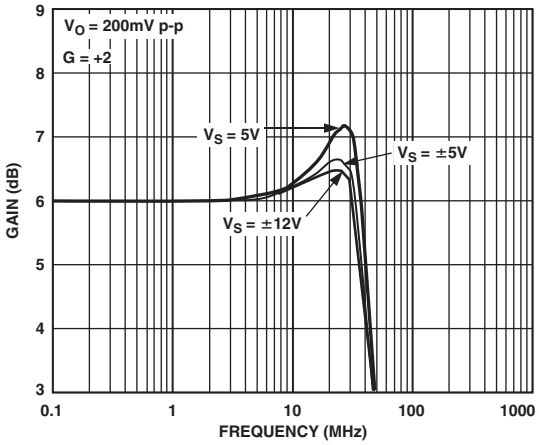
TPC 1. Small Signal Frequency Response for Various Gains



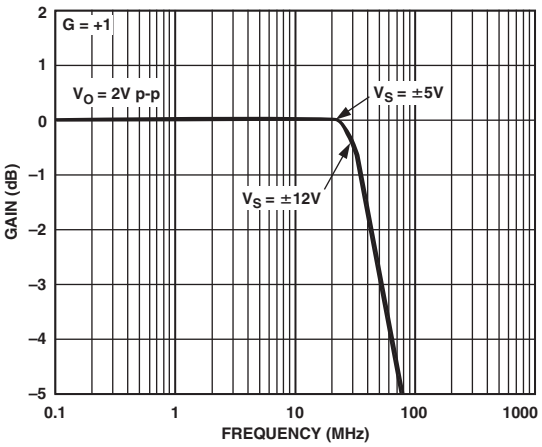
TPC 4. 0.1 dB Flatness Frequency Response (See Test Circuit 2)



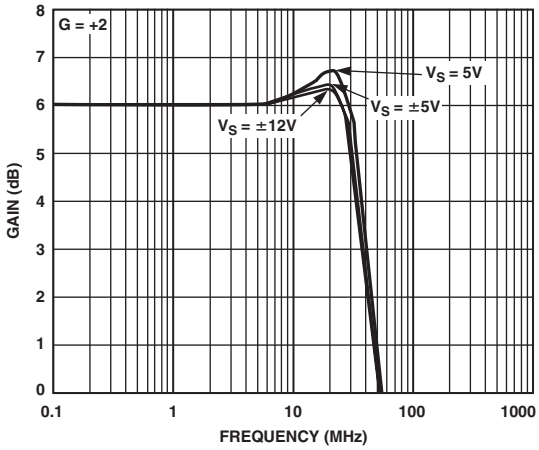
TPC 2. Small Signal Frequency Response for Various Supplies (See Test Circuit 1)



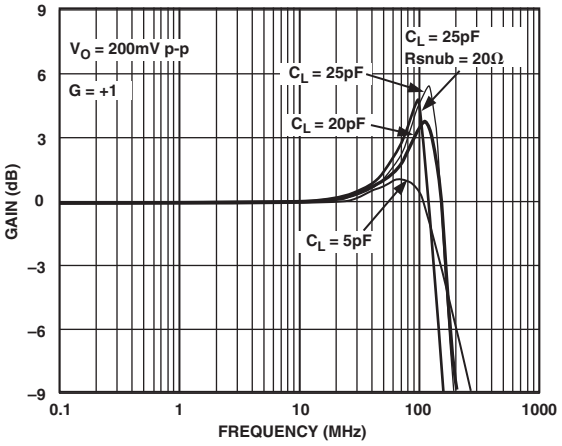
TPC 5. Small Signal Frequency Response for Various Supplies (See Test Circuit 2)



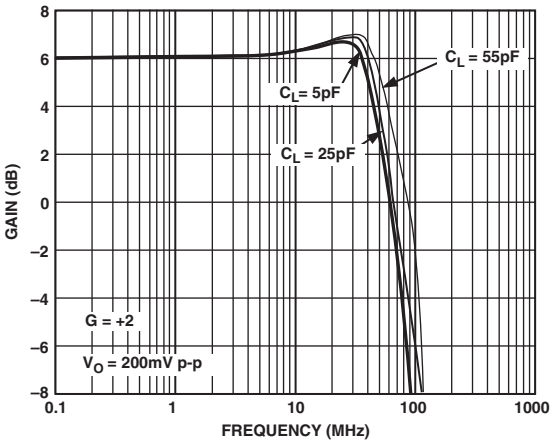
TPC 3. Large Signal Frequency Response for Various Supplies (See Test Circuit 1)



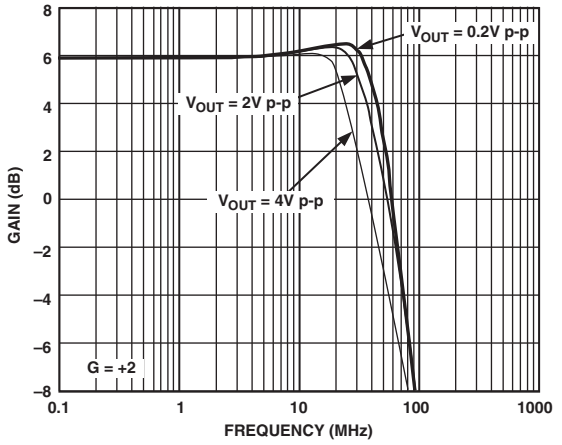
TPC 6. Large Signal Frequency Response for Various Supplies (See Test Circuit 2)



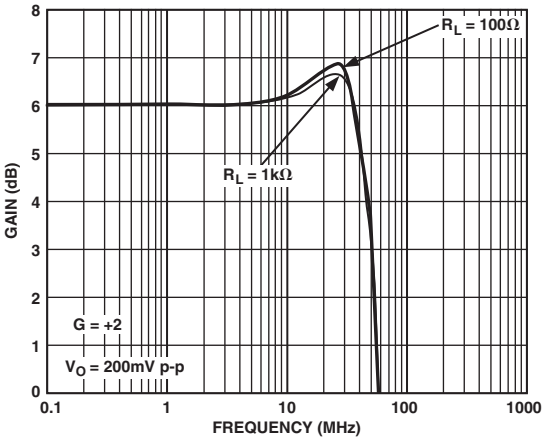
TPC 7. Small Signal Frequency Response for Various C_{LOAD} (See Test Circuit 1)



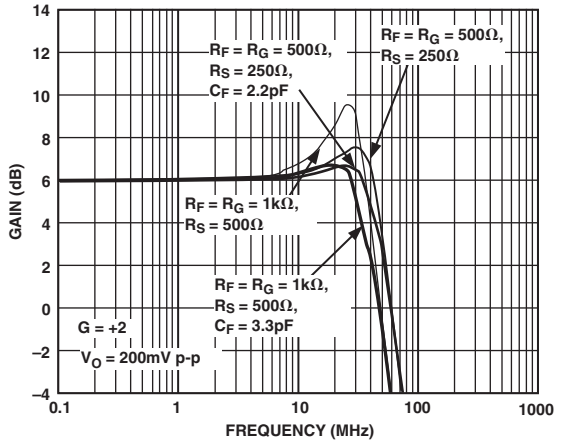
TPC 10. Small Signal Frequency Response for Various C_{LOAD} (See Test Circuit 2)



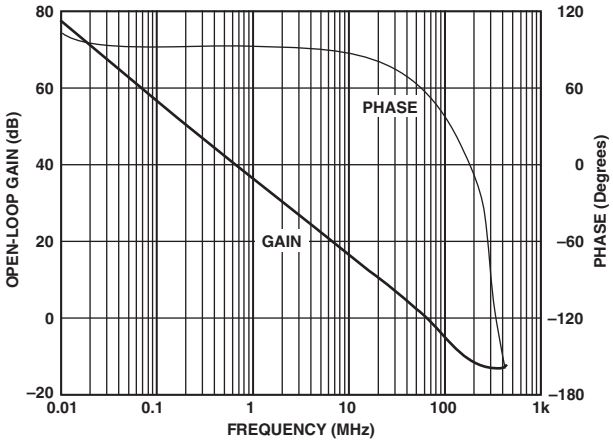
TPC 8. Frequency Response for Various Output Amplitudes (See Test Circuit 2)



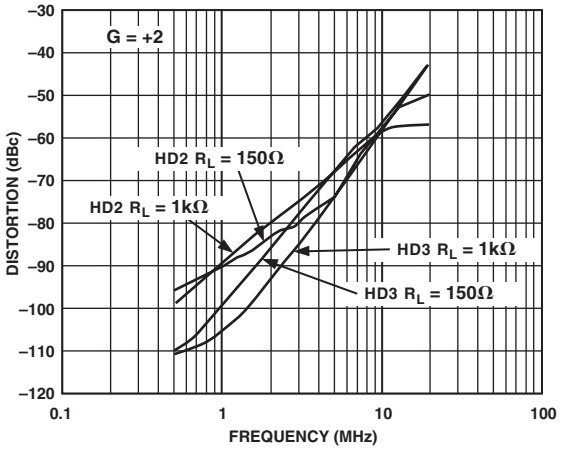
TPC 11. Small Signal Frequency Response for Various R_{LOAD} (See Test Circuit 2)



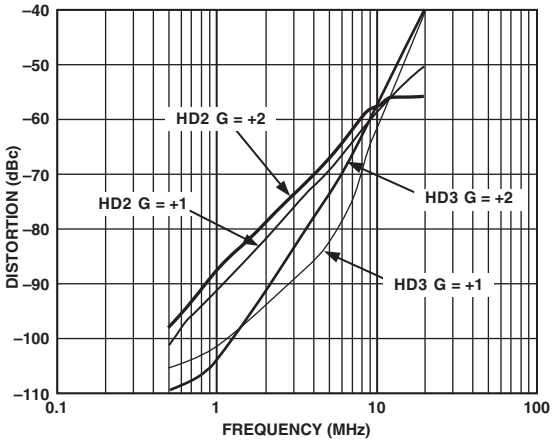
TPC 9. Small Signal Frequency Response for Various R_F/C_F (See Test Circuit 2)



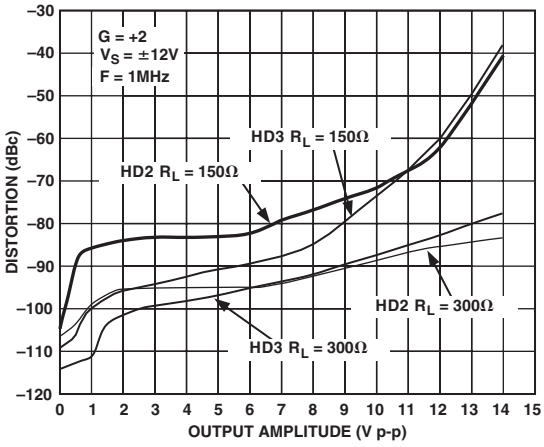
TPC 12. Open-Loop Response



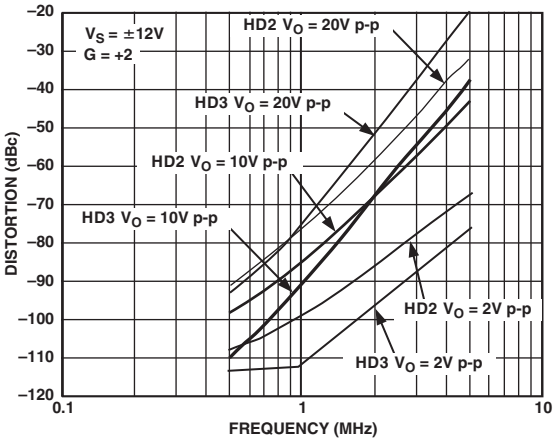
TPC 13. Harmonic Distortion vs. Frequency for Various Loads (See Test Circuit 2)



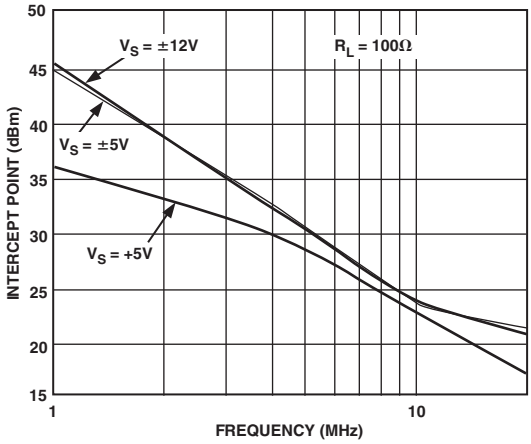
TPC 16. Harmonic Distortion vs. Frequency for Various Gains (See Test Circuits 1 and 2)



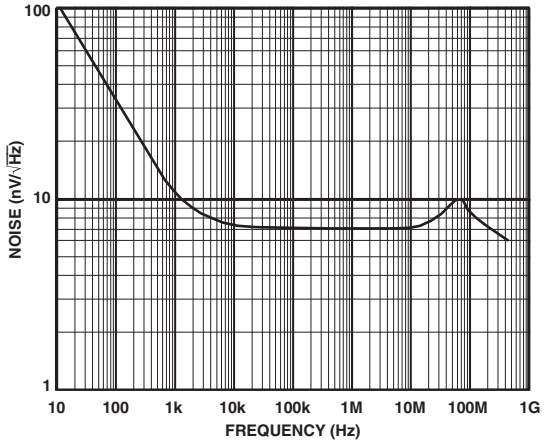
TPC 14. Harmonic Distortion vs. Amplitude for Various Loads VS = ±12 V (See Test Circuit 2)



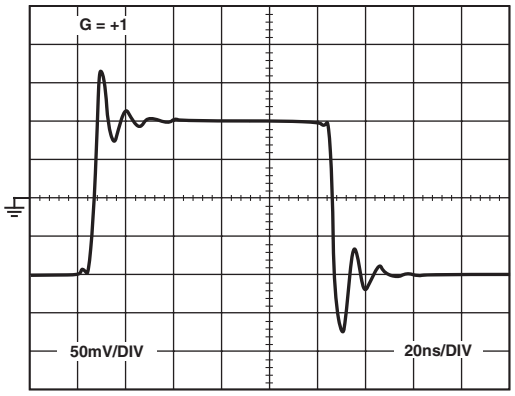
TPC 17. Harmonic Distortion vs. Frequency for Various Amplitudes (See Test Circuit 2)



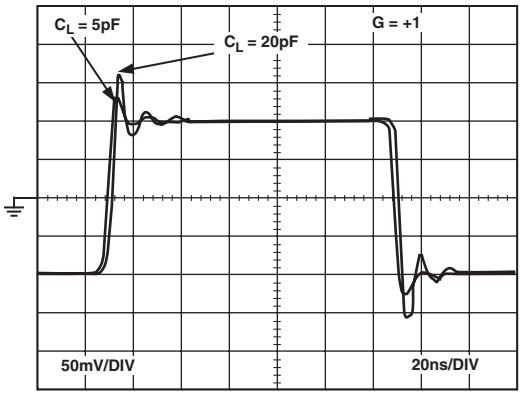
TPC 15. Third Order Intercept vs. Frequency and Supply Voltage



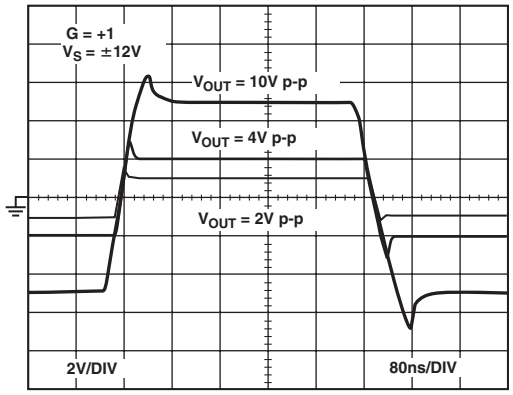
TPC 18. Voltage Noise



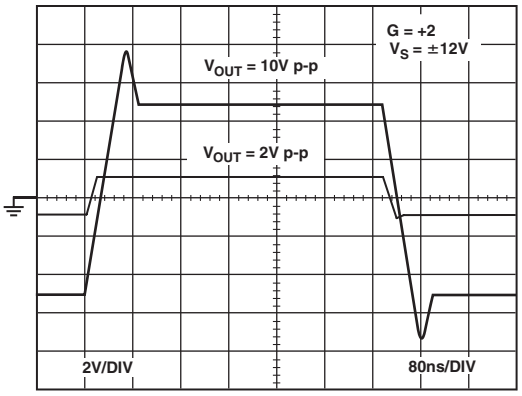
TPC 19. Small Signal Transient Response 5 V Supply (See Test Circuit 11)



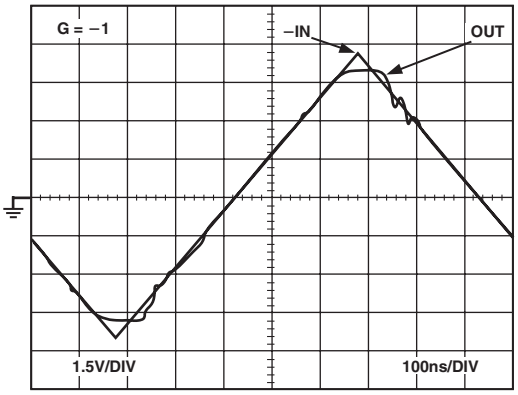
TPC 22. Small Signal Transient Response ±5 V (See Test Circuit 1)



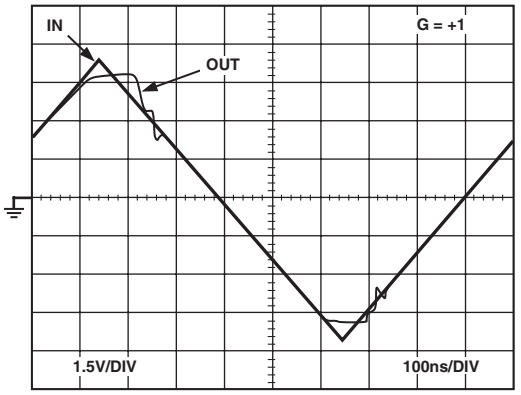
TPC 20. Large Signal Transient Response (See Test Circuit 1)



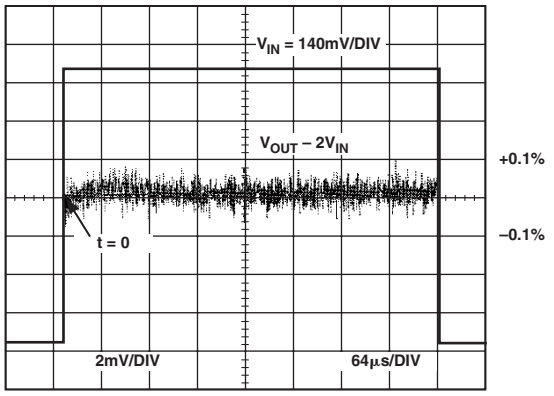
TPC 23. Large Signal Transient Response (See Test Circuit 2)



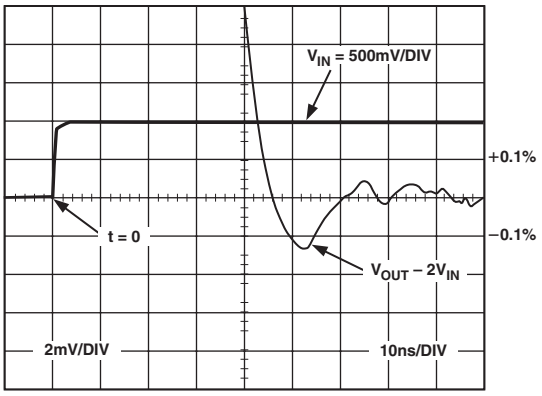
TPC 21. Output Overdrive Recovery (See Test Circuit 3), V_S = ±5 V



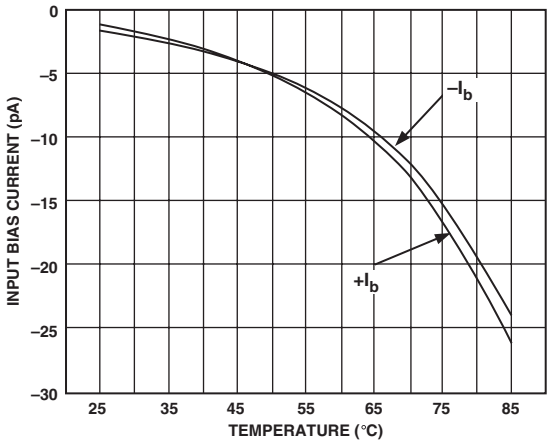
TPC 24. Input Overdrive Recovery (See Test Circuit 1), V_S = ±5 V



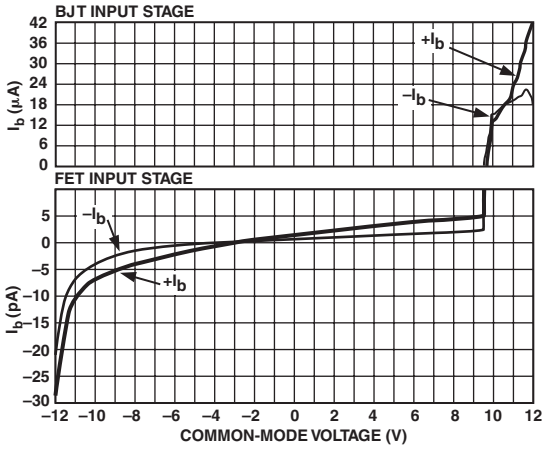
TPC 25. Long-Term Settling Time (See Test Circuit 8)



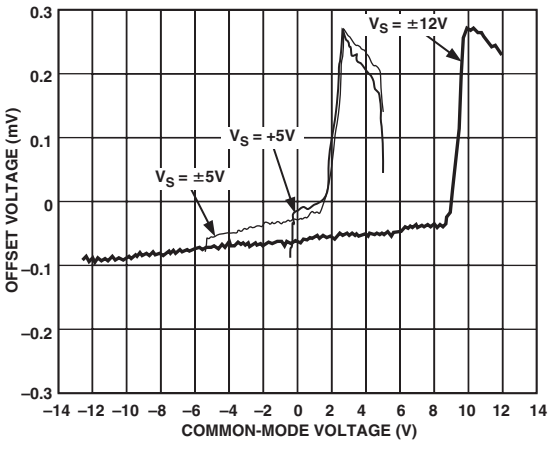
TPC 28. 0.1% Short-Term Settling Time (See Test Circuit 8)



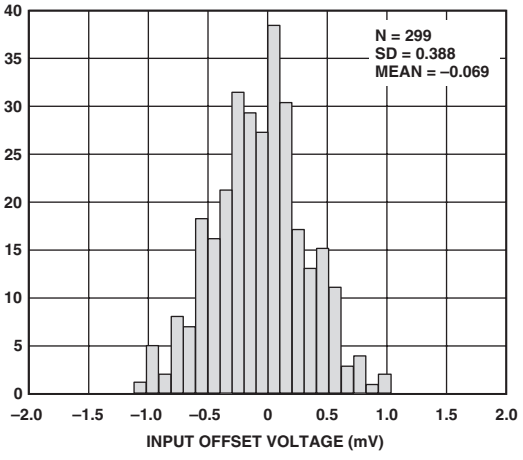
TPC 26. Input Bias Current vs. Temperature



TPC 29. Input Bias Current vs. Common-Mode Voltage Range*

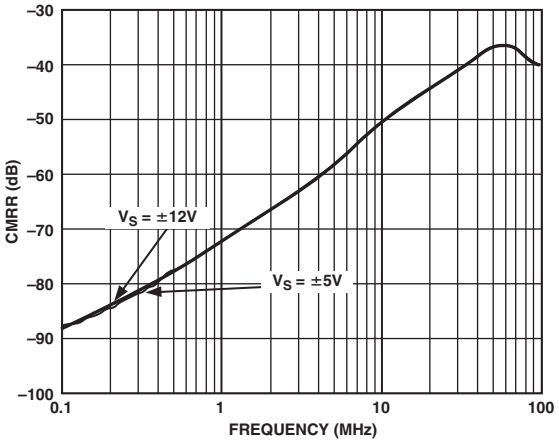


TPC 27. Input Offset Voltage vs. Common-Mode Voltage

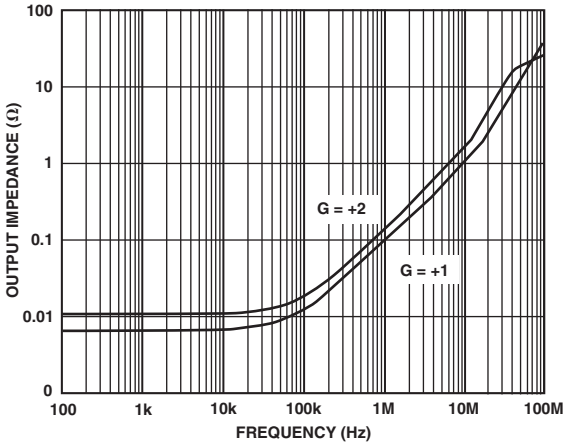


TPC 30. Input Offset Voltage

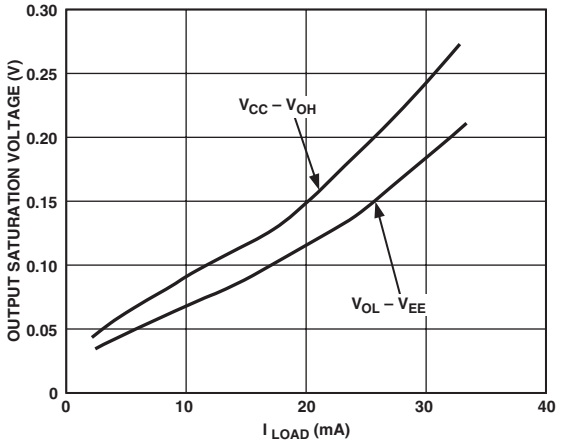
*See Input and Output Overload Behavior Section



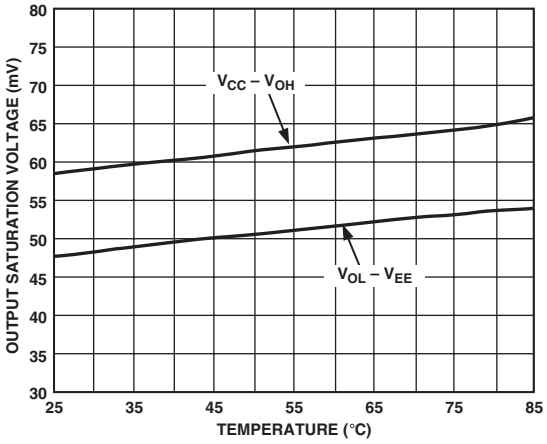
TPC 31. CMRR vs. Frequency (See Test Circuit 5)



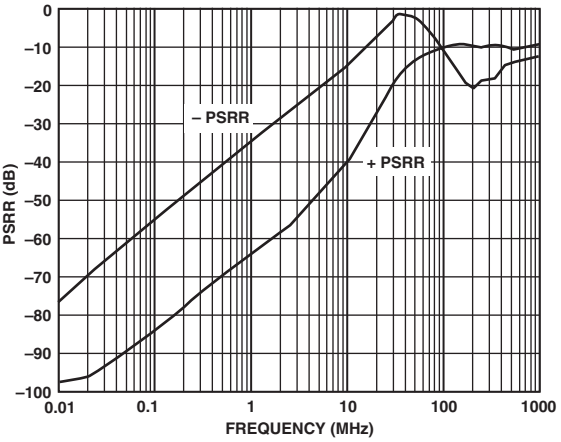
TPC 34. Output Impedance vs. Frequency (See Test Circuits 4 and 6)



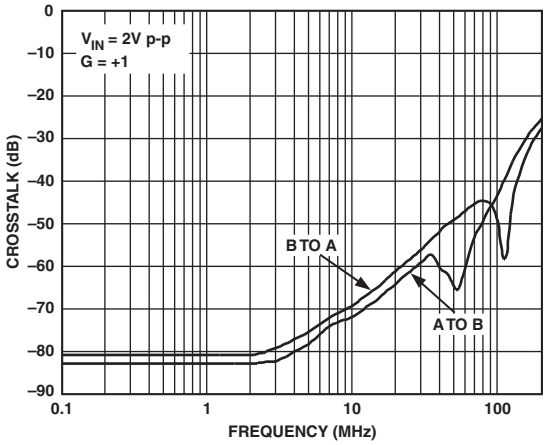
TPC 32. Output Saturation Voltage vs. Output Load Current



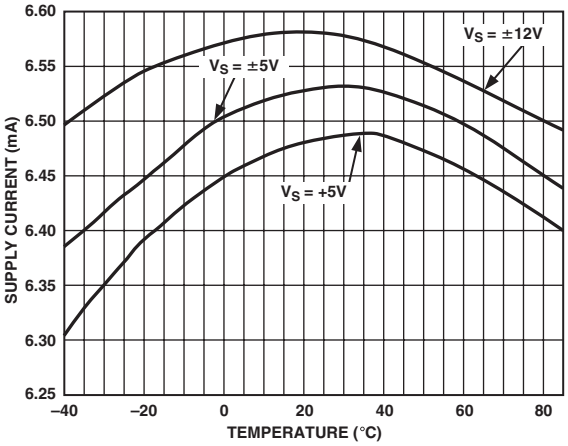
TPC 35. Output Saturation Voltage vs. Temperature



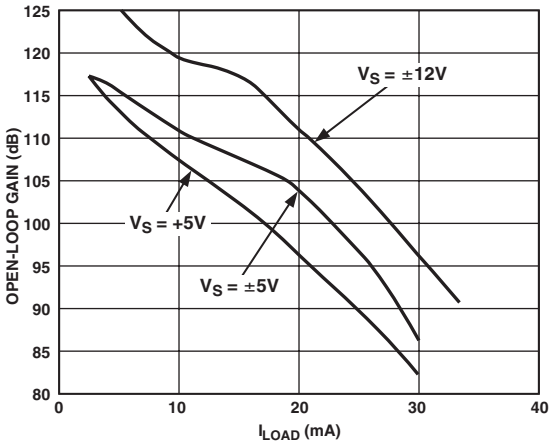
TPC 33. PSRR vs. Frequency (See Test Circuits 7 and 9)



TPC 36. Crosstalk vs. Frequency (See Test Circuit 10)



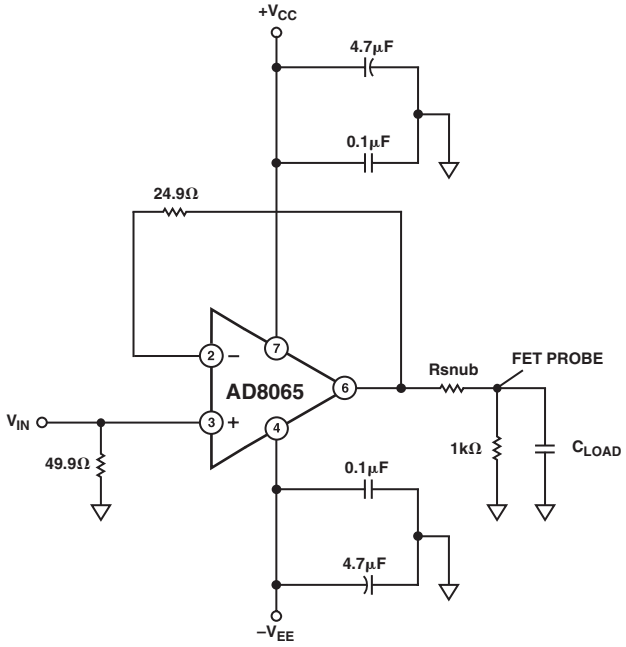
TPC 37. Quiescent Supply Current vs. Temperature for Various Supply Voltages



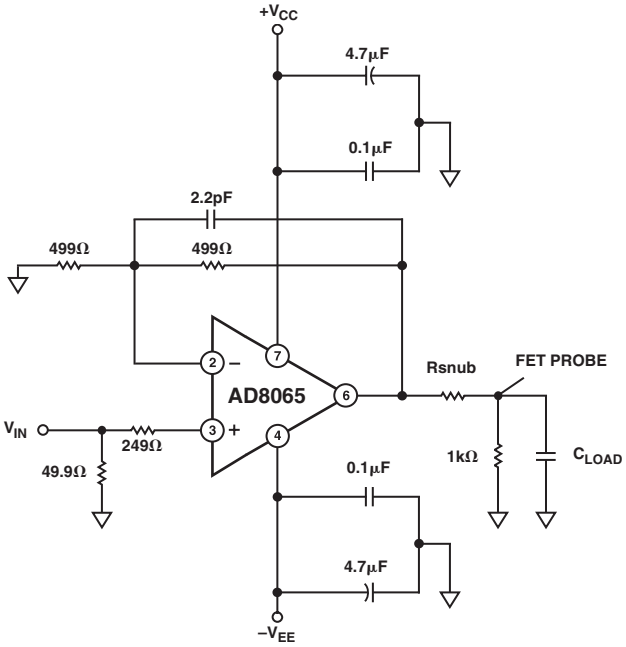
TPC 38. Open-Loop Gain vs. Load Current for Various Supply Voltages

Test Circuits

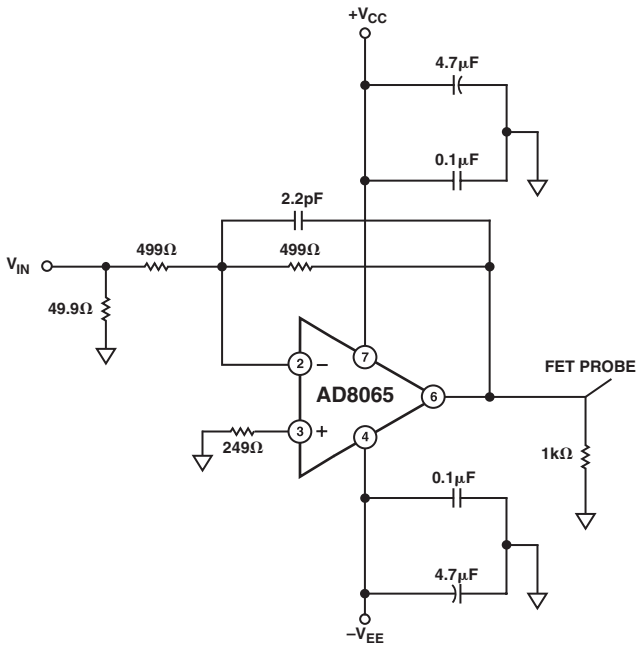
SOIC Pinout



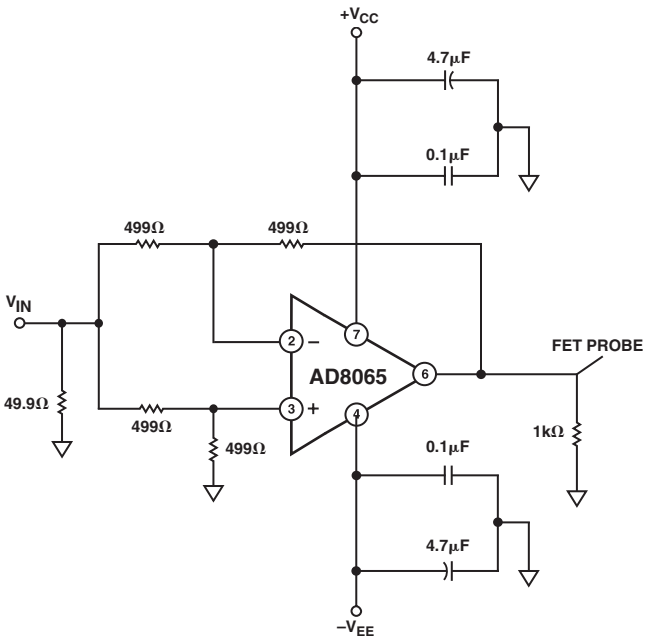
Test Circuit 1. G = +1



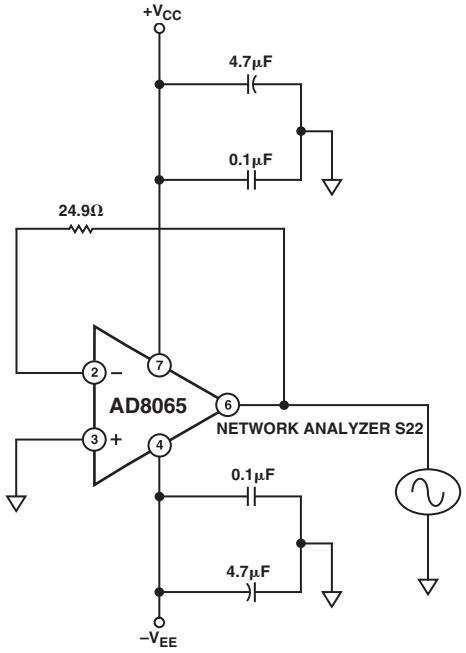
Test Circuit 2. G = +2



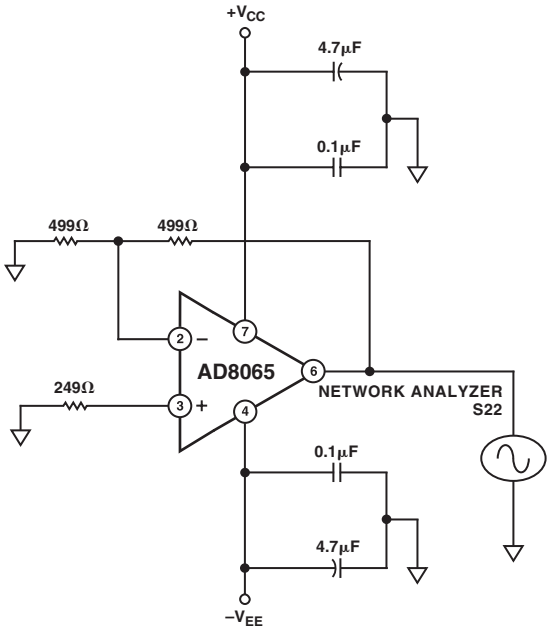
Test Circuit 3. G = –1



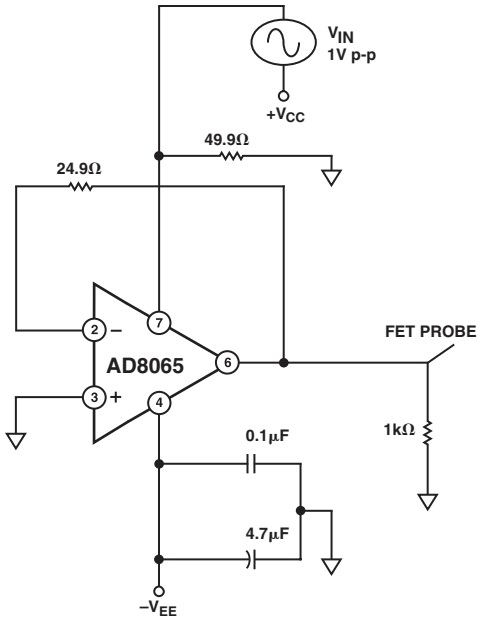
Test Circuit 5. CMRR



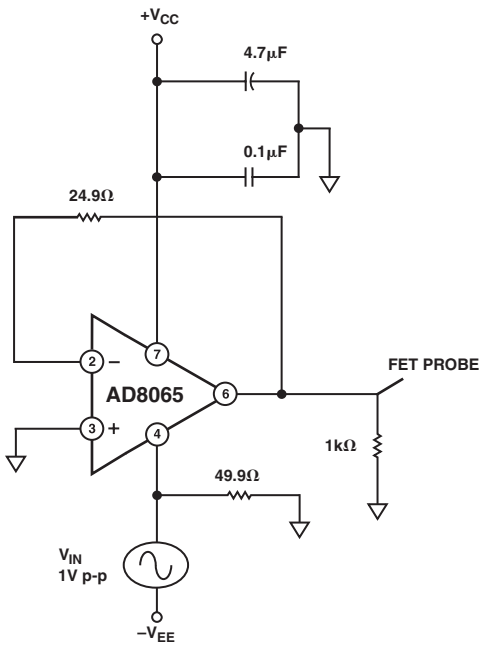
Test Circuit 4. Output Impedance G = +1



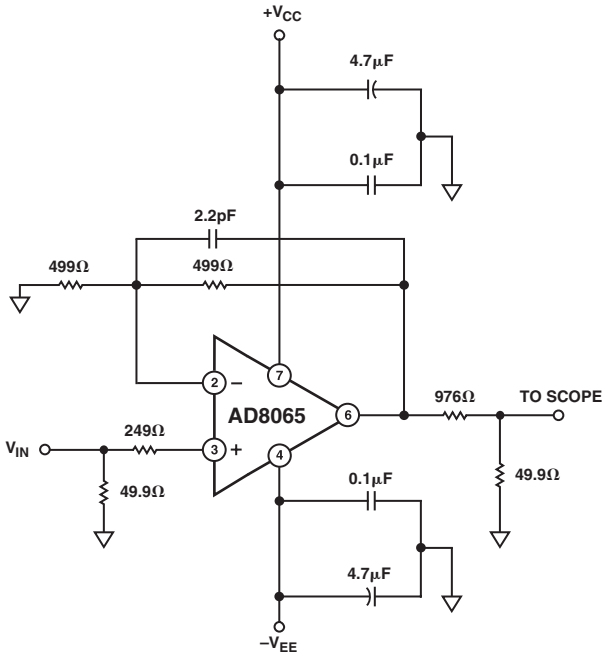
Test Circuit 6. Output Impedance G = +2



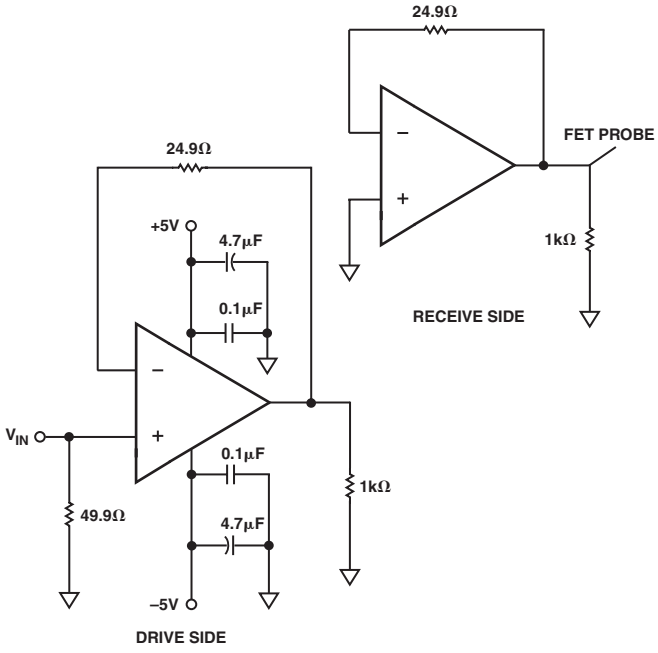
Test Circuit 7. Positive PSRR



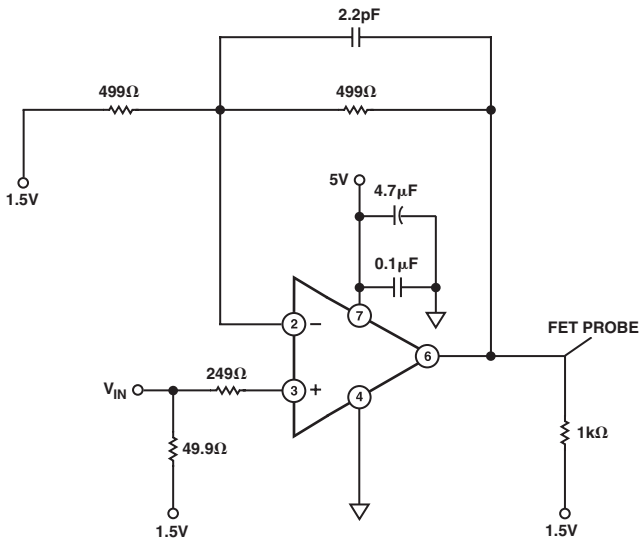
Test Circuit 9. Negative PSRR



Test Circuit 8. Settling Time



Test Circuit 10. Crosstalk – AD8066



Test Circuit 11. Single Supply

THEORY OF OPERATION

The AD8065/AD8066 are voltage feedback operational amplifiers that combine a laser-trimmed JFET input stage with Analog Devices' eXtra Fast Complementary Bipolar process, resulting in an outstanding combination of precision and speed. Supply voltage range is from 5 V to 24 V. The amplifiers feature a patented rail-to-rail output stage capable of driving within 0.5 V of either power supply while sourcing or sinking up to 30 mA. Also featured is a single-supply input stage that handles common-mode signals from below the negative supply to within 3 V of the positive rail. Operation beyond the JFET input range is possible because of an auxiliary bipolar input stage that functions with input voltages up to the positive supply. The amplifiers operate as if they have a rail-to-rail input and exhibit no phase reversal behavior for common-mode voltages within the power supply.

With voltage noise of 7 nV/$\sqrt{\text{Hz}}$ and –88 dBc distortion for 1 MHz 2 V p-p signals, the AD8065/AD8066 are a great choice for high resolution data acquisition systems. Their low noise, sub-pA input current, precision offset, and high speed make them a superb preamps for fast photodiode applications. The speed and output drive capability of the AD8065/AD8066 also make them useful in video applications.

Closed-Loop Frequency Response

The AD8065/AD8066 are classic voltage feedback amplifiers with an open-loop frequency response that can be approximated as the integrator response shown in Figure 3. Basic closed-loop frequency response for inverting and noninverting configurations can be derived from the schematics shown.

Noninverting Closed-Loop Frequency Response

Solving for the transfer function

$$\frac{V_O}{V_I} = \frac{2\pi \times f_{crossover}(R_G + R_F)}{(R_F + R_G)s + 2\pi \times f_{crossover} \times R_G}$$

where $f_{crossover}$ is the frequency where the amplifier's open-loop gain equals 0 db.

At dc

$$\frac{V_O}{V_I} = \frac{R_F + R_G}{R_G}$$

Closed-loop -3 dB frequency

$$f_{-3dB} = f_{crossover} \times \frac{R_G}{R_F + R_G}$$

Inverting Closed-Loop Frequency Response

$$\frac{V_O}{V_I} = \frac{-2\pi \times f_{crossover} \times R_F}{s(R_F + R_G) + 2\pi \times f_{crossover} \times R_G}$$

At dc

$$\frac{V_O}{V_I} = -\frac{R_F}{R_G}$$

Closed-loop -3 dB frequency

$$f_{-3dB} = f_{crossover} \times \frac{R_G}{R_F + R_G}$$

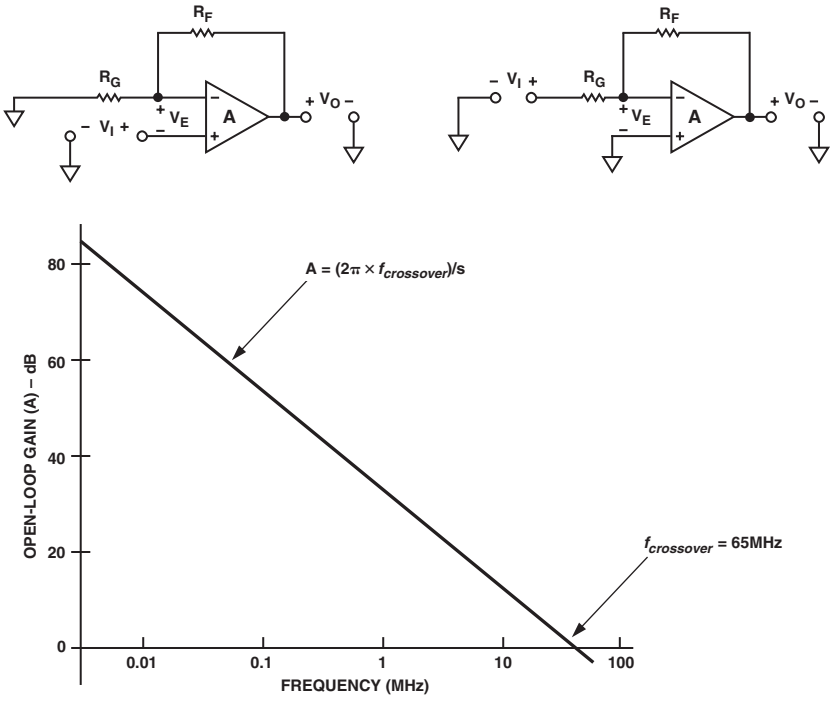


Figure 3. Open Look Gain vs. Frequency and Basic Connections

The closed-loop bandwidth is inversely proportional to the noise gain of the op amp circuit, $(R_F + R_G)/R_G$. This simple model is accurate for noise gains above 2. The actual bandwidth of circuits with noise gains at or below 2 will be higher than those predicted with this model due to the influence of other poles in the frequency response of the real op amp.

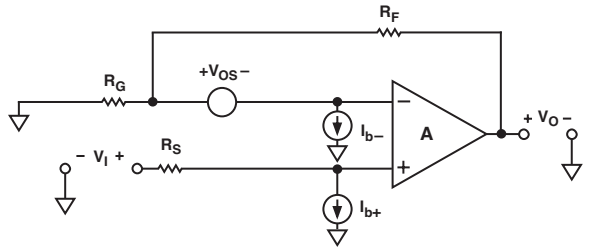


Figure 4. Voltage Feedback Amplifier DC Errors

Figure 4 shows a voltage feedback amplifier's dc errors. For both inverting and noninverting configurations

$$V_O\ (error) = I_{b+} \times R_S \left(\frac{R_G + R_F}{R_G}\right) - I_{b-} \times R_F + V_{OS} \left(\frac{R_G + R_F}{R_G}\right)$$

The voltage error due to I_{b+} and I_{b-} is minimized if $R_S = R_F \| R_G$ (though with the AD8065 input currents at less than 20 pA over temperature, this is likely not a concern). To include common-mode and power supply rejection effects, total V_{OS} can be modeled as

$$V_{OS} = V_{OS_{nom}} + \frac{\Delta V_S}{PSR} + \frac{\Delta V_{CM}}{CMR}$$

$V_{OS_{nom}}$ is the offset voltage specified at nominal conditions. ΔV_S is the change in power supply from nominal conditions. *PSR* is the power supply rejection. ΔV_{CM} is the change in common-mode voltage from nominal conditions. *CMR* is the common-mode rejection.

Wideband Operation

Test Circuits 1, 2, and 3 show the circuits used for wideband characterization for gains of +1, +2, and –1. Source impedance at the summing junction $(R_F \| R_G)$ will form a pole in the amplifier's loop response with the amplifier's input capacitance of 6.6 pF. This can cause peaking and ringing if the time constant formed is too low. Feedback resistances of 300 Ω to 1 kΩ are recommended, since they will not unduly load down the amplifier and the time constant formed will not be too low. Peaking in the frequency response can be compensated with a small capacitor (C_F) in parallel with the feedback resistor, as illustrated in TPC 9. This shows the effect of different feedback capacitances on the peaking and bandwidth for a noninverting G = +2 amplifier.

For the best settling times and the best distortion, the impedances at the AD8065/AD8066 input terminals should be matched. This minimizes nonlinear common-mode capacitive effects that can degrade ac performance.

Actual distortion performance depends on a number of variables:

- The closed-loop gain of the application
- Whether it is inverting or noninverting
- Amplifier loading
- Signal frequency and amplitude
- Board layout

Also see TPCs 13 to 17. The lowest distortion will be obtained with the AD8065 used in low gain inverting applications, since this eliminates common-mode effects. Higher closed-loop gains result in worse distortion performance.

Input Protection

The inputs of the AD8065/AD8066 are protected with back-to-back diodes between the input terminals as well as ESD diodes to either power supply. This results in an input stage with picoamps of input current that can withstand up to 1500 V ESD events (human body model) with no degradation.

Excessive power dissipation through the protection devices will destroy or degrade the performance of the amplifier. Differential voltages greater than 0.7 V will result in an input current of approximately $(|V_+ - V_-| - 0.7\ V)/R_I$, where R_I is the resistance in series with the inputs. For input voltages beyond the positive supply, the input current will be approximately $(V_I - V_{CC} - 0.7)/R_I$. Beyond the negative supply, the input current will be about $(V_I - V_{EE} + 0.7)/R_I$. If the inputs of the amplifier are to be subjected to sustained differential voltages greater than 0.7 V or to input voltages beyond the amplifier power supply, input current should be limited to 30 mA by an appropriately sized input resistor (R_I) as shown in Figure 5.

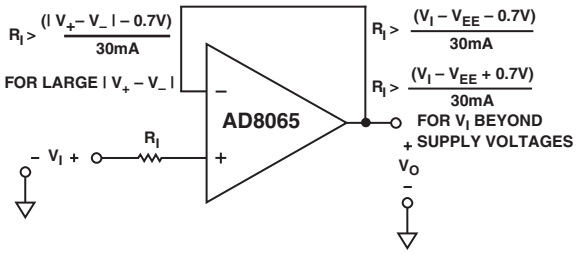


Figure 5. Current Limiting Resistor

Thermal Considerations

With 24 V power supplies and 6.5 mA quiescent current, the AD8065 dissipates 156 mW with no load. The AD8065/AD8066 dissipate 312 mW. This can lead to noticeable thermal effects, especially in the small SOT-23-5 (thermal resistance of 160°C/W). V_{OS} temperature drift is trimmed to guarantee a max drift of 17 µV/°C, so it can change up to 0.425 mV due to warm-up effects for an AD8065/AD8066 in a SOT-23-5 package on 24 V.

I_b increases by a factor of 1.7 for every 10°C rise in temperature. I_b will be close to 5 times higher at 24 V supplies as opposed to a single 5 V supply.

Heavy loads will increase power dissipation and raise the chip junction temperature as described in the Maximum Power Dissipation section. Care should be taken to not exceed the rated power dissipation of the package.

Input and Output Overload Behavior

The AD8065/AD8066 have internal circuitry to guard against phase reversal due to overdriving the input stage. A simplified schematic of the input stage, including the input-protection diodes and antiphase reversal circuitry, is shown in Figure 6.

The circuit is arranged such that when the input common-mode voltage exceeds a certain threshold, the input JFET pair's bias current will turn OFF, and the bias current of an auxiliary NPN pair will turn ON, taking over control of the amplifier. When the input common-mode voltage returns to a viable operating value, the FET stage turns back ON, the NPN stage turns OFF, and normal operation resumes.

The NPN pair can sustain operation with the input voltage up to the positive supply, so this is a pseudo rail-to-rail input stage. For operation beyond the FET stage's common-mode limit, the amplifier's V_{OS} will change to the NPN pair's offset (mean of 160 μV, standard deviation of 820 μV), and I_b will increase to the NPN pair's base current up to 45 μA (see TPC 29).

Switchback, or recovery time, is about 100 ns, as shown in TPC 24.

The output transistors of the rail-to-rail output stage have circuitry to limit the extent of their saturation when the output is overdriven. This helps output recovery time. Output recovery from a 0.5 V output overdrive on a ±5 V supply is shown in TPC 21.

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

Power Supply Bypassing

Power supply pins are actually inputs and care must be taken so that a noise-free stable dc voltage is applied. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering most of the noise.

Decoupling schemes are designed to minimize the bypassing impedance at all frequencies with a parallel combination of capacitors. 0.1 μF (X7R or NPO) chip capacitors are critical and should be as close as possible to the amplifier package. The 4.7 μF tantalum capacitor is less critical for high frequency bypassing, and in most cases, only one is needed per board, at the supply inputs.

Grounding

A ground plane layer is important in densely packed PC boards to spread the current minimizing parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances and therefore the high frequency impedance of the path. High speed currents in an inductive ground return will create an unwanted voltage noise.

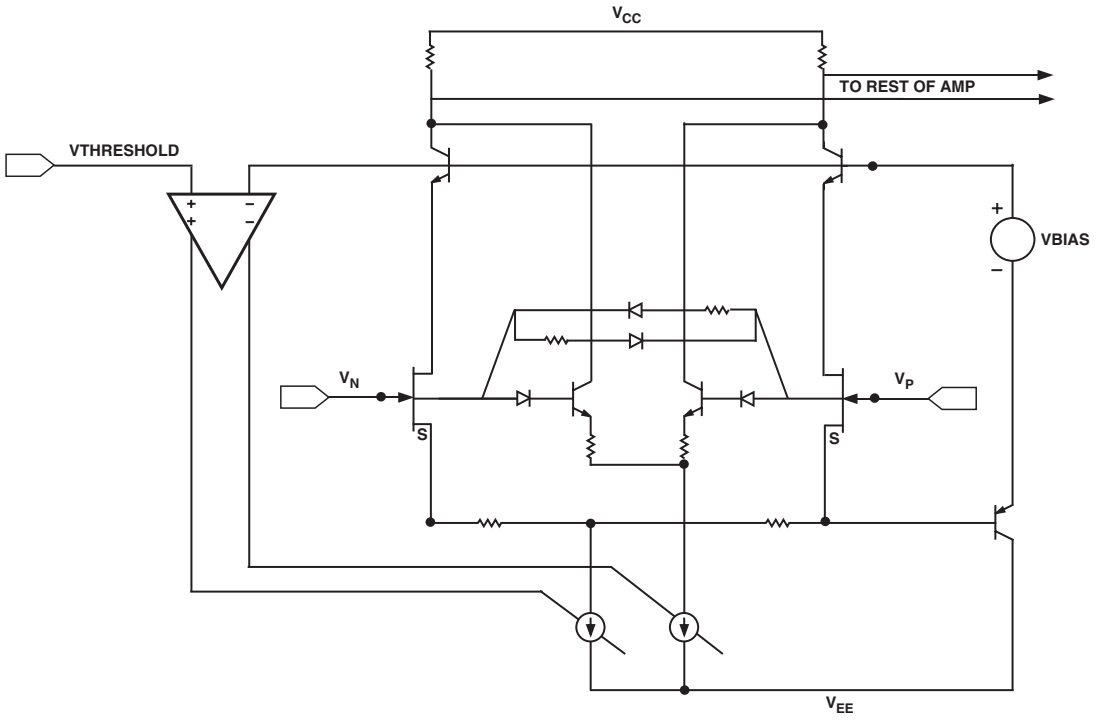


Figure 6. Simplified Input Stage

The length of the high frequency bypass capacitor leads is most critical. A parasitic inductance in the bypass grounding will work against the low impedance created by the bypass capacitor. Place the ground leads of the bypass capacitors at the same physical location. Because load currents flow from the supplies as well, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For the larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical.

Leakage Currents

Poor PC board layout, contaminants, and the board insulator material can create leakage currents that are much larger than the input bias current of the AD8065/AD8066. Any voltage differential between the inputs and nearby runs will set up leakage currents through the PC board insulator, for example, 1 V/100 GΩ = 10 pA. Similarly, any contaminants on the board can create significant leakage (skin oils are a common problem). To significantly reduce leakages, put a guard ring (shield) around the inputs and input leads that are driven to the same voltage potential as the inputs. This way there is no voltage potential between the inputs and surrounding area to set up any leakage currents. For the guard ring to be completely effective, it must be driven by a relatively low impedance source and should completely surround the input leads on all sides, above and below, using a multilayer board.

Another effect that can cause leakage currents is the charge absorption of the insulator material itself. Minimizing the amount of material between the input leads and the guard ring will help to reduce the absorption. Also, low absorption materials, such as Teflon® or ceramic, may be necessary in some instances.

Input Capacitance

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. A few pF of capacitance will reduce the input impedance at high frequencies, in turn increasing the amplifier's gain, causing peaking of the frequency response or even oscillations, if severe enough. It is recommended that the external passive components connected to the input pins be placed as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a small distance from the input pins on all layers of the board.

Output Capacitance

To a lesser extent, parasitic capacitances on the output can cause peaking and ringing of the frequency response. There are two methods to effectively minimize their effect.

1) As shown in Figure 7, put a small value resistor (R_S) in series with the output to isolate the load capacitor from the amp's output stage. A good value to choose is 20 Ω (see TPC 7).

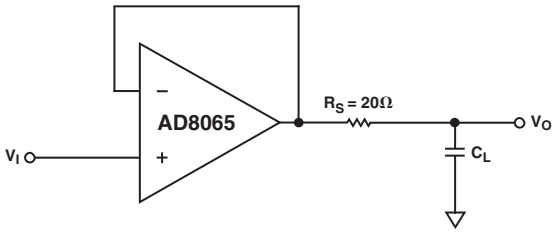


Figure 7. Output Isolation Resistor

2) Increase the phase margin with higher noise gains or add a pole with a parallel resistor and capacitor from –IN to the output.

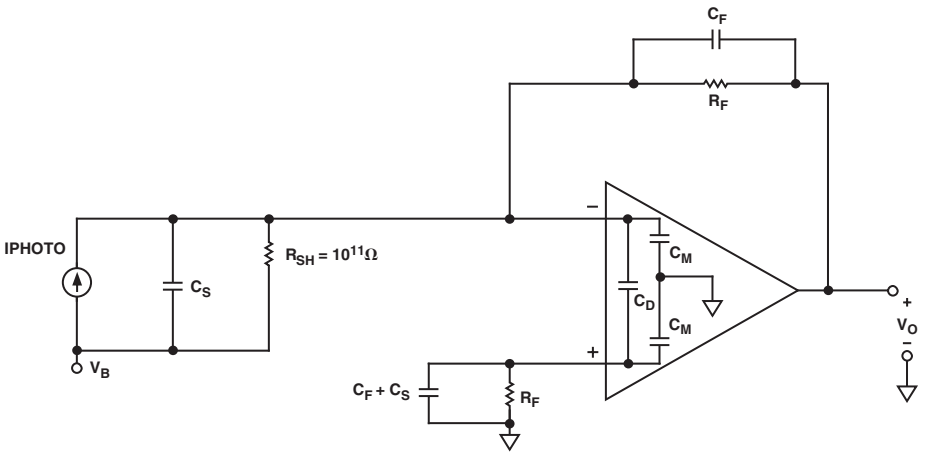


Figure 8. Wideband Photodiode Preamp

Input-to-Output Coupling
In order to minimize capacitive coupling between the inputs and output, the output signal traces should not be parallel with inputs.

Wideband Photodiode Preamp
Figure 8 shows an I/V converter with an electrical model of a photodiode. The basic transfer function is where

$$V_{OUT} = \frac{I_{PHOTO} \times R_F}{1 + sC_F R_F}$$

I_{PHOTO} is the output current of the photodiode and the parallel combination of R_F and C_F set the signal bandwidth.

The stable bandwidth attainable with this preamp is a function of R_F, the gain bandwidth product of the amplifier, and the total capacitance at the amplifier's summing junction, including C_S and the amplifier input capacitance. R_F and the total capacitance produce a pole in the amplifier's loop transmission that can result in peaking and instability. Adding C_F creates a zero in the loop transmission that compensates for the pole's effect and reduces the signal bandwidth. It can be shown that the signal bandwidth resulting in a 45° phase margin ($f_{(45)}$) is defined by the expression

$$f_{(45)} = \sqrt{\frac{f_{CR}}{2\pi \times R_F \times C_S}}$$

where:

f_{CR} is the the amplifier crossover frequency.

R_F is the feedback resistor.

C_S is the total capacitance at the amplifier summing junction (amplifier + photodiode + board parasitics).

The value of C_F that produces $f_{(45)}$ can be shown to be

$$C_F = \sqrt{\frac{C_S}{2\pi \times R_F \times f_{CR}}}$$

The frequency response in this case will show about 2 dB of peaking and 15% overshoot. Doubling C_F and cutting the bandwidth in half will result in a flat frequency response, with about 5% transient overshoot.

The preamp's output noise over frequency is shown in Figure 9.

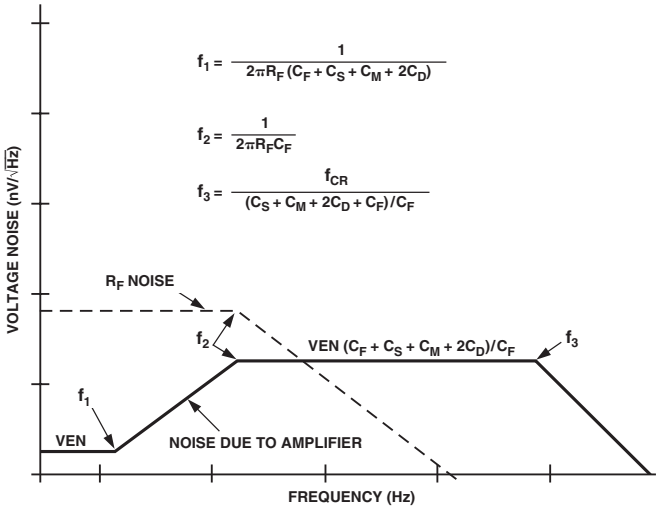


Figure 9. Photodiode Voltage Noise Contributions

The pole in the loop transmission translates to a zero in the amplifier's noise gain, leading to an amplification of the input voltage noise over frequency. The loop transmission zero introduced by C_F limits the amplification. The noise gain's bandwidth extends past the preamp signal bandwidth and is eventually rolled off by the decreasing loop gain of the amplifier. Keeping the input terminal impedances matched is recommended to eliminate common-mode noise peaking effects, which will add to the output noise.

Integrating the square of the output voltage noise spectral density over frequency and then taking the square root allows users to obtain the total rms output noise of the preamp. Table I summarizes approximations for the amplifier and feedback and source resistances. Noise components for an example preamp with R_F = 50 kΩ, C_S = 15 pF, and C_F = 2 pF (bandwidth of about 1.6 MHz) are also listed.

Table 1. RMS Noise Contributions of Photodiode Preamp

Contributor	Expression	RMS Noise with R_F =50 kΩ C_S = 15pF, C_S = 15pF
R_F (×2)	$\sqrt{2 \times 4\,kT \times R_F \times f_2 \times 1.57}$	64.5 μV
Amp to f_1	$ven \times \sqrt{f_1}$	2.4 μV
Amp (f_1–f_1)	$ven \times \sqrt{\frac{(C_S + C_M + C_F + 2C_D)}{C_F}} \times \sqrt{f_2 - f_1}$	31 μV
Amp to (past f_2)	$ven \times \sqrt{\frac{(C_S + C_M + C_D + 2C_F)}{C_F}} \times \sqrt{f_3 \times 1.57}$	260 μV
		270 μV **(Total)**

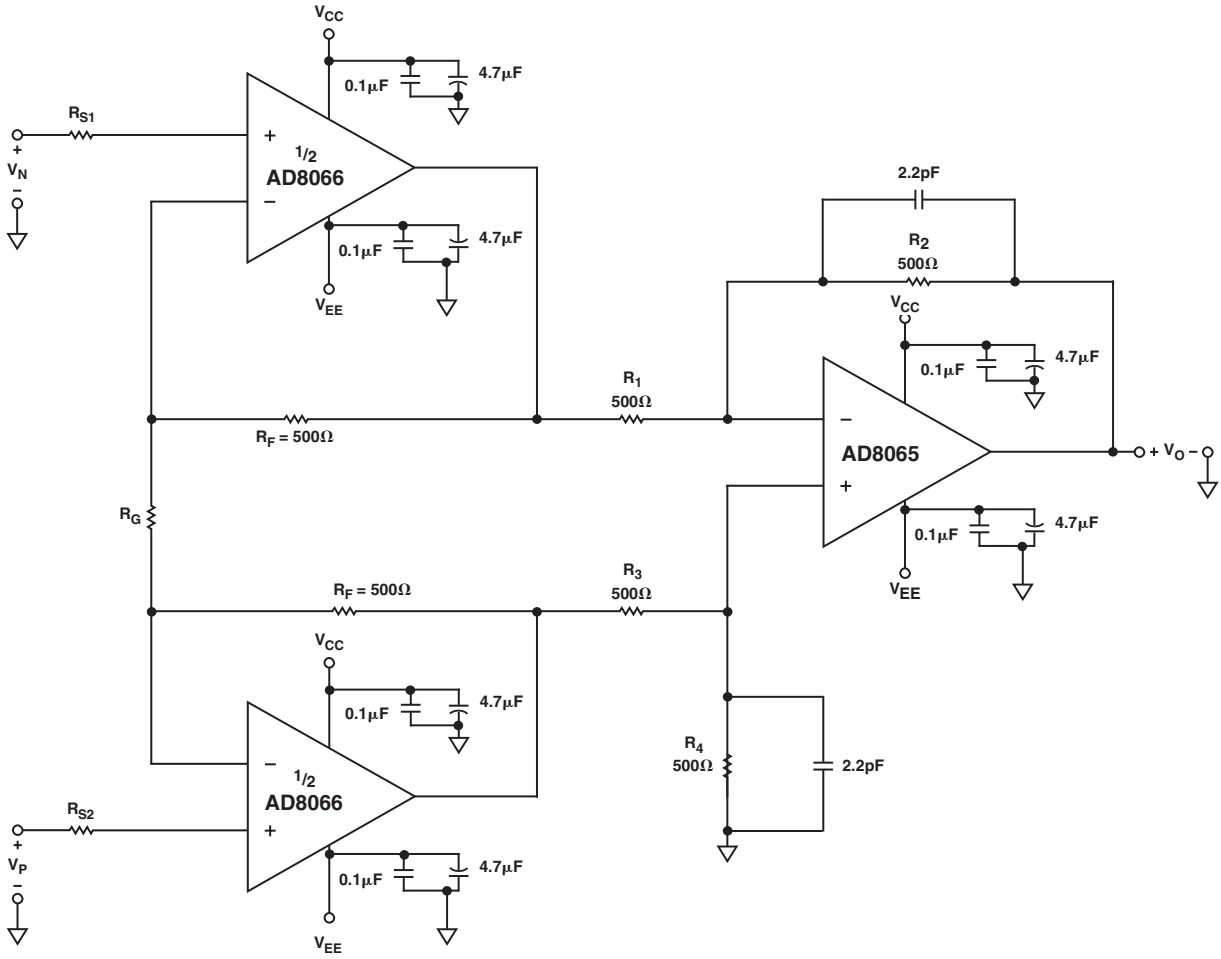


Figure 10. High Speed Instrumentation Amplifier

High Speed JFET Input Instrumentation Amplifier

Figure 10 shows an example of a high speed instrumentation amplifier with high input impedance using the AD8065/AD8066. The dc transfer function is

$$V_{OUT} = (V_N - V_P)\left(\frac{1+1000}{R_G}\right)$$

For G = +1, it is recommended that the feedback resistors for the two preamps be set to a low value (for instance 50 Ω for 50 Ω source impedance). The bandwidth for G = +1 will be 50 MHz. For higher gains, the bandwidth will be set by the preamp, equaling

$$Inamp_{-3dB} = (f_{CR} \times R_G) / (2 \times R_F)$$

Common-mode rejection of the inamp will be primarily determined by the match of the resistor ratios R1:R2 to R3:R4. It can be estimated

$$\frac{V_O}{V_{CM}} = \frac{(\delta 1 - \delta 2)}{(1+\delta 1)\,\delta 2}$$

The summing junction impedance for the preamps is equal to $R_F \| 0.5(R_G)$. This is the value to be used for matching purposes.

Video Buffer

The output current capability and speed of the AD8065 make it useful as a video buffer, shown in Figure 11.

The G = +2 configuration compensates for the voltage division of the signal due to the signal termination. This buffer maintains 0.1 dB flatness for signals up to 7 MHz, from low amplitudes up to 2 V p-p (TPC 4). Differential gain and phase have been measured to be 0.02% and 0.028° at ±5 V supplies.

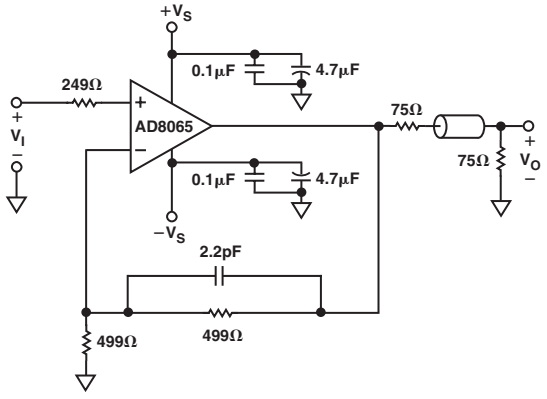
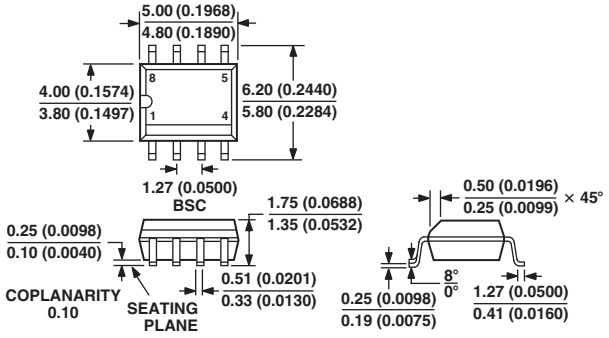


Figure 11. Video Buffer

OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package (SOIC)
Narrow Body
(R-8)

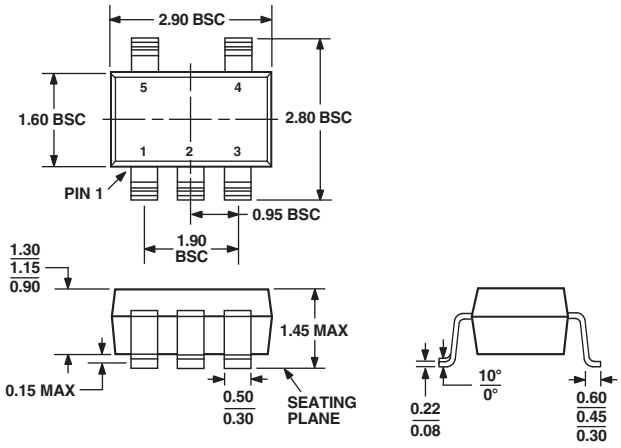
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

5-Lead Plastic Surface Mount Package (SOT-23)
(RT-5)

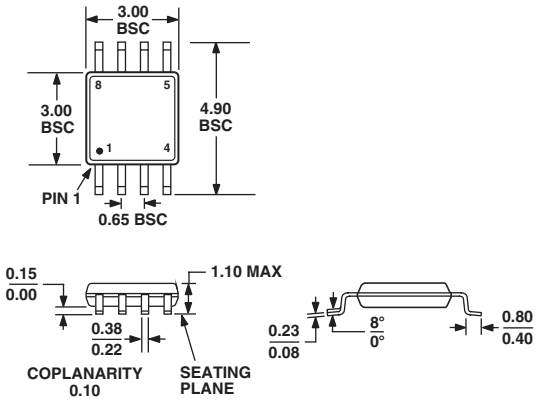
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178AA

8-Lead MicroSOIC Package (MSOP)
(RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

Revision History

Location	Page
4/03–Data Sheet changed from REV. B to REV. C.	
Added SOIC-8 (R) for the AD8065	4
2/03–Data Sheet changed from REV. A to REV. B.	
Changes to ABSOLUTE MAXIMUM RATINGS	4
Changes to Test Circuit 10	14
Changes to Test Circuit 11	15
Changes to Noninverting Closed-Loop Frequency Response	16
Changes to Inverting Closed-Loop Frequency Response	16
Updated Figure 6	18
Changes to Figure 7	19
Changes to Figures 10	21
Changes to Figure 11	22
Changes to High Speed JFET Instrumentation Amplifier	22
Changes to Video Buffer	22
8/02–Data Sheet changed from REV. 0 to REV. A.	
Added AD8066	Universal
Added SOIC-8 (R) and MSOP-8 (RM)	1
Edits to GENERAL DESCRIPTION	1
Edits to SPECIFICATIONS	2
New Figure 2	5
Changes to ORDERING GUIDE	5
Edits to TPCs 18, 25, and 28	8
New TPC 36	11
Added Test Circuits 10 and 11	14
MSOP (RM-8) added	23