Low Power, 3.3 V, RS-232 Line Drivers/Receivers

ADM3202/ADM3222/ADM1385

FEATURES

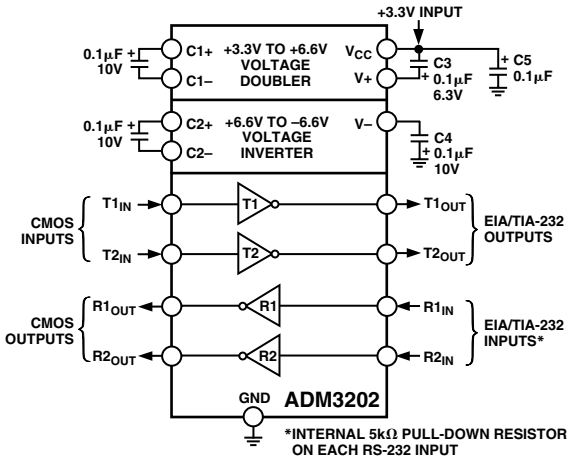
460 kbps Data Rate
Specified at 3.3 V
Meets EIA-232E Specifications
0.1 μF Charge Pump Capacitors
Low Power Shutdown (ADM3222E and ADM1385)
DIP, SO, SOIC, SSOP and TSSOP Package Options
Upgrade for MAX3222/32 and LTC1385

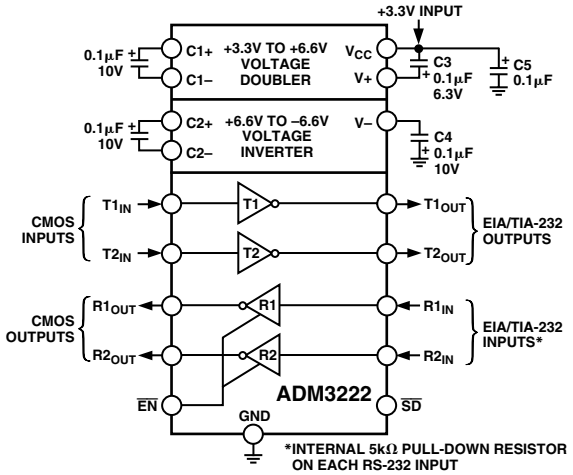
ESD Protection to IEC1000-4-2 (801.2)
on RS-232 Pins (ADM3202 Only)
±8 kV: Contact Discharge
±15 kV: Air-Gap Discharge

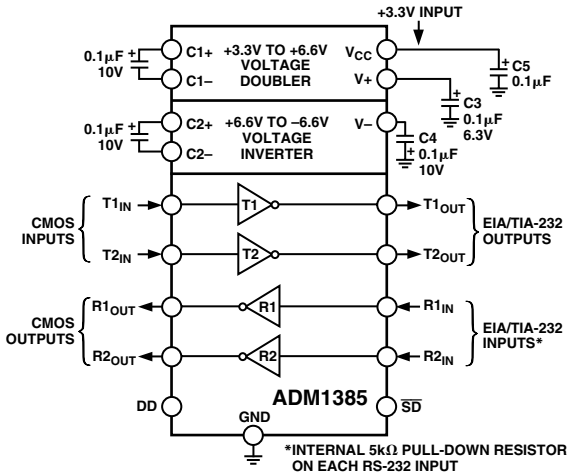
APPLICATIONS

General Purpose RS-232 Data Link
Portable Instruments
Printers
Palmtop Computers
PDAs

FUNCTIONAL BLOCK DIAGRAMS







GENERAL DESCRIPTION

The ADM3202/ADM3222/ADM1385 transceivers are high speed, 2-channel RS-232/V.28 interface devices which operate from a single 3.3 V power supply.

Low power consumption and a shutdown facility (ADM3222/ADM1385) makes them ideal for battery powered portable instruments.

The ADM3202/ADM3222/ADM1385 conforms to the EIA-232E and CCITT V.28 specifications and operates at data rates up to 460 kbps.

Four external 0.1 μF charge pump capacitors are used for the voltage doubler/inverter permitting operation from a single 3.3 V supply.

The ADM3222 contains additional enable and shutdown circuitry. The $\overline{EN}$ input may be used to three-state the receiver outputs. The $\overline{SD}$ input is used to power down the charge pump and transmitter outputs reducing the quiescent current to less than 0.5 μA. The receivers remain enabled during shutdown unless disabled using $\overline{EN}$.

The ADM1385 contains a driver disable mode and a complete shutdown mode.

The ADM3202 is available in a 16-lead DIP, narrow and wide SOIC as well as a space saving 16-lead TSSOP package. The ADM3222 is available in 18-lead DIP, SO and in 20-lead SSOP and TSSOP. The ADM1385 is available in a 20-lead SSOP package, which is pin compatible with the LTC1385 CG.

REV. B

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703
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ADM3202/ADM3222/ADM1385–SPECIFICATIONS

(V_{CC} = 3.3 V ± 0.3 V, C1–C4 = 0.1 µF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC CHARACTERISTICS					
Operating Voltage Range	3.0	3.3	5.5	V	
V_{CC} Power Supply Current		1.3	3	mA	No Load
		8	12	mA	R_L = 3 kΩ to GND
Shutdown Supply Current		0.01	0.5	µA	
LOGIC					
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA
CMOS Output Voltage High, V_{OH}	V_{CC} – 0.6			V	I_{OUT} = –1 mA
Logic Pull-Up Current		5	10	µA	T_{IN} = GND to V_{CC}*
Output Leakage Current			±10	µA	Receivers Disabled
RS-232 RECEIVER					
EIA-232 Input Voltage Range	–30		+30	V	
EIA-232 Input Threshold Low	0.6	1.2		V	
EIA-232 Input Threshold High		1.6	2.4	V	
EIA-232 Input Hysteresis		0.4		V	
EIA-232 Input Resistance	3	5	7	kΩ	
RS-232 TRANSMITTER					
Output Voltage Swing (RS-232)	±5.0	±5.2		V	V_{CC} = 3.3 V. All Transmitter Outputs Loaded with 3 kΩ to Ground
Output Voltage Swing (RS-562)	±3.7			V	V_{CC} = 3.0 V
Transmitter Output Resistance	300			Ω	V_{CC} = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±15		mA	
Output Leakage Current			±25	µA	SD = Low, V_{OUT} = 12 V
TIMING CHARACTERISTICS					
Maximum Data Rate	460			kbps	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 1000 pF. One Tx Switching
Receiver Propagation Delay					
TPHL		0.4	1	µs	
TPLH		0.4	1	µs	
Transmitter Propagation Delay		300	1.2	µs	R_L = 3 kΩ, C_L = 1000 pF
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Transmitter Skew		30		ns	
Receiver Skew		300		ns	
Transition Region Slew Rate					Measured from +3 V to –3 V or –3 V to +3 V, V_{CC} = +3.3 V
	5.5	10	30	V/µs	R_L = 3 kΩ, C_L = 1000 pF, T_A = 25°C

*ADM1385: Input leakage current typically –10 µA when T_{IN} = GND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . –0.3 V to +6 V
V+ . . . . . (V_{CC} – 0.3 V) to +14 V
V– . . . . . +0.3 V to –14 V
Input Voltages
  T_{IN} . . . . . –0.3 V to (V+, +0.3 V)
  R_{IN} . . . . . ±30 V
Output Voltages
  T_{OUT} . . . . . ±15 V
  R_{OUT} . . . . . –0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous
Power Dissipation
  Power Dissipation N-16 . . . . . 450 mW
    (Derate 6 mW/°C above 50°C)
    θ_{JA}, Thermal Impedance . . . . . 117°C/W
  Power Dissipation R-16 . . . . . 450 mW
    (Derate 6 mW/°C above 50°C)
    θ_{JA}, Thermal Impedance . . . . . 158°C/W
  Power Dissipation RU-16 . . . . . 500 mW
    (Derate 6 mW/°C above 50°C)
    θ_{JA}, Thermal Impedance . . . . . 158°C/W
  Power Dissipation R-18 . . . . . 450 mW
    (Derate 6 mW/°C above 50°C)
    θ_{JA}, Thermal Impedance . . . . . 158°C/W
  Power Dissipation RS-20 . . . . . 450 mW
    (Derate 6 mW/°C above 50°C)
    θ_{JA}, Thermal Impedance . . . . . 158°C/W
  Power Dissipation RU-20 . . . . . 450 mW
    (Derate 6 mW/°C above 50°C)
    θ_{JA}, Thermal Impedance . . . . . 158°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ORDERING GUIDE

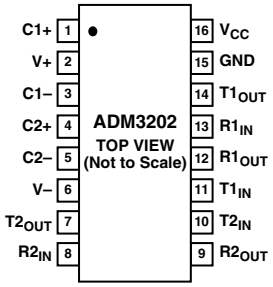
Model	Temperature Range	Package Options*
ADM3202AN	–40°C to +85°C	N-16
ADM3202ARN	–40°C to +85°C	R-16A
ADM3202ARW	–40°C to +85°C	R-16
ADM3202ARU	–40°C to +85°C	RU-16
ADM3222AN	–40°C to +85°C	N-18
ADM3222ARW	–40°C to +85°C	R-18
ADM3222ARS	–40°C to +85°C	RS-20
ADM3222ARU	–40°C to +85°C	RU-20
ADM1385ARS	–40°C to +85°C	RS-20

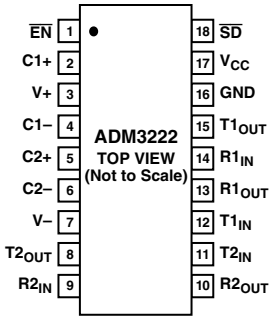
*N = Plastic DIP; R = Small Outline; RS = Shrink Small Outline; RU = Thin Shrink Small Outline.

PIN FUNCTION DESCRIPTIONS

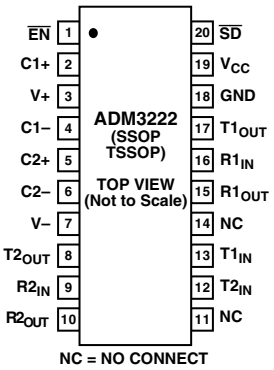
Mnemonic	Function
V_{CC}	Power Supply Input: 3.3 V ± 0.3 V.
V+	Internally Generated Positive Supply (+6 V Nominal).
V–	Internally Generated Negative Supply (–6 V Nominal).
GND	Ground Pin. Must be connected to 0 V.
C1+, C1–	External Capacitor 1 is connected between these pins. 0.1 µF capacitor is recommended but larger capacitors up to 47 µF may be used.
C2+, C2–	External Capacitor 2 is connected between these pins. 0.1 µF capacitor is recommended but larger capacitors up to 47 µF may be used.
Tx_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels.
Tx_{OUT}	Transmitter (Driver) Outputs. These are RS-232 signal levels (typically ±9 V).
Rx_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
Rx_{OUT}	Receiver Outputs. These are CMOS output logic levels.
$\overline{EN}$	(ADM3222) Receiver Enable, Active Low. When low, the receiver outputs are enabled. When high, they are three-stated.
$\overline{SD}$	(ADM3222) Shutdown Control. Active Low. When low, the charge pump is shut down and the transmitter outputs are disabled.
$\overline{SD}$	(ADM1385) Shutdown Control. When low, the charge pump is shut down and all transmitters and receivers are disabled.
DD	(ADM1385) Driver Disable. When low, the charge pump is turned off and the transmitters are disabled. The receivers remain active.

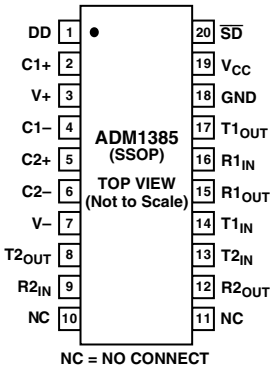
PIN CONNECTIONS DIP (N, R Packages)

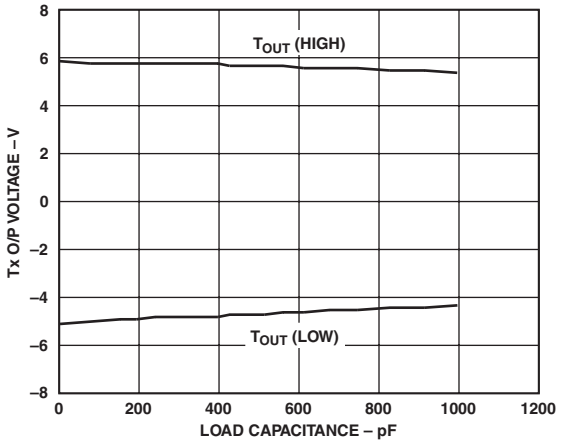




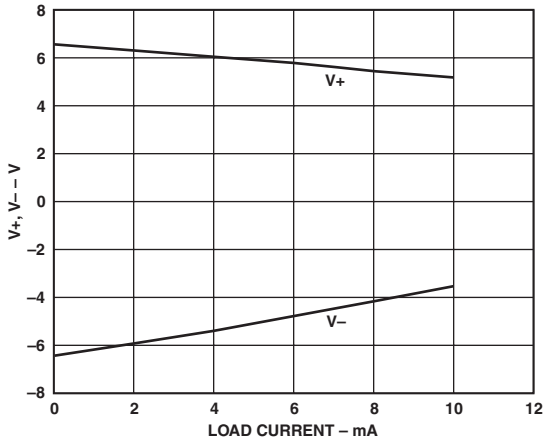
PIN CONNECTIONS DIP (RS, RU Packages)



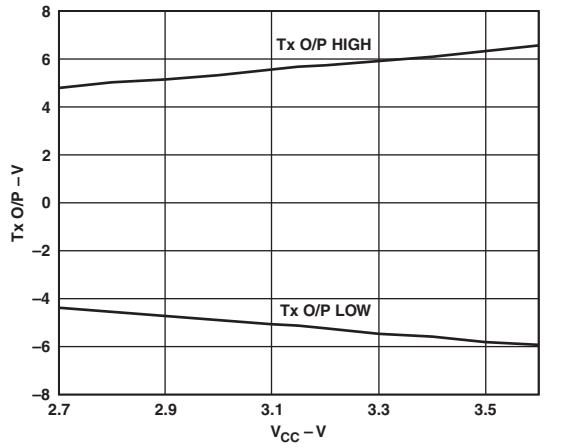




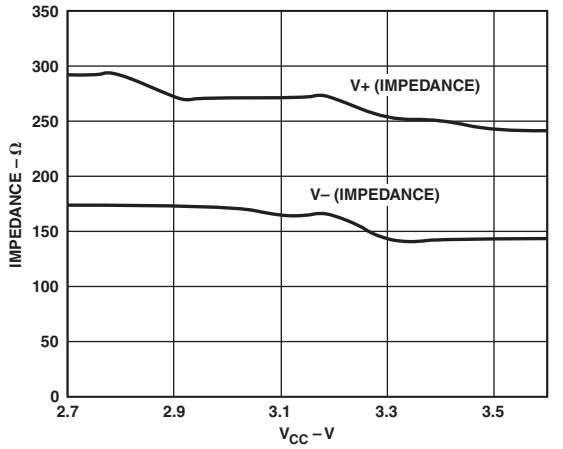
TPC 1. Transmitter Output Voltage High/Low vs. Load Capacitance @ 460 kbps



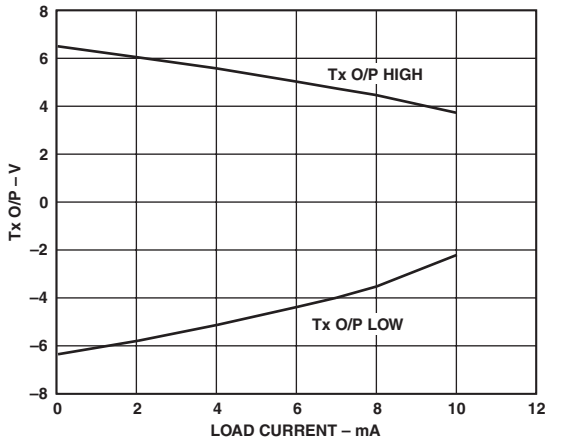
TPC 4. Charge Pump V+, V– vs. Load Current



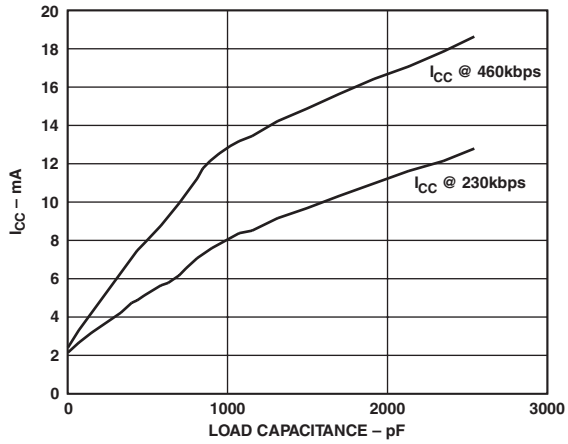
TPC 2. Transmitter Output Voltage vs. V_{CC}



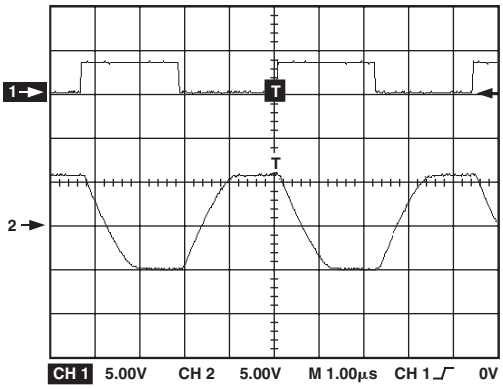
TPC 5. Charge Pump Impedance vs. V_{CC}



TPC 3. Transmitter Output Voltage Low/High vs. Load Current



TPC 6. Power Supply Current vs. Load Capacitance



TPC 7. 460 kbps Data Transmission

GENERAL DESCRIPTION

The ADM3202/ADM3222/ADM1385 are RS-232 line drivers/receivers. Step-up voltage converters coupled with level shifting transmitters and receivers allow RS-232 levels to be developed while operating from a single 3.3 V supply.

CMOS technology is used to keep the power dissipation to an absolute minimum, allowing maximum battery life in portable applications.

The ADM3202/ADM3222/ADM1385 is a modification, enhancement and improvement to the AD230–AD241 family and its derivatives. It is essentially plug-in compatible and does not have materially different applications.

CIRCUIT DESCRIPTION

The internal circuitry consists of three main sections. These are:

1. A charge pump voltage converter
2. 3.3 V logic to EIA-232 transmitters
3. EIA-232 to 5 V logic receivers.

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of a 200 kHz oscillator and a switching matrix. The converter generates a ±6.6 V supply from the input 3.3 V level. This is done in two stages using a switched capacitor technique as illustrated below. First, the 3.3 V input supply is doubled to 6.6 V using capacitor C1 as the charge storage element. The +6.6 V level is then inverted to generate –6.6 V using C2 as the storage element. C3 is shown connected between V+ and V_{CC}, but is equally effective if connected between V+ and GND.

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be increased if desired. Capacitor C3 is shown connected between V+ and V_{CC}. It is also acceptable to connect this capacitor between V+ and GND.

If desired, larger capacitors (up to 10 µF) can be used for capacitors C1–C4.

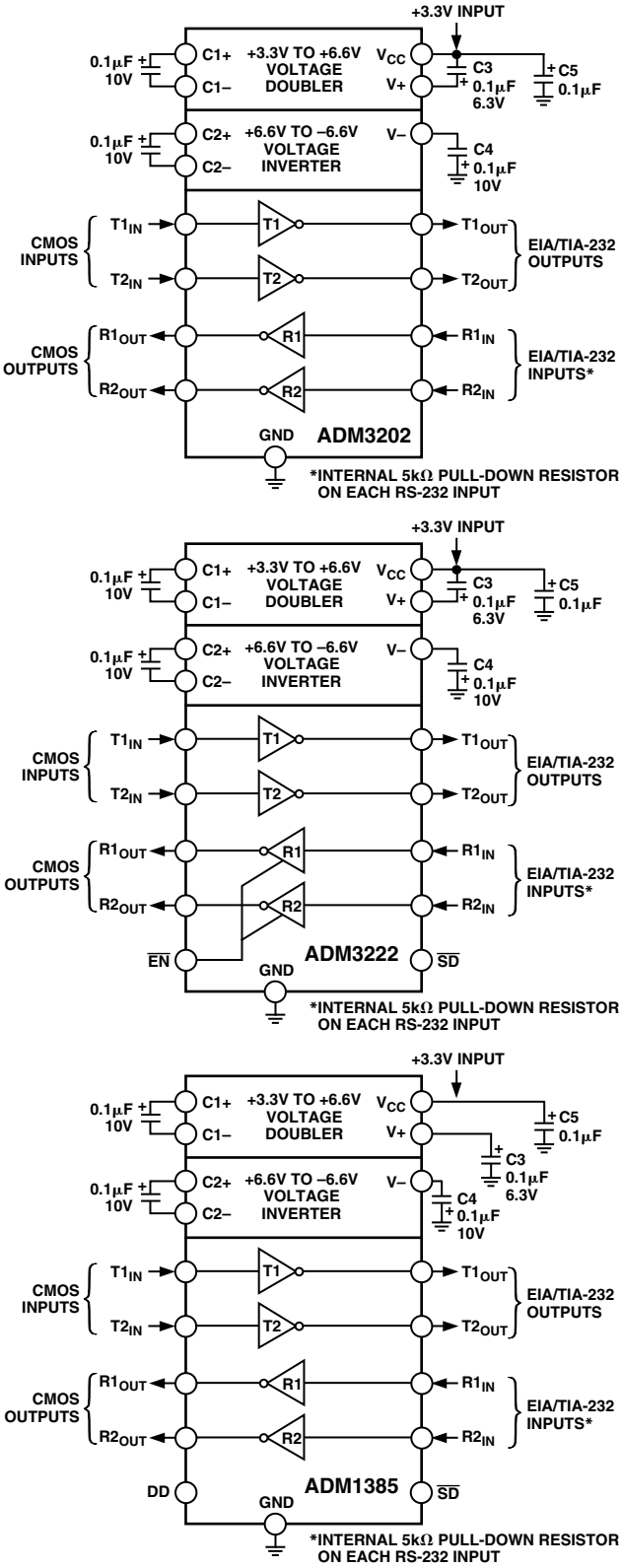


Figure 1. Typical Operating Circuits

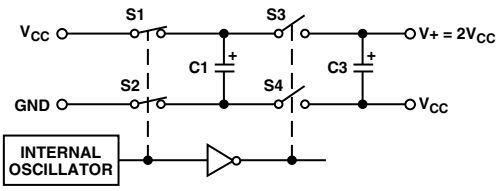


Figure 2. Charge Pump Voltage Doubler

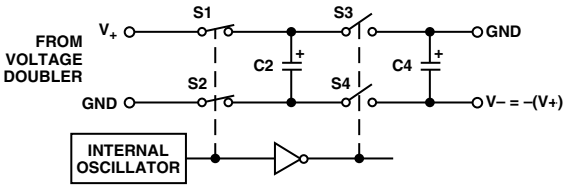


Figure 3. Charge Pump Voltage Inverter

Transmitter (Driver) Section

The drivers convert 3.3 V logic input levels into RS-232 output levels. With V_{CC} = 3.3 V and driving an RS-232 load, the output voltage swing is typically ±6 V.

Receiver Section

The receivers are inverting level-shifters that accept RS-232 input levels and translate them into 3 V logic output levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. Unconnected inputs are pulled to 0 V by the internal 5 kΩ pull-down resistor. This, therefore, results in a Logic 1 output level for unconnected inputs or for inputs connected to GND.

The receivers have Schmitt trigger inputs with a hysteresis level of 0.4 V. This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

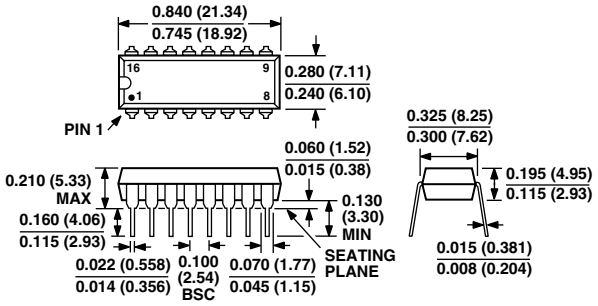
HIGH BAUD RATE

The ADM3202E/ADM3222E feature high slew rates permitting data transmission at rates well in excess of the EIA/RS-232E specifications. RS-232 voltage levels are maintained at data rates up to 460 kbps even under worst case loading conditions. This allows for high speed data links between two terminals or indeed it is suitable for the new generation I_{SDN} modem standards which requires data rates of 230 kbps. The slew rate is internally controlled to less than 30 V/µs in order to minimize EMI interference.

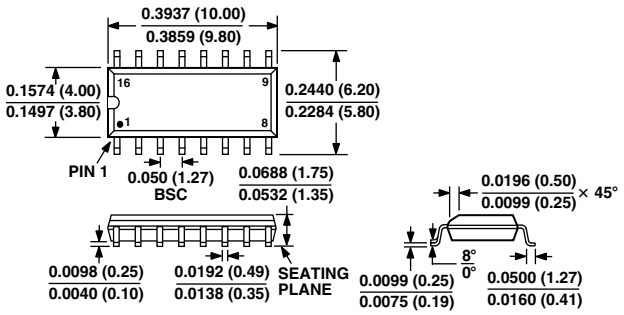
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

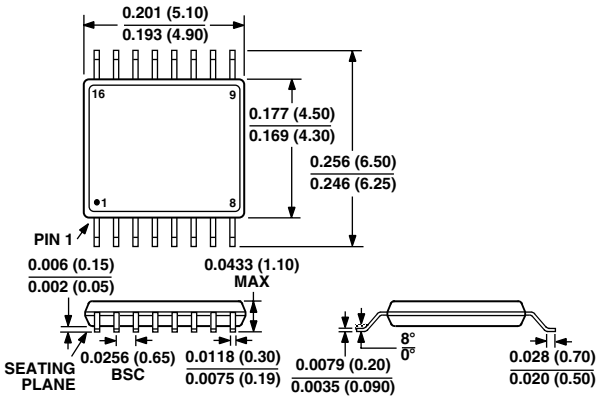
16-Lead Plastic DIP (N-16)



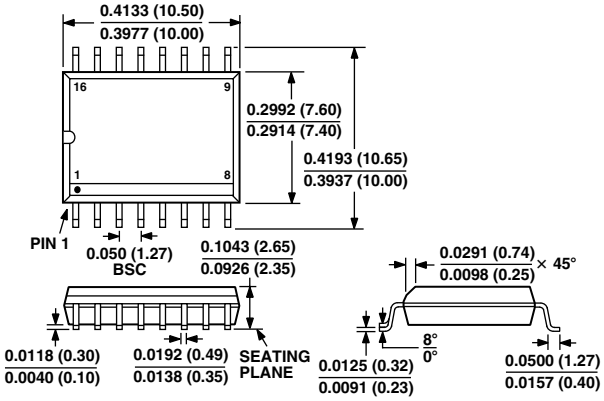
16-Lead Narrow Body SOIC (R-16A)



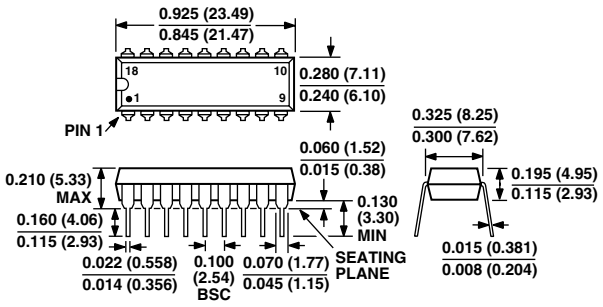
16-Lead Thin Shrink Small Outline (TSSOP) (RU-16)



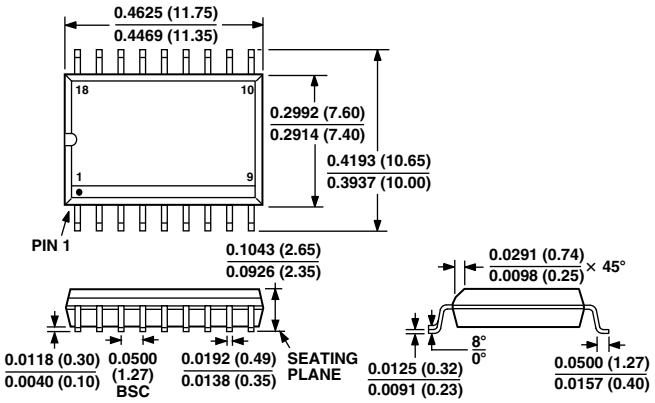
16-Lead Wide Body SOIC (R-16)



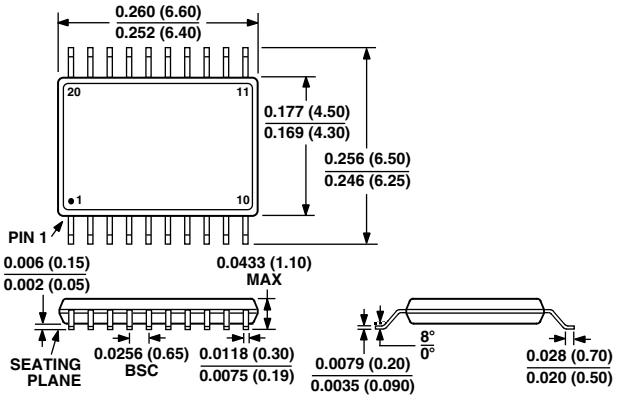
18-Lead Plastic DIP
(N-18)



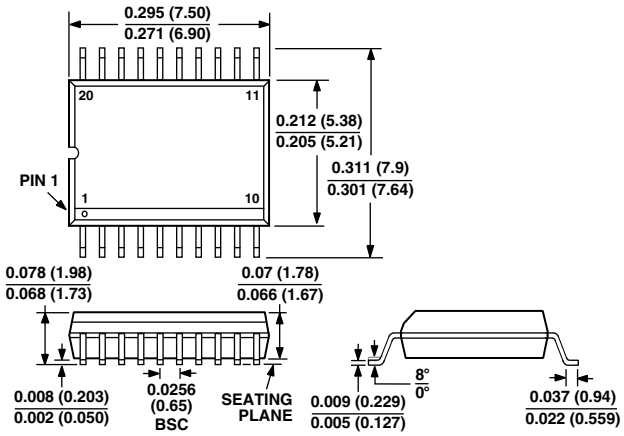
18-Lead Wide Body SOIC
(R-18)



20-Lead Thin Shrink Small Outline (TSSOP)
(RU-20)



20-Lead Shrink Small Outline (SSOP)
(RS-20)



Revision History

Location	Page
11/01—Data Sheet changed from REV. A to REV. B.	
Changes to Specifications page	2

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