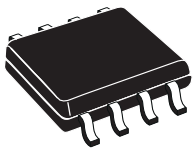
STS5NS150

N-CHANNEL 150V - 0.075 Ω - 5A SO-8
LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS5NS150	150 V	<0.1 Ω	5 A

- TYPICAL $R_{DS}(on)$ = 0.075 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION



SO-8

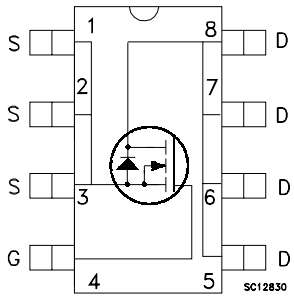
DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	150	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	150	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	5	A
I_D	Drain Current (continuous) at T_C = 100°C	3	A
I_{DM}(•)	Drain Current (pulsed)	20	A
P_{tot}	Total Dissipation at T_C = 25°C	2.5	W
	Derating Factor	0.02	W/°C
T_{stg}	Storage Temperature	-55 to 150	°C
T_j	Operating Junction Temperature		

(•) Pulse width limited by safe operating area.

THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient	Max	50	°C/W

(*) When mounted on FR-4 board with 0.5 in2 pad of Cu.

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	500	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	150			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 2.5 A		0.075	0.1	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, V_{GS} = 4 V		5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		990 175 110		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 75 V I_D = 2.5 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 1)		12 2.8		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 120V I_D= 5A V_{GS}= 10V (see test circuit, Figure 2)		65 5.5 2.7		nC nC nC

SWITCHING OFF

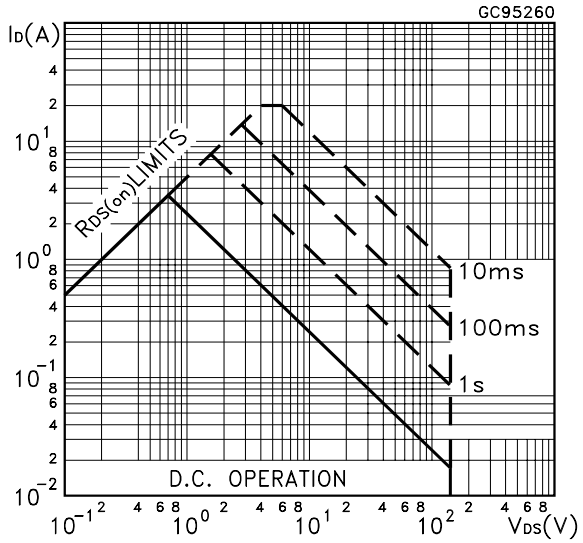
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 75 V I_D = 2.5 A R_G = 4.7Ω, V_{GS} = 10 V (Resistive Load, Figure 1)		50 12		ns ns
$t_{r(Voff)}$ t_f t_c	Turn-off Delay Time Fall Time Cross-over Time	V_{clamp} = 120 V I_D = 5 A R_G = 4.7Ω, V_{GS} = 10 V (Inductive Load, Figure 5)		11 17 36		ns ns ns

SOURCE DRAIN DIODE

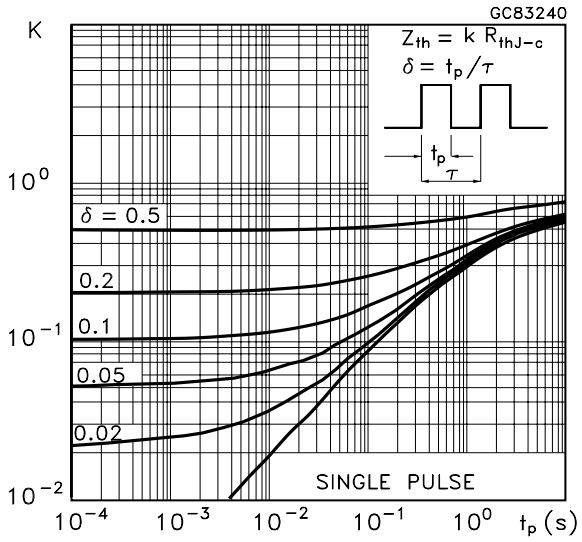
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				5 20	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 5 A V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 5 A di/dt = 100A/µs V_{DD} = 30 V T_j = 150°C (see test circuit, Figure 3)		150 712 9.5		ns nC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

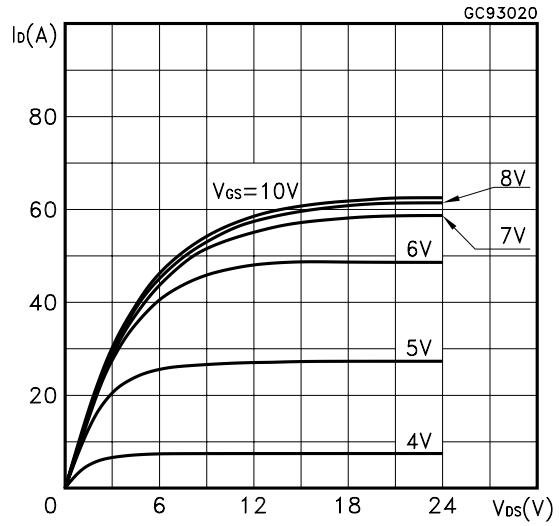
Safe Operating Area



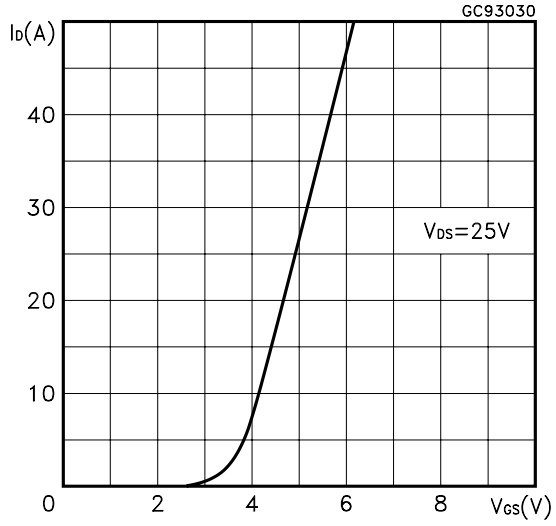
Thermal Impedance



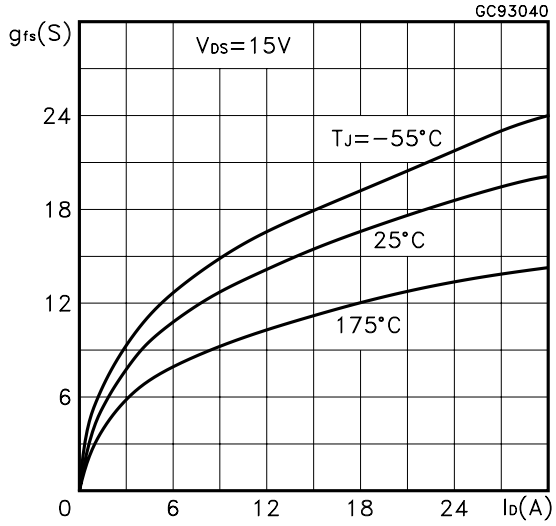
Output Characteristics



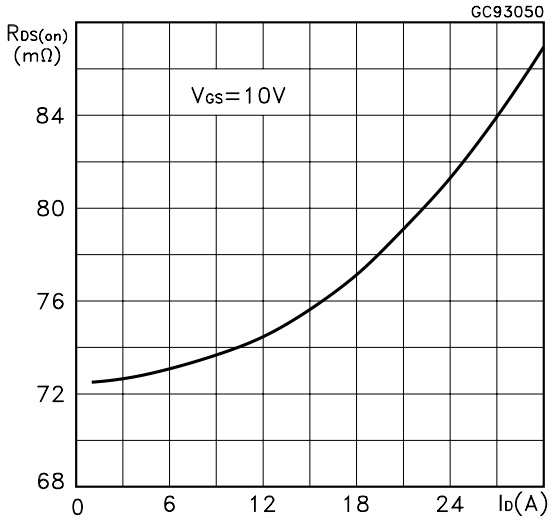
Transfer Characteristics



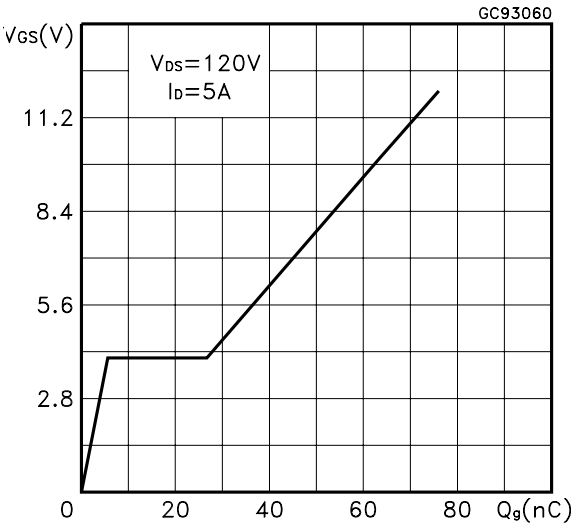
Transconductance



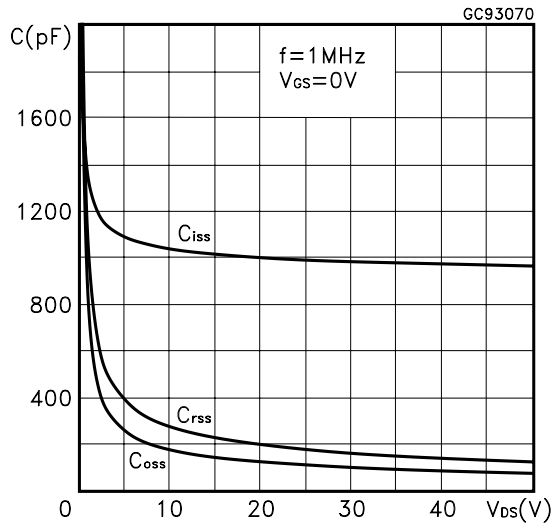
Static Drain-source On Resistance



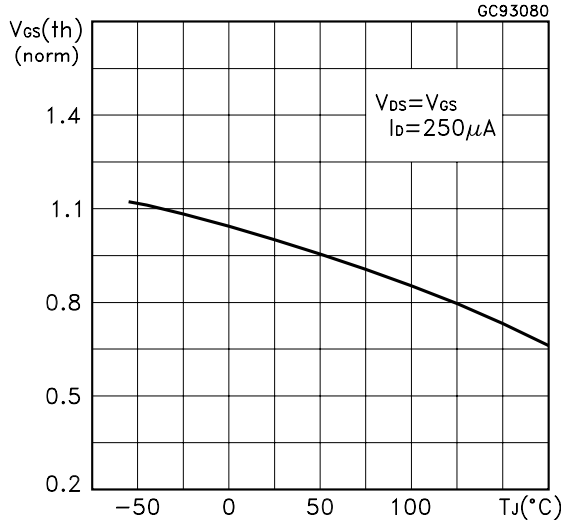
Gate Charge vs Gate-source Voltage



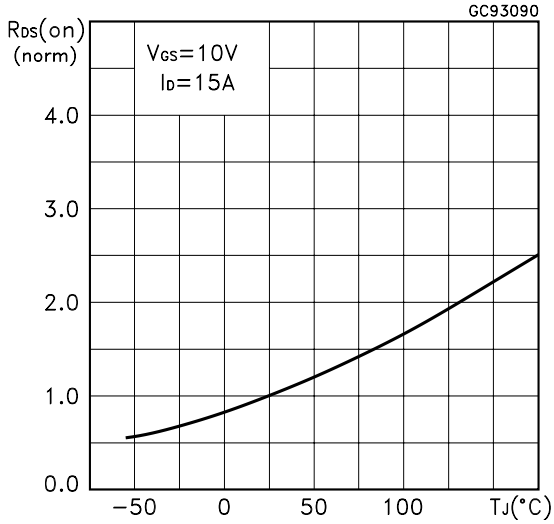
Capacitance Variations



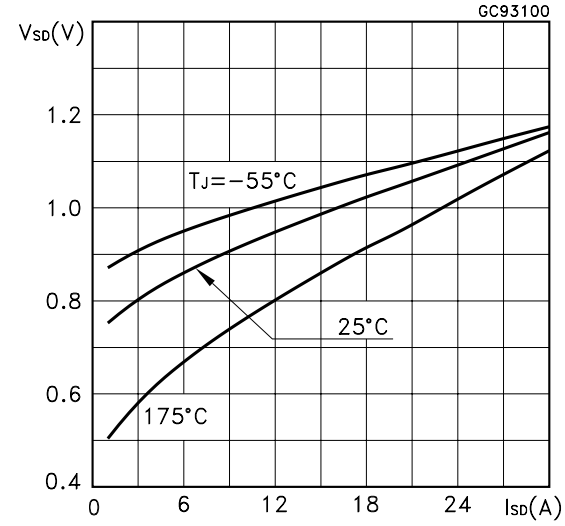
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage Temperature

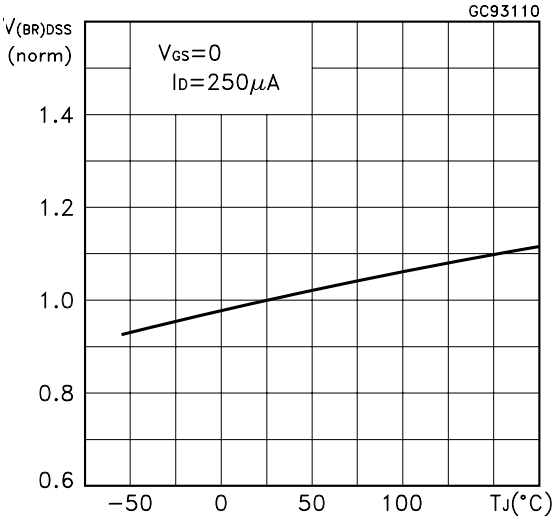


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Fig. 1: Switching Times Test Circuits For Resistive Load

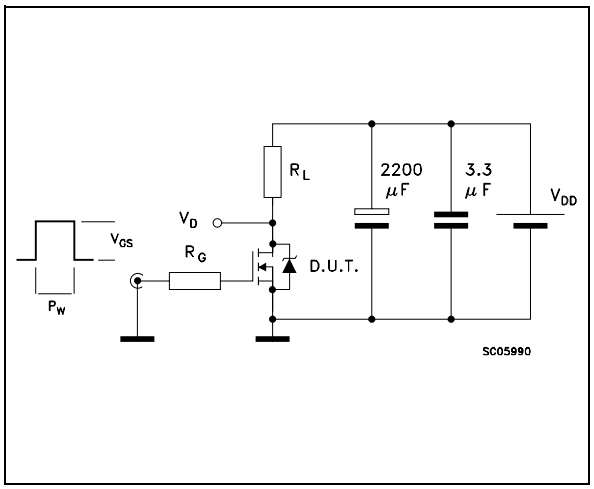


Fig. 2: Gate Charge test Circuit

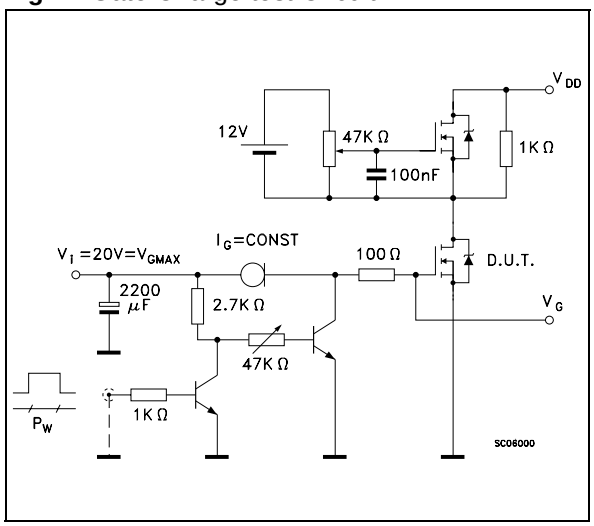
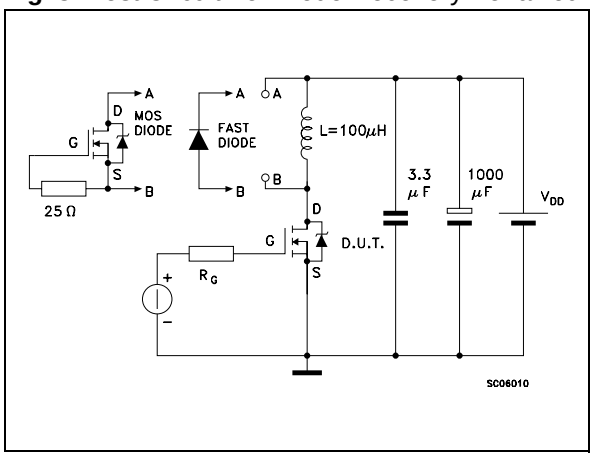
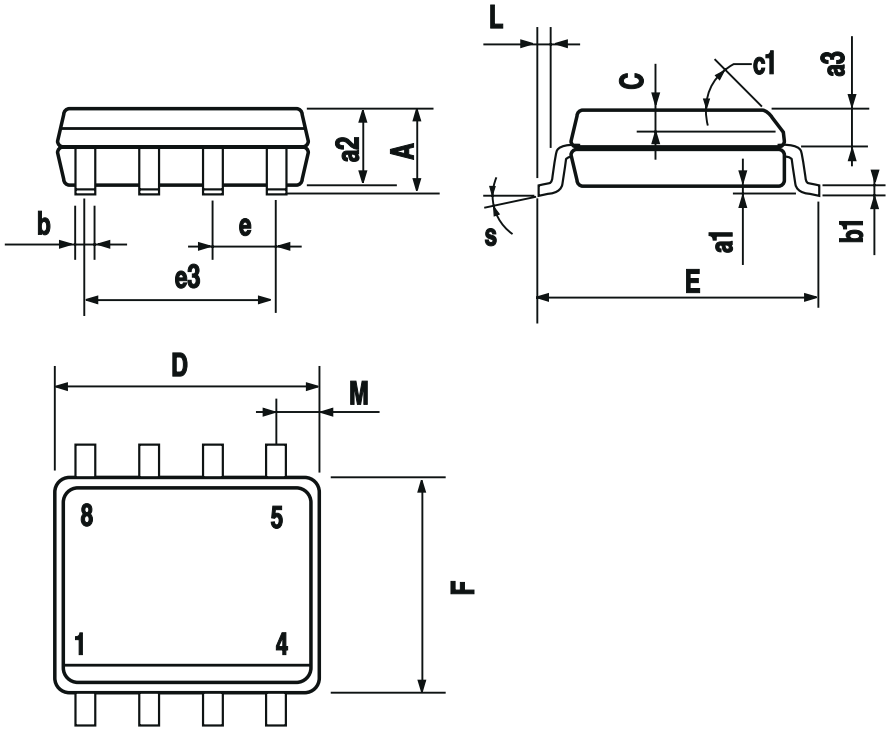


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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