ANALOG DEVICES

Integrated Synthesizer and VCO

Preliminary Technical Data — ADF4360

FEATURES

Six Output Ranges:
- 2000 MHz to 2550 MHz
- 1700 MHz to 2150 MHz
- 1600 MHz to 1950 MHz
- 1400 MHz to 1800 MHz
- 1150 MHz to 1400 MHz
- 1000 MHz to 1250 MHz
- External L for Lower Frequencies

Divide-by-2 output
+2.7 V to +3.3V Power Supply
1.8 V Logic Compatibility
Integer-N Synthesizer
Programmable Dual Modulus Prescaler
8/9, 16/17, 32/33
Programmable Output Power Level
Programmable Core Power Level
3-Wire Serial Interface
Analog and Digital Lock Detect
Hardware and Software Power Down Mode

APPLICATIONS

Wireless Handsets (DECT, GSM, PCS, DCS, WCDMA)
Test Equipment
Wireless LANS
CATV Equipment

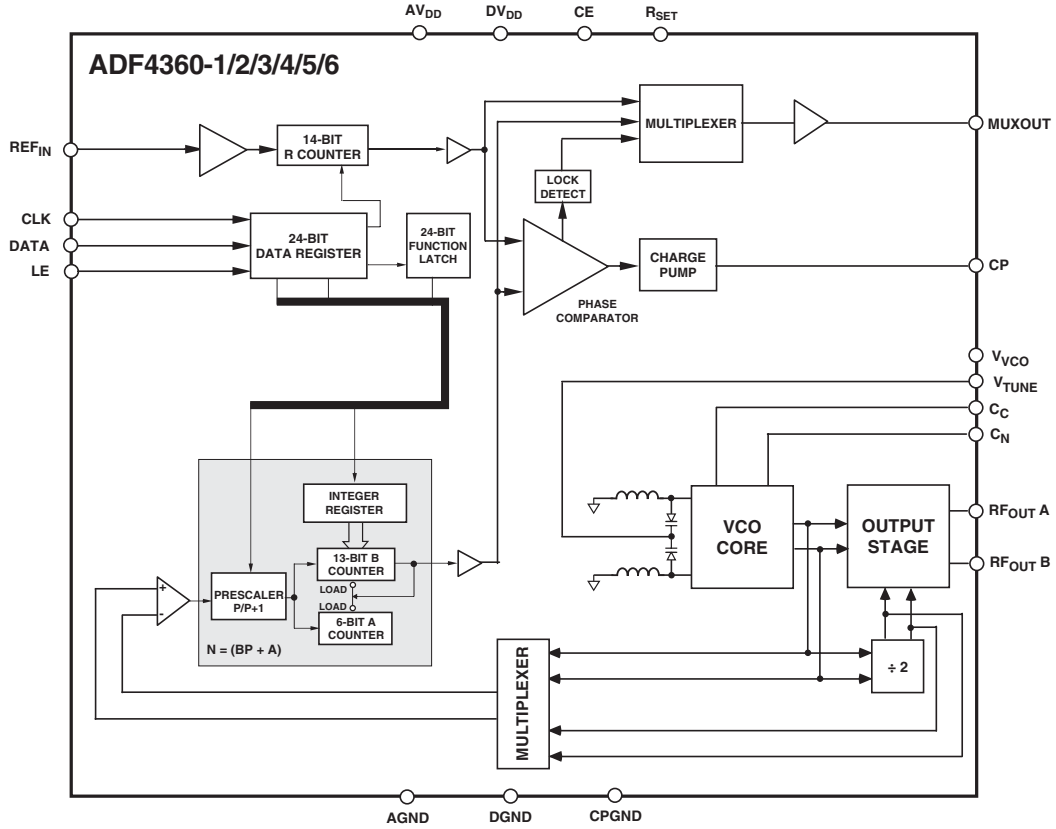
GENERAL DESCRIPTION

The ADF4360 family is a fully integrated integer-N synthesizer and voltage controlled oscillator (VCO). The user has the choice of seven output frequency ranges; the ADF4360-1 is designed for a center frequency of 2400MHz, the ADF4360-2 for 2000MHz, the ADF4360-3 for 1800 MHz, the ADF4360-4 for 1600MHz, the ADF4360-5 for 1300MHz and the ADF4360-6 for 1150 MHz. The ADF4360-7 center frequency is set by external inductors.

In addition, there is a divide-by-2 option available, whereby the user gets an RF output center frequency of either 1200MHz (ADF4360-1), 1000MHz (ADF4360-2), 900 MHz (ADF4360-3) etc.

Control of all the on-chip registers is via a simple 3-wire interface. The device operates with a power supply ranging from 2.7V to 3.3V and can be powered down when not in use.

ADF4360-1/2/3/4/5/6 FUNCTIONAL BLOCK DIAGRAM



REV. PrP 01/03

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ADF4360–SPECIFICATIONS[1]

(AV_{DD} = DV_{DD} = V_{VCO} = +3V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version	B Chips[2] (Typical)	Units	Test Conditions/Comments
REFIN CHARACTERISTICS				
REFIN Input Frequency	10/100	10/100	MHz min/max	For f < 10MHz, use dc-coupled CMOS compatible square wave
REFIN Input Sensitivity[3] 0 to V_{DD} max	-5/0	-5/0	dBm min/max	AC coupled. (CMOS compatible)
REFIN Input Capacitance	10	10	pF max	
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[4]	1	1	MHz max	
CHARGE PUMP				
I_{CP} sink/source[5]				With R_{SET} = 4.7kΩ
High Value	2.5	2.5	mA typ	
Low Value	0.312	0.312	mA typ	
R_{SET} Range	2.7/10	2.7/10	kΩ typ	
I_{CP} 3-State Leakage Current	1	1	nA typ	
Sink and Source Current Matching	2	2	% typ	0.5V ≤ V_{CP} ≤ V_P - 0.5
I_{CP} vs. V_{CP}	1.5	1.5	% typ	0.5V ≤ V_{CP} ≤ V_P - 0.5
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = V_P/2
RF OUTPUT CHARACTERISTICS				
VCO Output Frequency				
ADF4360-1	2000/2550	2000/2550	MHz min/max	Center Frequency: 2250MHz
ADF4360-2	1700/2150	1700/2150	MHz min/max	Center Frequency: 2000MHz
ADF4360-3	1600/1950	1600/1950	MHz min/max	Center Frequency: 1800MHz
ADF4360-4	1400/1800	1400/1800	MHz min/max	Center Frequency: 1600MHz
ADF4360-5	1150/1400	1150/1400	MHz min/max	Center Frequency: 1300MHz
ADF4360-6	1000/1250	1000/1250	MHz min/max	Center Frequency: 1150MHz
ADF4360-7	TBD	TBD	MHz min/max	
VCO Sensitivity ADF4360-1/2	60	60	MHz/Volt typ	Fundamental Frequency Selected
ADF4360-3/4	50	50		
ADF4360-5/6	40	40		
				30/25/20 with Divide by two selected
Frequency Pushing	4	4	MHz/Volt typ	
Frequency Pulling	200	200	kHz typ	Into 2.00 VSWR Load
Harmonic Content	-10	-10	dBc typ	
VCO Output Power Range	-12/-3	-12/-3	dBm min/max	Programmable in 3dB steps.Table X
VCO Tuning Range	1.5/2.5	1.5/2.5	V min/max	
LOGIC INPUTS				
V_{INH}, Input High Voltage	1.35	1.35	V min	
V_{INL}, Input Low Voltage	0.6	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	DV_{DD}-0.4	V_{DD}-0.4	V min	Open drain output chosen. 1kΩ pull-up to 1.8V
V_{OH}, Output High Voltage	DV_{DD}-0.4	V_{DD}-0.4	V min	CMOS output chosen
I_{OH}	500	500	µA max	
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500µA
POWER SUPPLIES				
AV_{DD}	2.7/3.3	2.7/3.3	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
I_{DD}[6] (AI_{DD} + DI_{DD})	9.0	9.0	mA	VCO core power level is
I_{VCO}	10-28	10.0-28.0	mA	programmable; as is the RF Output
I_{RFOUT}	3.5-11.0	3.5-11.0	mA	Stage
Low Power Sleep Mode	5	5	µA typ	

NOTES
1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. Only the ADF4360-7 is offered in die (chip) form. The B Chip specifications are given as typical values.
3. AV_{DD} = DV_{DD} = V_{VCO} = 3V
4. Guaranteed by design. Sample tested to ensure compliance.
5. I_{CP} is internally modified to maintain constant loop gain over the frequency range
6. T_A = +25°C; AV_{DD} = DV_{DD} = V_{VCO} = 3V; P = 16

ADF4360–SPECIFICATIONS[1]

(AV_{DD} = DV_{DD} = V_{VCO} = +3V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B	Units	Test Conditions/Comments
NOISE CHARACTERISTICS			
Synthesizer Phase Noise Floor[2]	-171	dBc/Hz typ	@ 25kHz PFD Frequency
	-164	dBc/Hz typ	@ 200kHz PFD Frequency
VCO Phase Noise Performance	-130	dBc/Hz typ	@ 800kHz offset from carrier
	-141	dBc/Hz typ	@ 3MHz Offset from carrier
Output Phase Noise Performance[3]			@ VCO Output
2250 MHz output[4]	-80	dBc/Hz typ	ADF4360-1
2000 MHz output[5]	-83	dBc/Hz typ	ADF4360-2
1800 MHz output[6]	-84	dBc/Hz typ	ADF4360-3
1600 MHz output[7]	-84	dBc/Hz typ	ADF4360-4
1300 MHz output[8]	-85	dBc/Hz typ	ADF4360-5
1150 MHz output[9]	-85	dBc/Hz typ	ADF4360-6
Spurious Signals			
2250MHz output[4]	-70/-72	dBc typ	ADF4360-1
2000MHz output[5]	-70/-72	dBc typ	ADF4360-2
1800MHz output[6]	-70/-72	dBc typ	ADF4360-3
1600MHz output[7]	-70/-72	dBc typ	ADF4360-4
1300MHz output[8]	-70/-72	dBc typ	ADF4360-5
1150 MHz output[9]	-70/-72	dBc typ	ADF4360-6

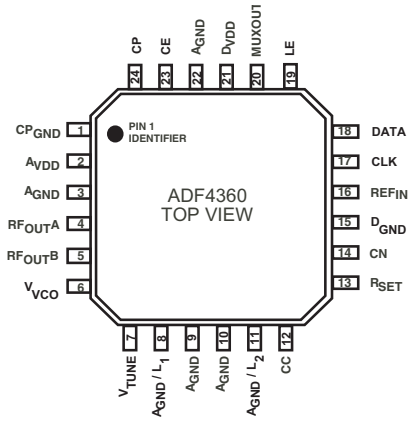
NOTES
1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value).
3. The phase noise is measured with the EVAL-ADF4360EBX Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10MHz @ 0dBm).
4. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; N = 11250; Loop B/W = 10kHz
5. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; N = 10000; Loop B/W = 10kHz
6. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; N = 9000; Loop B/W = 10kHz
7. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; N = 8000; Loop B/W = 10kHz
8. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; N = 6500; Loop B/W = 10kHz
9. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; N = 5750; Loop B/W = 10kHz

ORDERING GUIDE

Model	Temperature Range	Frequency Range	Package Option*
ADF4360-1BCP	–40°C to +85°C	2000-2550 MHz	CP-24
ADF4360-2BCP	–40°C to +85°C	1700-2150 MHz	CP-24
ADF4360-3BCP	–40°C to +85°C	1600-1950 MHz	CP-24
ADF4360-4BCP	–40°C to +85°C	1400-1800 MHz	CP-24
ADF4360-5BCP	–40°C to +85°C	1150-1400 MHz	CP-24
ADF4360-6BCP	–40°C to +85°C	1000-1250 MHz	CP-24
ADF4360-7BCP	–40°C to +85°C	Set By External L	CP-24

* CP = Chip Scale Package
Contact the factory for chip availability

PIN CONFIGURATION
TOP VIEW



TIMING CHARACTERISTICS

(AV_{DD} = DV_{DD} = V_{VCO} = +3V ± 10%; AGND = DGND = 0 V; 1.8V and 3V Logic Levels Used; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Set Up Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Set Up Time
t_6	20	ns min	LE Pulse Width

NOTE
Guaranteed by Design but not Production Tested.

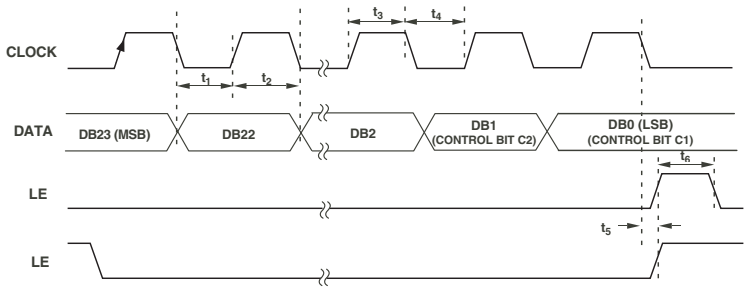


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

AV_{DD} to GND[3] .....–0.3 V to +3.6 V
AV_{DD} to DV_{DD} .....–0.3 V to +0.3 V
V_P to GND.....–0.3 V to +3.6 V
V_{VCO} to GND.....–0.3 V to +3.6 V
V_{VCO} to AV_{DD} .....–0.3 V to +0.3 V
Digital I/O Voltage to GND.....–0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND.....–0.3 V to V_{DD} + 0.3 V
REF_{IN}, to GND.....–0.3 V to V_{DD} + 0.3 V
OperatingTemperature Range
Industrial (B Version).....–40°C to +85°C
Maximum Junction Temperature.....+150°C
CSP θ_{JA} Thermal Impedance
(Paddle Soldered).....50°C/W
(Paddle Not Soldered).....88°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec).....+215°C
Infrared (15 sec).....+220°C

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. This device is a high-performance RF integrated circuit with an ESD rating of < 2kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

3. GND = AGND = DGND = 0V

TRANSISTOR COUNT

TBA (CMOS) and TBA (Bipolar)

CAUTION

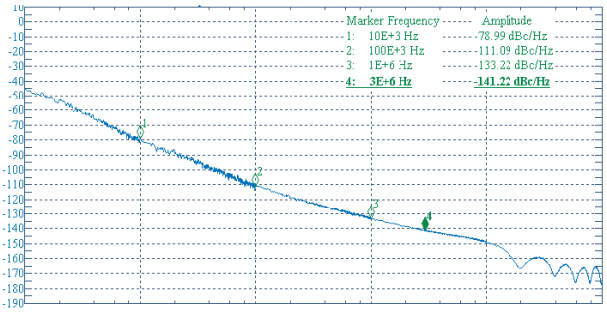
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF4360 family features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

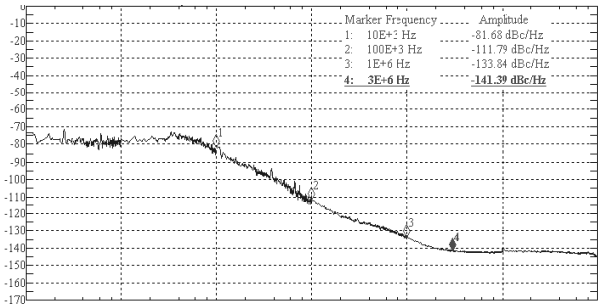
Mnemonic	Function
AV_{DD}	Analog Power Supply. This may range from 2.7V to 3.3V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
DV_{DD}	Digital Power Supply. This may range from 2.7V to 3.3V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current for the synthesizer. The nominal voltage potential at the R_{SET} pin is 0.6V. The relationship between I_{CP} and R_{SET} is $$I_{CPmax} = \frac{11.75}{R_{SET}}$$ So, with R_{SET} = 4.7kΩ, I_{CPmax} = 2.5mA.
MUXOUT	This multiplexer output allows either the Lock Detect, the scaled RF or the scaled Reference Frequency to be accessed externally.
CP	Charge Pump Output. When enabled this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the internal VCO.
V_{VCO}	Power supply for the VCO. This may range from 2.7V to 3.3V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. V_{VCO} must be the same value as AV_{DD}.
V_{TUNE}	Control input to the VCO. This voltage determines the output frequency and is derived from filtering the CP_{OUT} voltage.
L1	ADF4360-7 only. An external inductor should be connected to this pin to set the ADF4360-7 output frequency.
L2	ADF4360-7 only. An external inductor should be connected to this pin to set the ADF4360-7 output frequency.
C_C	Internal compensation node. This pin must be decoupled to ground with a 10nF capacitor.
C_N	Internal compensation node. This pin must be decoupled to V_{VCO} with a 10uF capacitor.
$RF_{OUT}A$	VCO output. The output level is programmable from -3dBm to -12dBm.
$RF_{OUT}B$	VCO complementary output. The output level is programmable from -3dBm to -12dBm.
CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
DGND	Digital Ground.
AGND	Analog Ground. This is the ground return path of the prescaler & VCO.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three state mode. Taking the pin high will power up the device depending on the status of the power-down bits.
REFIN	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100kΩ. See Figure 2. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac coupled.

ADF4360

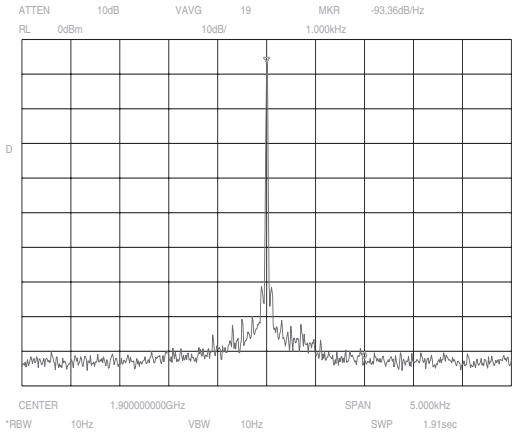
Typical Performance Characteristics



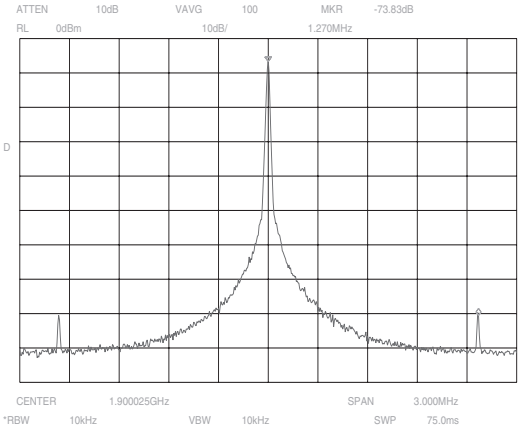
TPC 1. VCO Phase Noise (Unlocked)



TPC 2. VCO Phase Noise (Locked)



TPC 3. Close-In Phase Noise at 1900MHz (1.25MHz Channel Spacing)



TPC 4. Reference Spurs at 1900MHz (1.25MHz Channel Spacing)

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The Reference Input stage is shown below in Figure 2. SW1 and SW2 are normally-closed switches. SW3 is normally-open. When Powerdown is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on powerdown.

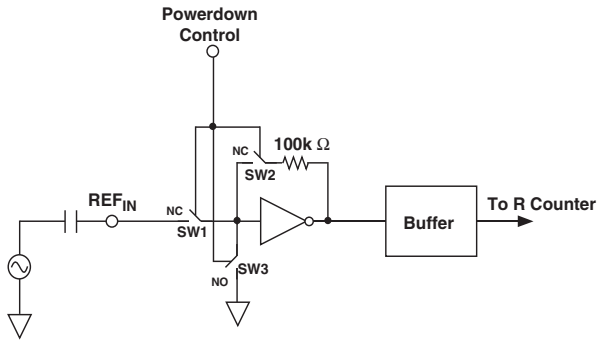


Figure 2. Reference Input Stage

PRESCALER (P/P+1)

The dual modulus prescaler (P/P+1), along with the A and B counters, enables the large division ratio, N, to be realised (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the VCO and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17 or 32/33. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value and is given by: (P^2-P).

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300MHz or less. Thus, with an VCO frequency of 2.5GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R . The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO} Ouput Frequency of voltage controlled oscillator (VCO).

P Preset modulus of dual modulus prescaler (8/9, 16/17, etc.,).

B Preset Divide Ratio of binary 13-bit counter (3 to 8191).

A Preset Divide Ratio of binary 6-bit swallow counter (0 to 31).

f_{REFIN} External reference frequency oscillator.

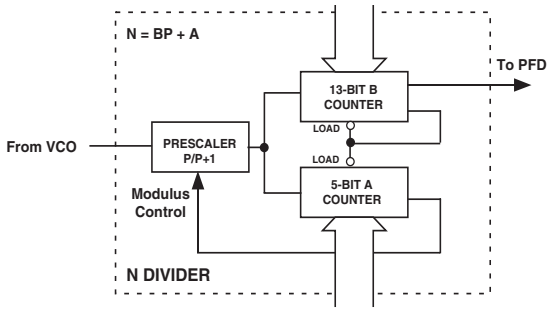


Figure 4. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N=BP+A) and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic. The PFD includes a programmable delay element which controls the width of the anti-backlash pulse. This pulse ensures that there is no deadzone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the R Counter Latch, ABP2 and ABP1 control the width of the pulse. See Table 3.

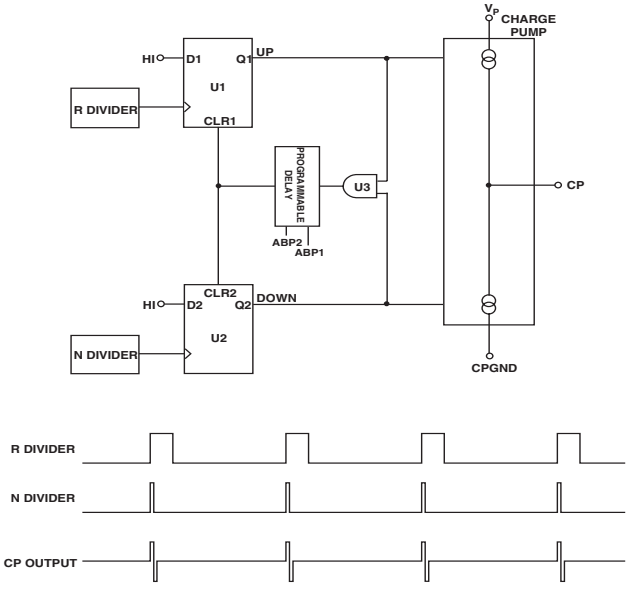


Figure 5. PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4360 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2 and M1 in the Function Latch. Table 5 shows the full truth table. Figure 6 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect
Digital lock detect is active high. When LDP in the R Counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive Phase Detector cycles is less than 15ns.

With LDP set to "1", five consecutive cycles of less than 15ns are required to set the lock detect. It will stay set high until a phase error of greater than 25ns is detected on any subsequent PD cycle.
The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10kΩ nominal. When lock has been detected this output will be high with narrow low-going pulses .

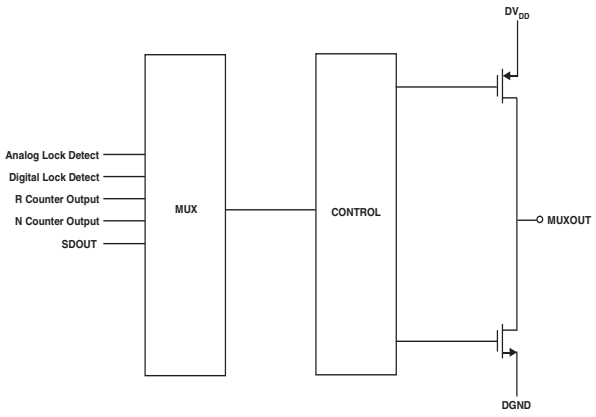


Figure 6. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4360 family's digital section includes a 24-bit input shift register, a 14-bit R counter and a 19-bit N counter, comprising a 5-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two lsb's DB1, DB0 as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table 6. Table 1 shows a summary of how the latches are programmed.

Table I. C2, C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	Control Latch
0	1	R Counter
1	0	N Counter (A & B)
1	1	Test Modes Latch

VCO

The VCO core in the ADF4360 family uses eight overlapping bands as shown in figure 7 to allow a wide frequency range to be covered without a large VCO sensitivity (Kv) and resultant poor phase noise and spurious performance.

The correct band is chosen automatically by the band select logic at power-up or whenever the N Counter latch is updated. It is important that the correct write sequence be followed at power-up. This sequence is:

1) R Counter latch

2) Control latch

3) N Counter latch

During band select, which takes five PFD cycles, The VCO Vtune is disconnected from the output of the loop filter and connected to an internal reference voltage.

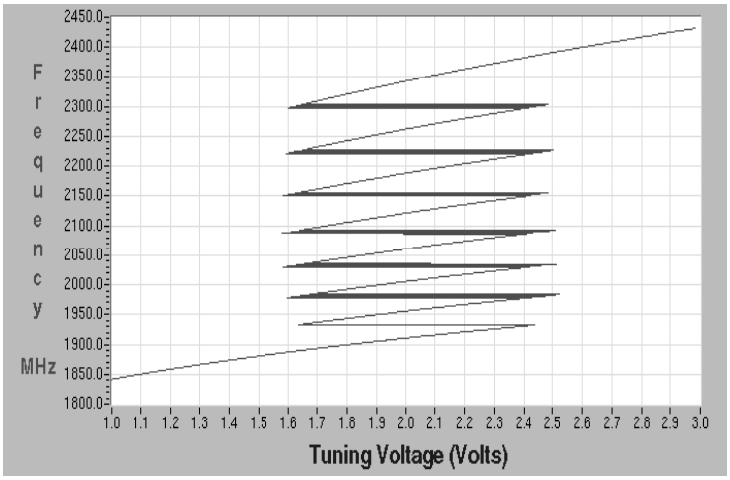


Figure 7 Band Select vs Vtune

The R Counter output is used as the clock for the band select logic and should not exceed 250 kHz. A programmable divider is provided at the R Counter input to allow division by 1,2,4 or 8, and is controlled by bits BSC1 and BSC2 in the R Counter Latch. Where the required PFD frequency exceeds 250 kHz the divide ratio should be set to allow enough time for correct band selection.

After band select, normal PLL action resumes. The nominal value of Kv is 75MHz/Volt (for the ADF4360-1/2) or 37.5MHZ/Volt if divide by two operation has been selected (by programming DIVSEL high in the N Counter latch). The ADF4360 family contains linearisation circuitry to minimise any variation of the product of Icp and Kv.

The Phase Noise of the VCO is best at high power levels. To allow the user to optimise this noise-power trade off depending on his/her requirements. The operating current in the VCO core is programmable in four steps, 5mA, 10mA, 15mA & 20mA. This is controlled by bits PC1 & PC2 in the Control latch.

OUTPUT STAGE

The RFoutA and RFoutB pins of the ADF4360 family are connected to the collectors of an NPN differential pair driven by buffered outputs of the VCO. To allow the user to optimise his/her power dissipation vs output power requirements, The tail current of the differential pair is programmable via bits PL1 & PL2 in the Control latch. Four current levels may be set; 3mA, 4.5mA, 6.5mA and 9.5mA giving output power levels of -3dBm, -6dBm, -9dBm & -12dBm into a 50ohm load. Alternatively, both outputs can be combined in a 1+1:1 transformer or a 180° microstrip coupler.

Another feature of the ADF4360 family is provided whereby the supply current to the RF output stage is shut down until the part achieves lock as measured by the Digital Lock detect circuitry. This is enabled by the MTLD (Mute Till Lock Detect) bit in the Control latch.

ADF4360

LATCH STRUCTURE

The diagram below shows the four on-chip latches for the ADF4360 family. The two LSB's decide which latch is programmed.

Control Latch

Prescaler Value		Power Down 2	Power Down 1	Current Setting 2			Current Setting 1			Output Power Level		Mute Till LD	CP Gain	CP 3-State	Phase Detector Polarity	MUXOUT Control			Counter Reset	Core Power Level		Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	M3	M2	M1	CR	PC2	PC1	C2 (0)	C1 (0)

N Counter Latch

Divide by 2 Select	Divide by 2	CP Gain	13-Bit B Counter													Reserved	5-Bit A Counter					Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DIVSEL	DIV2	CPG	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	RSV7	A5	A4	A3	A2	A1	C2 (1)	C1 (0)

R Counter Latch

Reserved		Band Select Clock		Test Mode Bit	Lock Detect Precision	Anti Backlash Width		14-Bit Reference Counter, R														Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSV6	RSV5	BSC2	BSC1	TMB	LDP	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (1)

CONTROL LATCH
With (C2, C1) = (0,0), the Control Latch is programmed.

Control Latch

Prescaler Value		Power Down 2	Power Down 1	Current Setting 2			Current Setting 1			Output Power Level		Mute Till LD	CP Gain	CP 3-State	Phase Detector Polarity	MUXOUT Control			Counter Reset	Core Power Level		Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	M3	M2	M1	CR	PC2	PC1	C2 (0)	C1 (0)

Prescaler Value
In the ADF4360 family, P2 and P1 in the Control Latch set the prescaler values.

P2	P1	Prescaler Value
0	0	8/9
0	1	16/17
1	0	32/33
1	1	32/33

Power Down
DB21 (PD2) and DB20 (PD1) provide programmable power-down modes.

In the programmed asynchronous power-down, the device powers down immediately after latching a "1" into bit PD1, with the condition that PD2 has been loaded with a "0".
In the programmed synchronous power-down, the device power down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a "1" into bit PD1 (on condition that a "1" has also been loaded to PD2), then the device will go into power-down on the second rising edge of the R counter output, after LE goes high.

When a power down is activated (either synchronous or asynchronous mode), the following events occur:

All active DC current paths are removed.

The R, N and timeout counters are forced to their load state conditions.

The charge pump is forced into three-state mode.

The digital clock detect circuitry is reset.

The RF_{IN} input is debiased to a high impedance state.

The reference input buffer circuitry is disabled.

The input register remains active and capable of loading and latching data.

PD2	PD1	Mode
X	0	Normal Operation
0	1	Asynchronous Power-Down
1	1	Synchronous Power-Down

Control Latch

Prescaler Value		Power Down 2	Power Down 1	Current Setting 2			Current Setting 1			Output Power Level		Mute Till LD	CP Gain	CP 3-State	Phase Detector Polarity	MUXOUT Control			Counter Reset	Core Power Level		Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	M3	M2	M1	CR	PC2	PC1	C2 (0)	C1 (0)

Charge Pump Currents
CPI3, CPI2, CPI1 in the ADF4360 family determine Current Setting 1. CPI6, CPI5, CPI4 determine Current Setting 2. The truth table is given below.

CPI6 CPI3	CPI5 CPI2	CPI4 CPI1	I_{CP}
0	0	0	0.31 mA
0	0	1	0.62 mA
0	1	0	0.93 mA
0	1	1	1.25 mA
1	0	0	1.56 mA
1	0	1	1.87 mA
1	1	0	2.18 mA
1	1	1	2.50 mA

Output Power Level
The output power level of the VCO is set by these bits

PL2	PL1	Output Power Level (dBm into 50 ohm)
0	0	-12
0	1	-9
1	0	-6
1	1	-3

Mute Till Lock Detect
DB11 of the Control Latch in the ADF4360 family is the Mute Till Lock Detect Bit. When this is programmed to a "1", the RF output is disabled until digital lock detect goes high.

CP Gain Bit
DB10 of the Control Latch in the ADF4360 family is the Charge Pump Gain bit. When this is programmed to a "1" then Current Setting 2 is used. When programmed to a "0", Current Setting 1 is used.

Charge Pump Three-State
This bit puts the charge pump into three-state mode when programmed to a "1". It should be set to "0" for normal operation.

Phase Detector Polarity
The PDP bit in the ADF4360 family sets the Phase Detector Polarity. When the VCO characteristics are positive this should be set to "1". This is the normal setting when using the on-chip VCO, with a passive loop filter or an active non-inverting filter. It can also be set to "0". This is required if an active inverting loop filter is used.

Control Latch

Prescaler Value		Power Down 2	Power Down 1	Current Setting 2			Current Setting 1			Output Power Level		Mute Till LD	CP Gain	CP 3-State	Phase Detector Polarity	MUXOUT Control			Counter Reset	Core Power Level		Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	M3	M2	M1	CR	PC2	PC1	C2 (0)	C1 (0)

MUXOUT Control
The on-chip multiplexer is controlled by M3, M2, M1.

M3	M2	M1	MUXOUT
0	0	0	Three-State Output
0	0	1	Digital Lock Detect
0	1	0	N Divider Output
0	1	1	DV_{DD}
1	0	0	R Divider Output
1	0	1	N-Channel Open Drain Lock Detect
1	1	0	Serial Data Output
1	1	1	DGND

Counter Reset
DB4 is the counter reset bit for the ADF4360 family. When this is "1", the R counter and the A,B counters are reset. For normal operation this bit should be "0".

Core Power Level
PC1 and PC2 set the power level in the core.

PC2	PC1	Core Power Level
0	0	5mA
0	1	10mA
1	0	15mA
1	1	20mA

R COUNTER LATCH
With (C2, C1) = (0,1), the R CounterLatch is programmed.

R Counter Latch

Reserved		Band Select Clock		Test Mode Bit	Lock Detect Precision	Anti Backlash Width		14-Bit Reference Counter, R														Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSV6	RSV5	BSC2	BSC1	TMB	LDP	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (1)

R Counter
R1 to R14 sets the counter divide ratio. The divide range is 1 (00.....001) to 16383 (111.....111).

Anti-Backlash Pulse Width
DB16 and DB17 set the anti-backlash pulse width.

ABP2	ABP1	Anti-Backlash Pulse Width
0	0	3.0ns
0	1	1.5ns
1	0	6.0ns
1	1	3.0ns

Lock Detect Precision Bit
DB18 is the Lock Detect Precision Bit and sets the number of references cycles for entering the locked state. With LDP at "1", 5 cycles are taken and with LDP at "0", 3 cycles are taken.

Test Mode Bit
DB19 is the Test Mode Bit (TMB).
With TMB = 0, the contents of the Test Mode Latch are ignored and normal operation occurs as determined by the contents of the Control Latch, R Counter Latch and N Counter Latch. External Band Select = 0, Band Control of ICP = 1, and SAR control of ICP = 1. This is normal operation.
With TMB = 1, the contents of the Test Mode Latch are enabled and will control the mode of operation. These are defined in the Test Modes Latch.

Band Select Clock Bits
These Bits set a divider for the band select logic clock input, The output of the R Counter is by default the value used to clock the band select logic, but if this value is too high (>250kHz), a divider can be switched in to divide the R counter output to a smaller value.

BSC2	BSC1	Band Select Clock Divider Value
0	0	1
0	1	2
1	0	4
1	1	8

Reserved Bits
DB23 - DB22 are spare bits and have been designated as "Reserved".

A,B COUNTER LATCH
With (C2, C1) = (1,0), the A, B Counters Latch is programmed.

N Counter Latch

Divide by 2 Select	Divide by 2	CP Gain	13-Bit B Counter													Reserved	5-Bit A Counter					Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DIVSEL	DIV2	CPG	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	RSV7	A5	A4	A3	A2	A1	C2 (1)	C1 (0)

A Counter Latch
A5 - A1 program the 5-bit A counter. The divide range is 0 (00000) to 31 (11111).

B Counter Latch
B13 - B1 program the B counter. The divide range here is 3 (00.....0011) to 8191 (11....111).

Overall Divide Range
The overall divide range is defined by ((PxB) + A), where P is the prescaler value.

CP Gain Bit
DB21 of the N Counter Latch in the ADF4360 family is the Charge Pump Gain bit. When this is programmed to a "1" then Current Setting 2 is used. When programmed to a "0", Current Setting 1 is used. This bit can also be programmed via DB10 of the Control Latch. The bit will always reflect the latest value written to it, whether this is through the Control Latch or the N Counter Latch.

Divide by 2
DB22 is the divide-by-2 bit. When set to a "1", the output divide by 2 function is chosen. When it is set to "0", normal operation occurs.

Divide by 2 Select
DB23 is the divide-by-2 select bit. When this is programmed to a "1", the divide-by-2 output is selected as the prescaler input. When it is set to a "0", the fundamental is used as the prescaler input.

POWER UP CONDITIONS

On power-up, Reset Bit stays low and CPI 3-State stays high until a valid Control write, R write and N write have been completed. The device comes up in power-down mode and stays in this mode until the valid writes have been completed.

PUTTING THE CHARGE PUMP INTO 3-STATE

Three conditions can potentially three-state the charge pump.

a) The initialisation sequences (reset counters cp -> tri-state).
b) The CP 3-State bit in the function latch

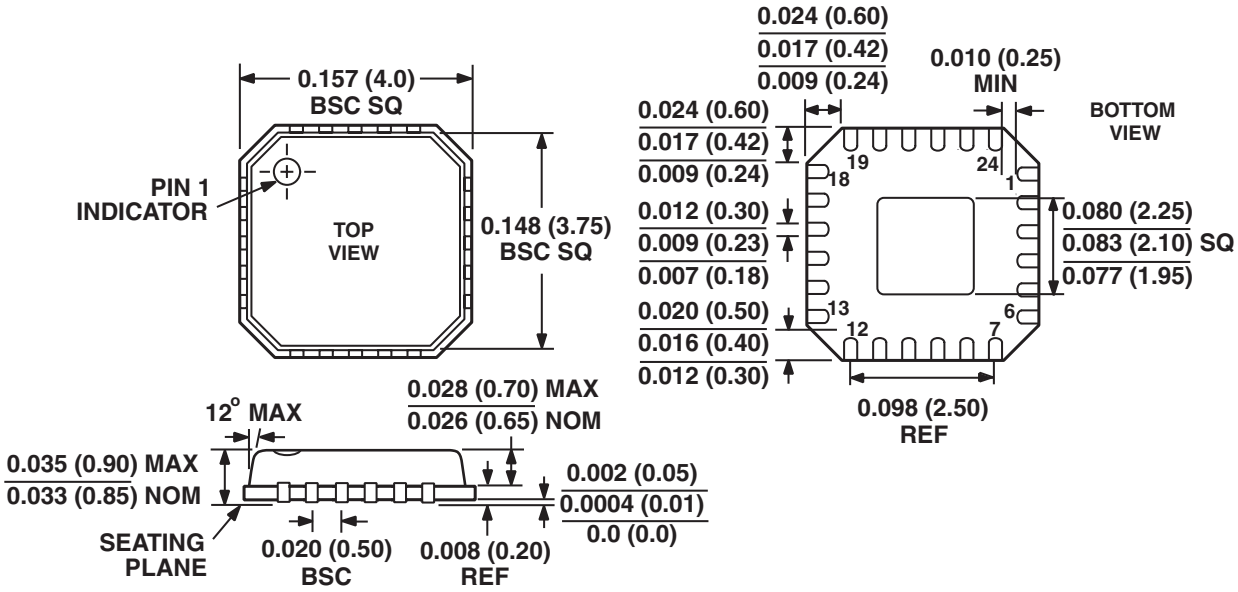
Note that a) takes priority over b).

That is to say:

- If CP is tri-state due to an initialialisation sequence then the function latch CP 3-state bit is ‘dont care’.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS