

### FEATURES

- 2-Channel, 256-position**
- End-to-end resistance 2.5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$**
- Compact MSOP-10 (3 mm  $\times$  4.9 mm) Package**
- Full read/write of wiper register**
- Power-on preset to midscale**
- Extra package address decode pins AD0 and AD1(AD5248)**
- Single supply +2.7 V to +5.5 V**
- Low temperature coefficient 35 ppm/ $^{\circ}$ C**
- Low power, I<sub>DD</sub> = 5  $\mu$ A**
- Wide operating temperature -40 $^{\circ}$ C to +125 $^{\circ}$ C**
- Evaluation board available**

### APPLICATIONS

- Mechanical potentiometer replacement in new designs**
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors**
- RF amplifier biasing**
- Automotive electronics adjustment**
- Gain control and offset adjustment**

### GENERAL OVERVIEW

The AD5243 & AD5248 provide a compact 3x4.9mm packaged solution for dual 256 position adjustment applications. These devices perform the same electronic adjustment function as a 3-terminal mechanical potentiometer (AD5243) or a 2-terminal variable resistor (AD5248). Available in four different end-to-end resistance values (2.5k, 10k, 50k, 100k) these low temperature coefficient devices are ideal for high accuracy and stability variable resistance adjustments. The wiper settings are controllable through the I<sup>2</sup>C compatible digital interface. The AD5248 has extra package address decode pins AD0 & AD1 allowing multiple parts to share the same I<sup>2</sup>C 2-wire bus on a PCB.

The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch<sup>1</sup>.

Operating from a 2.7 to 5.5 volt power supply and consuming less than 5 $\mu$ A allows for usage in portable battery operated

applications.

All parts are guaranteed to operate over the extended automotive temperature range of -40 $^{\circ}$ C to +125 $^{\circ}$ C.

### FUNCTIONAL BLOCK DIAGRAMS

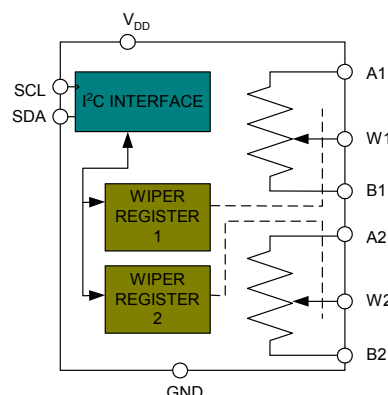


Figure 1. AD5243

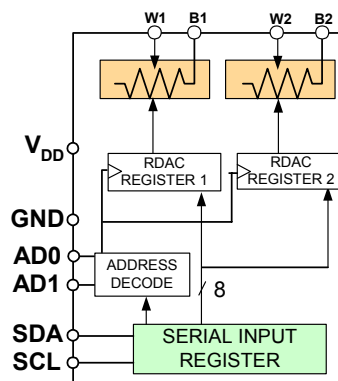


Figure 2. AD5248

Note:

The terms *digital potentiometer*, *VR*, and *RDAC* are used interchangeably.

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Rev. PrE5/12/03

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REVISION HISTORY

Revision 0: Initial Version

**ELECTRICAL CHARACTERISTICS—2.5 k $\Omega$  VERSION**(V<sub>DD</sub> = 5 V  $\pm$  10%, or 3 V  $\pm$  10%; V<sub>A</sub> = +V<sub>DD</sub>; V<sub>B</sub> = 0 V; -40°C < T<sub>A</sub> < +125°C; unless otherwise noted.)

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	R <sub>WB</sub> , V <sub>A</sub> = no connect	−1.8	±0.2	+1.8	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	R <sub>WB</sub> , V <sub>A</sub> = no connect	−5	±0.75	+5	LSB
Nominal Resistor Tolerance <sup>3</sup>	ΔR <sub>AB</sub>	T <sub>A</sub> = 25°C	−30		+30	%
Resistance Temperature Coefficient	ΔR <sub>AB</sub> /ΔT	V <sub>AB</sub> = V <sub>DD</sub> , Wiper = no connect		35		ppm/°C
Wiper Resistance	R <sub>W</sub>			50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Resolution	N				8	Bits
Differential Nonlinearity <sup>4</sup>	DNL		−1.5	±0.1	+1.5	LSB
Integral Nonlinearity <sup>4</sup>	INL		−1.5	±0.6	+1.5	LSB
Voltage Divider Temperature Coefficient	ΔV <sub>W</sub> /ΔT	Code = 0x80		15		ppm/°C
Full-Scale Error	V <sub>WFSE</sub>	Code = 0xFF	−6	−2.5	0	LSB
Zero-Scale Error	V <sub>WZSE</sub>	Code = 0x00	0	+2	+6	LSB
RESISTOR TERMINALS						
Voltage Range <sup>5</sup>	V <sub>A,B,W</sub>	f = 1 MHz, measured to GND, Code = 0x80	GND		V <sub>DD</sub>	V
Capacitance <sup>6</sup> A, B	C <sub>A,B</sub>			45		pF
Capacitance <sup>6</sup> W	C <sub>W</sub>	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current <sup>7</sup>	I <sub>DD_SD</sub>	V <sub>DD</sub> = 5.5 V		0.01	1	μA
Common-Mode Leakage	I <sub>CM</sub>	V <sub>A</sub> = V <sub>B</sub> = V <sub>DD</sub> /2		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V <sub>IH</sub>	V <sub>DD</sub> = 3 V V <sub>DD</sub> = 3 V V <sub>IN</sub> = 0 V or 5 V	2.4			V
Input Logic Low	V <sub>IL</sub>				0.8	V
Input Logic High	V <sub>IH</sub>		2.1			V
Input Logic Low	V <sub>IL</sub>				0.6	V
Input Current	I <sub>IL</sub>				±1	μA
Input Capacitance <sup>6</sup>	C <sub>IL</sub>			5		pF
POWER SUPPLIES						
Power Supply Range	V <sub>DD RANGE</sub>	V <sub>IH</sub> = 5 V or V <sub>IL</sub> = 0 V V <sub>IH</sub> = 5 V or V <sub>IL</sub> = 0 V, V <sub>DD</sub> = 5 V ΔV <sub>DD</sub> = +5 V ± 10%, Code = Midscale	2.7		5.5	V
Supply Current	I <sub>DD</sub>			3	5	μA
Power Dissipation <sup>8</sup>	P <sub>DISS</sub>				0.2	mW
Power Supply Sensitivity	PSS			±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS <sup>6,9</sup>						
Bandwidth −3dB	BW_5K	R <sub>AB</sub> = 2.5 kΩ, Code = 0x80		2.4		MHz
Total Harmonic Distortion	THD <sub>W</sub>	V <sub>A</sub> = 1 V rms, V <sub>B</sub> = 0 V, f = 1 kHz		0.05		%
V <sub>W</sub> Settling Time	t <sub>S</sub>	V <sub>A</sub> = 5 V, V <sub>B</sub> = 0 V, ±1 LSB error band		1		μs
Resistor Noise Voltage Density	e <sub>N_WB</sub>	R <sub>WB</sub> = 2.5 kΩ, R <sub>S</sub> = 0		4.5		nV/√Hz

**ELECTRICAL CHARACTERISTICS—10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$  VERSIONS**(V<sub>DD</sub> = 5 V  $\pm$  10%, or 3 V  $\pm$  10%; V<sub>A</sub> = V<sub>DD</sub>; V<sub>B</sub> = 0 V; -40°C < T<sub>A</sub> < +125°C; unless otherwise noted.)

Table 2.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS—RHEOSTAT MODE</b>						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	R <sub>WB</sub> , V <sub>A</sub> = no connect	-1	$\pm 0.1$	+1	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	R <sub>WB</sub> , V <sub>A</sub> = no connect	-2	$\pm 0.25$	+2	LSB
Nominal Resistor Tolerance <sup>3</sup>	$\Delta R_{AB}$	T <sub>A</sub> = 25°C	-30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V <sub>AB</sub> = V <sub>DD</sub> , Wiper = no connect		35		ppm/°C
Wiper Resistance	R <sub>W</sub>	V <sub>DD</sub> = 5 V		50	120	$\Omega$
<b>DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)</b>						
Resolution	N				8	Bits
Differential Nonlinearity <sup>4</sup>	DNL		-1	$\pm 0.1$	+1	LSB
Integral Nonlinearity <sup>4</sup>	INL		-1	$\pm 0.3$	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V <sub>WFSE</sub>	Code = 0xFF	-3	-1	0	LSB
Zero-Scale Error	V <sub>WZSE</sub>	Code = 0x00	0	1	3	LSB
<b>RESISTOR TERMINALS</b>						
Voltage Range <sup>5</sup>	V <sub>A,B,W</sub>		GND		V <sub>DD</sub>	V
Capacitance <sup>6</sup> A, B	C <sub>A,B</sub>	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance <sup>6</sup> W	C <sub>W</sub>	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current <sup>7</sup>	I <sub>DD_SD</sub>	V <sub>DD</sub> = 5.5 V		0.01	1	$\mu$ A
Common-Mode Leakage	I <sub>CM</sub>	V <sub>A</sub> = V <sub>B</sub> = V <sub>DD</sub> /2		1		nA
<b>DIGITAL INPUTS AND OUTPUTS</b>						
Input Logic High	V <sub>IH</sub>		2.4			V
Input Logic Low	V <sub>IL</sub>				0.8	V
Input Logic High	V <sub>IH</sub>	V <sub>DD</sub> = 3 V	2.1			V
Input Logic Low	V <sub>IL</sub>	V <sub>DD</sub> = 3 V			0.6	V
Input Current	I <sub>IL</sub>	V <sub>IN</sub> = 0 V or 5 V			$\pm 1$	$\mu$ A
Input Capacitance <sup>6</sup>	C <sub>IL</sub>			5		pF
<b>POWER SUPPLIES</b>						
Power Supply Range	V <sub>DD RANGE</sub>		2.7		5.5	V
Supply Current	I <sub>DD</sub>	V <sub>IH</sub> = 5 V or V <sub>IL</sub> = 0 V		3	5	$\mu$ A
Power Dissipation <sup>8</sup>	P <sub>DISS</sub>	V <sub>IH</sub> = 5 V or V <sub>IL</sub> = 0 V, V <sub>DD</sub> = 5 V			0.2	mW
Power Supply Sensitivity	PSS	$\Delta V_{DD}$ = +5 V $\pm$ 10%, Code = Midscale		$\pm 0.02$	$\pm 0.05$	%/%
<b>DYNAMIC CHARACTERISTICS<sup>6,9</sup></b>						
Bandwidth -3dB	BW	R <sub>AB</sub> = 10 k $\Omega$ /50 k $\Omega$ /100 k $\Omega$ , Code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD <sub>W</sub>	V <sub>A</sub> = 1 V rms, V <sub>B</sub> = 0 V, f = 1 kHz, R <sub>AB</sub> = 10 k $\Omega$		0.05		%
V <sub>W</sub> Settling Time (10 k $\Omega$ /50 k $\Omega$ /100 k $\Omega$ )	t <sub>s</sub>	V <sub>A</sub> = 5 V, V <sub>B</sub> = 0 V, $\pm 1$ LSB error band		2		$\mu$ s
Resistor Noise Voltage Density	e <sub>N_WB</sub>	R <sub>WB</sub> = 5 k $\Omega$ , R <sub>S</sub> = 0		9		nV/ $\sqrt$ Hz

TIMING CHARACTERISTICS—2.5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$  VERSIONS(V<sub>DD</sub> = +5V  $\pm$  10%, or +3V  $\pm$  10%; V<sub>A</sub> = V<sub>DD</sub>; V<sub>B</sub> = 0 V; -40°C < T<sub>A</sub> < +125°C; unless otherwise noted.)

Table 3.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<sup>12</sup> C INTERFACE TIMING CHARACTERISTICS <sup>6, 10</sup> (Specifications Apply to All Parts)						
SCL Clock Frequency	f <sub>SCL</sub>	After this period, the first clock pulse is generated.			400	kHz
t <sub>BUF</sub> Bus Free Time between STOP and START	t <sub>1</sub>		1.3			$\mu$ s
t <sub>HD,STA</sub> Hold Time (Repeated START)	t <sub>2</sub>		0.6			$\mu$ s
t <sub>LOW</sub> Low Period of SCL Clock	t <sub>3</sub>		1.3			$\mu$ s
t <sub>HIGH</sub> High Period of SCL Clock	t <sub>4</sub>		0.6		50	$\mu$ s
t <sub>SU,STA</sub> Setup Time for Repeated START Condition	t <sub>5</sub>		0.6			$\mu$ s
t <sub>HD,DAT</sub> Data Hold Time	t <sub>6</sub>				0.9	$\mu$ s
t <sub>SU,DAT</sub> Data Setup Time	t <sub>7</sub>		100			ns
t <sub>F</sub> Fall Time of Both SDA and SCL Signals	t <sub>8</sub>				300	ns
t <sub>R</sub> Rise Time of Both SDA and SCL Signals	t <sub>9</sub>				300	ns
t <sub>SU,STO</sub> Setup Time for STOP Condition	t <sub>10</sub>		0.6			$\mu$ s

## NOTES

<sup>1</sup> Typical specifications represent average readings at +25°C and V<sub>DD</sub> = 5 V.<sup>2</sup> Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.<sup>3</sup> V<sub>AB</sub> = V<sub>DD</sub>, Wiper (V<sub>W</sub>) = no connect.<sup>4</sup> INL and DNL are measured at V<sub>W</sub> with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V<sub>A</sub> = V<sub>DD</sub> and V<sub>B</sub> = 0 V.DNL specification limits of  $\pm 1$  LSB maximum are guaranteed monotonic operating conditions.<sup>5</sup> Resistor terminals A, B, W have no limitations on polarity with respect to each other.<sup>6</sup> Guaranteed by design and not subject to production test.<sup>7</sup> Measured at the A terminal. The A terminal is open circuited in shutdown mode.<sup>8</sup> P<sub>DISS</sub> is calculated from (I<sub>DD</sub>  $\times$  V<sub>DD</sub>). CMOS logic level inputs result in minimum power dissipation.<sup>9</sup> All dynamic characteristics use V<sub>DD</sub> = 5 V.<sup>10</sup> See timing diagrams for locations of measured values.ABSOLUTE MAXIMUM RATINGS<sup>1</sup>(T<sub>A</sub> = +25°C, unless otherwise noted.)

Table 4.

Parameter	Value
V <sub>DD</sub> to GND	-0.3 V to +7 V
V <sub>A</sub> , V <sub>B</sub> , V <sub>W</sub> to GND	V <sub>DD</sub>
I <sub>MAX</sub> <sup>1</sup>	$\pm 20$ mA
Digital Inputs and Output Voltage to GND	0 V to +7 V
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature (T <sub>JMAX</sub> )	150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance <sup>2</sup> $\theta_{JA}$ : MSOP-10	230°C/W

## NOTES

<sup>1</sup> Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.<sup>2</sup> Package power dissipation = (T<sub>JMAX</sub> - T<sub>A</sub>)/ $\theta_{JA}$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **TYPICAL PERFORMANCE CHARACTERISTICS**

## TEST CIRCUITS

Figure 3 to Figure 11 illustrate the test circuits that define the test conditions used in the product specification tables.

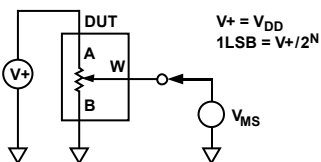


Figure 3. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

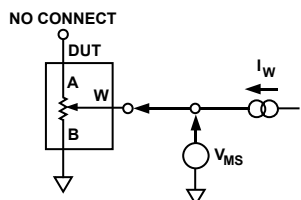


Figure 4. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

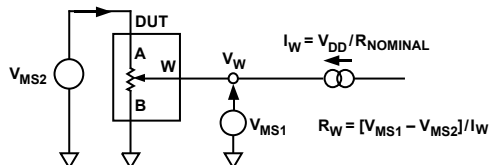


Figure 5. Test Circuit for Wiper Resistance

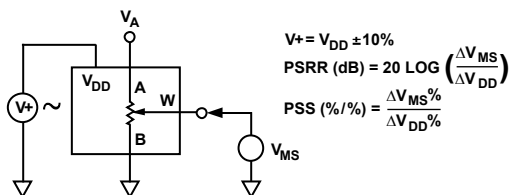


Figure 6. Test Circuit for Power Supply Sensitivity (PSS, PSRR)

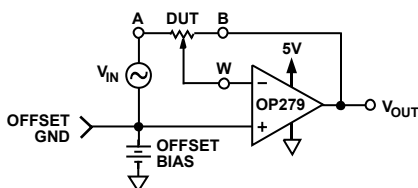


Figure 7. Test Circuit for Inverting Gain

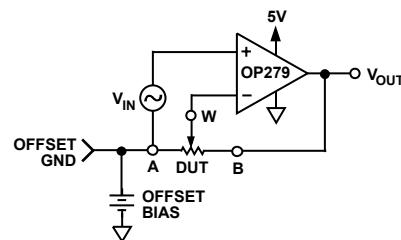


Figure 8. Test Circuit for Noninverting Gain

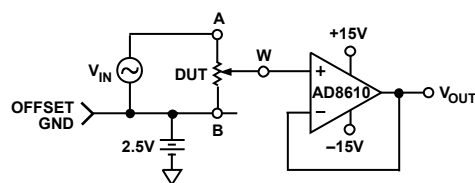


Figure 9. Test Circuit for Gain vs. Frequency

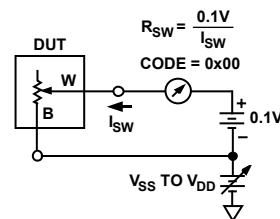


Figure 10. Test Circuit for Incremental ON Resistance

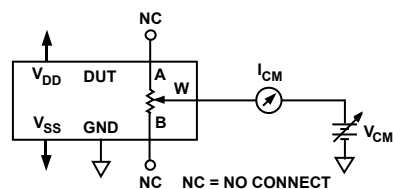


Figure 11. Test Circuit for Common-Mode Leakage current

I<sup>2</sup>C INTERFACE

Table 5. Write Mode

AD5243

S	0	1	0	1	1	1	1	$\overline{W}$	A	A0	SD	X	X	X	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
Slave Address Byte									Instruction Byte									Data Byte										

AD5248

S	0	1	0	1	1	AD1	AD0	$\overline{W}$	A	A0	SD	X	X	X	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
Slave Address Byte									Instruction Byte									Data Byte										

Table 6. Read Mode

AD5243

S	0	1	0	1	1	1	1	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
Slave Address Byte										Data Byte									

AD5248

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
Slave Address Byte										Data Byte									

S = Start Condition

P = Stop Condition

A = Acknowledge

X = Don't Care

 $\overline{W}$  = Write

R = Read

A0 = RDAC sub address select bit

SD = Shutdown connects wiper to B terminal and open circuits A terminal. It does not change contents of wiper register.

D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits



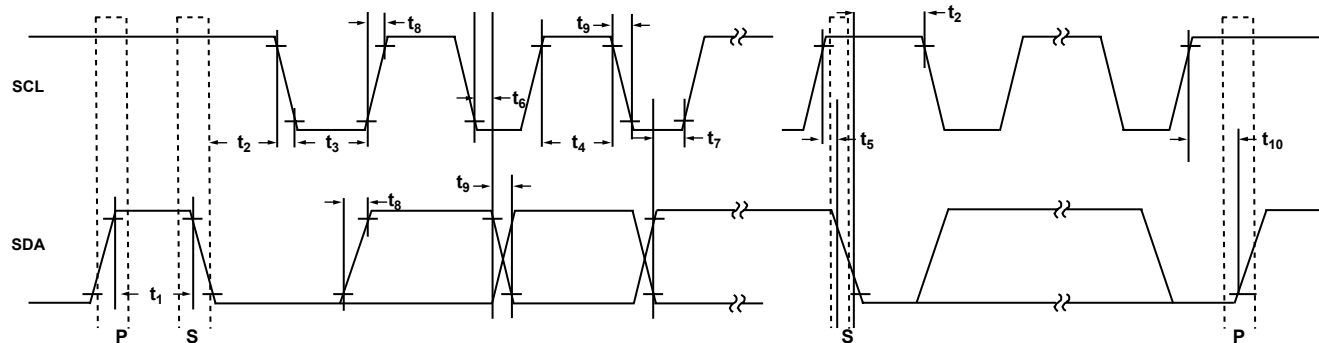


Figure 12. I²C Interface Detailed Timing Diagram

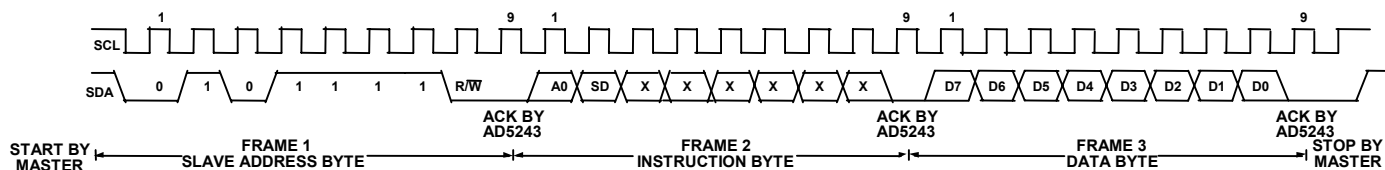


Figure 13. Writing to the RDAC Register – AD5243

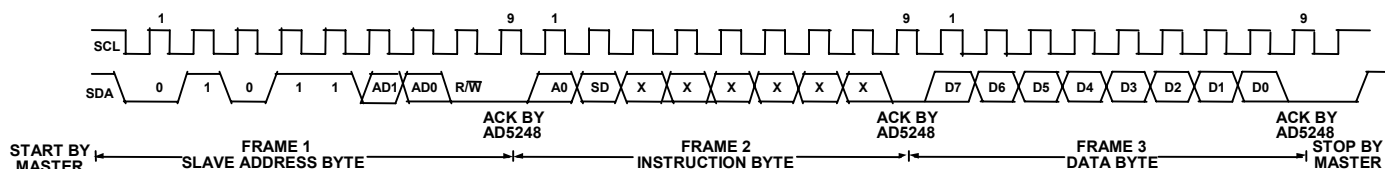


Figure 14. Writing to the RDAC Register – AD5248

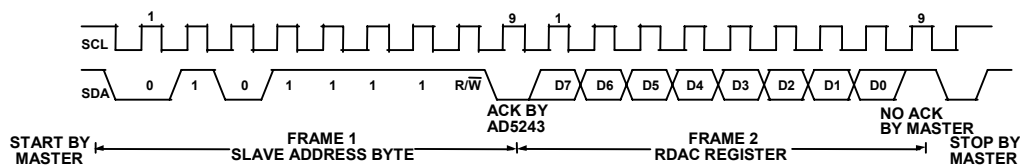


Figure 15. Reading Data from a Previously Selected RDAC Register in Write Mode – AD5243

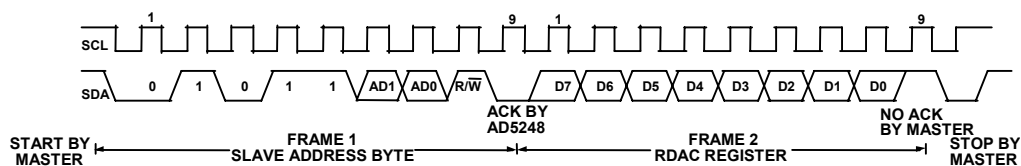


Figure 16 Reading Data from a Previously Selected RDAC Register in Write Mode – AD5248

## OPERATION

The AD5243/48 is a 256-position digitally controlled variable resistor (VR) device.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

### PROGRAMMING THE VARIABLE RESISTOR

#### Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$ . The final two or three digits of the part number determine the nominal resistance value, e.g., 10 k $\Omega$  = 10; 50 k $\Omega$  = 50. The nominal resistance ( $R_{AB}$ ) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assume a 10 k $\Omega$  part is used, the wiper's first connection starts at the B terminal for data 0x00. Since there is a 60  $\Omega$  wiper contact resistance, such connection yields a minimum of 60  $\Omega$  resistance between terminals W and B. The second connection is the first tap point, which corresponds to 99  $\Omega$  ( $R_{WB} = R_{AB}/256 + R_W = 39 \Omega + 60 \Omega$ ) for data 0x01. The third connection is the next tap point, representing 138  $\Omega$  ( $2 \times 39 \Omega + 60 \Omega$ ) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 9961  $\Omega$  ( $R_{AB} - 1 \text{ LSB} + R_W$ ). Figure 17 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string will not be accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

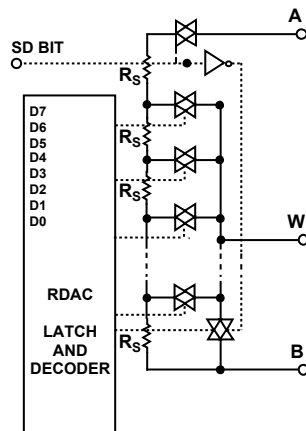


Figure 17. AD5243/48 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where  $D$  is the decimal equivalent of the binary code loaded in the 8-bit RDAC register,  $R_{AB}$  is the end-to-end resistance, and  $R_W$  is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if  $R_{AB} = 10 \text{ k}\Omega$  and the A terminal is open circuited, the following output resistance  $R_{WB}$  will be set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding  $R_{WB}$  Resistance

D (Dec.)	$R_{WB} (\Omega)$	Output State
255	9,961	Full Scale ( $R_{AB} - 1 \text{ LSB} + R_W$ )
128	5,060	Midscale
1	99	1 LSB
0	60	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 60  $\Omega$  is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance  $R_{WA}$ . When these terminals are used, the B terminal can be opened. Setting the resistance value for  $R_{WA}$  starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

For  $R_{AB} = 10 \text{ k}\Omega$  and the B terminal open circuited, the following output resistance  $R_{WA}$  will be set for the indicated RDAC latch codes.

Table 8. Codes and Corresponding  $R_{WA}$  Resistance

D (Dec.)	$R_{WA} (\Omega)$	Output State
255	99	Full Scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero Scale

Typical device to device matching is process lot dependent and may vary by up to  $\pm 30\%$ . Since the resistance element is processed in thin film technology, the change in  $R_{AB}$  with temperature has a very low 45 ppm/ $^{\circ}\text{C}$  temperature coefficient.

## PROGRAMMING THE POTENTIOMETER DIVIDER

### Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A-to-B. Unlike the polarity of  $V_{DD}$  to GND, which must be positive, voltage across A-B, W-A, and W-B can be at either polarity.

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at  $V_W$  with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256-D}{256} V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance,  $V_W$ , can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors  $R_{WA}$  and  $R_{WB}$  and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

## I<sup>2</sup>C COMPATIBLE 2-WIRE SERIAL BUS

The 2-wire I<sup>2</sup>C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 13). The following byte is the slave address byte, which consists of the slave address followed by an R/W bit (this bit determines whether data will be read from or written to the slave device). The AD5243 has a fixed slave address byte whereas the AD5248 has two configurable address bits AD0 and AD1 (see Table 5).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/W bit is high, the master will read from the slave device. On the other hand, if the R/W bit is low, the master will write to the slave device.

2. In the write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is the RDAC sub address select bit. A logic low will select channel-1 and a logic high will select channel-2.

The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at terminal A while shorting the wiper to terminal B. This operation yields almost 0  $\Omega$  in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting will be applied to the RDAC. Also, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting will be applied to the RDAC.

The remainder of the bits in the instruction byte are don't cares (see Table 5).

After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Table 5).

3. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference with the write mode, where there are eight data bits followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 15 and Figure 16).

Note that the channel of interest is the one that is previously selected in the Write Mode. In the case where users need to read the RDAC values of both channels, they need to program the first channel in the Write Mode and then change to the Read Mode to read the first channel value. After that, they need to change back to the Write Mode with the second channel selected and read the second channel value in the Read Mode again. It is not necessary for users to issue the Frame 3 data byte in the write mode for subsequent readback operation. Users should refer to Figure 15 for the programming format.

4. After all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master will pull the SDA line high during the tenth clock pulse to establish a STOP condition (see Figure 13). In read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse which goes high to establish a STOP condition (see Figure 15 and Figure 16).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output will update on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

#### Multiple Devices on One Bus (applies only to AD5248)

Figure 18 shows four AD5248 devices on the same serial bus. Each has a different slave address since the states of their AD0 and AD1 pins are different. This allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I<sup>2</sup>C compatible interface.

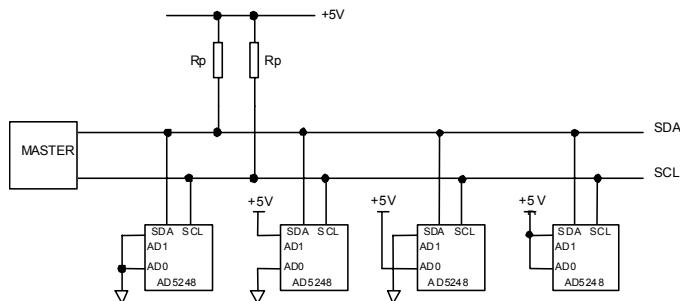


Figure 18. Multiple AD5248 Devices on One I<sup>2</sup>C Bus

#### LEVEL SHIFTING FOR BIDIRECTIONAL INTERFACE

While most legacy systems may be operated at one voltage, a new component may be optimized at another. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, one can use a 3.3 V E<sup>2</sup>PROM to interface with a 5 V digital potentiometer. A level shifting scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored to and retrieved from the E<sup>2</sup>PROM. Figure 19 shows one of the implementations. M1 and M2 can be any N-channel signal FETs, or if V<sub>DD</sub> falls below 2.5 V, low threshold

FETs such as the FDV301N.

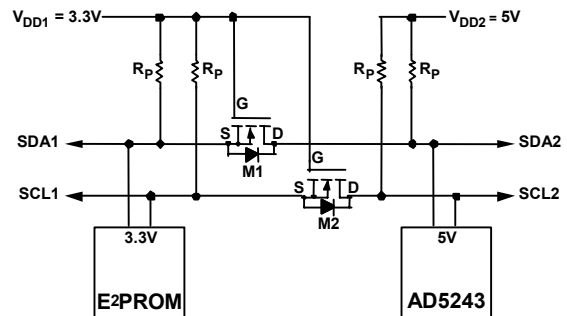


Figure 19. Level Shifting for Operation at Different Potentials

#### ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 20 and Figure 21. This applies to the digital input pins SDA, SCL, and AD0.

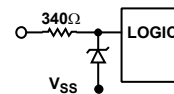


Figure 20. ESD Protection of Digital Pins

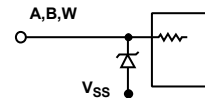


Figure 21. ESD Protection of Resistor Terminals

#### TERMINAL VOLTAGE OPERATING RANGE

The AD5243/48 V<sub>DD</sub> and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V<sub>DD</sub> or GND will be clamped by the internal forward biased diodes (see Figure 22).

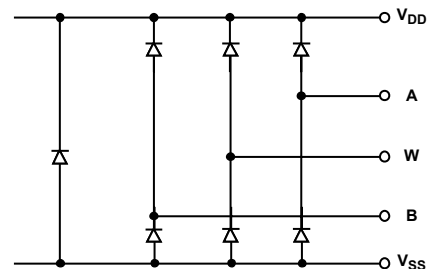


Figure 22. Maximum Terminal Voltages Set by V<sub>DD</sub> and V<sub>SS</sub>

## POWER-UP SEQUENCE

Since the ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 22), it is important to power  $V_{DD}/GND$  before applying any voltage to terminals A, B, and W; otherwise, the diode will be forward biased such that  $V_{DD}$  will be powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND,  $V_{DD}$ , digital inputs, and then  $V_{A/B/W}$ . The relative order of powering  $V_A$ ,  $V_B$ ,  $V_W$ , and the digital inputs is not important as long as they are powered after  $V_{DD}/GND$ .

## LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the

device should be bypassed with disc or chip ceramic capacitors of 0.01  $\mu F$  to 0.1  $\mu F$ . Low ESR 1  $\mu F$  to 10  $\mu F$  tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 23). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

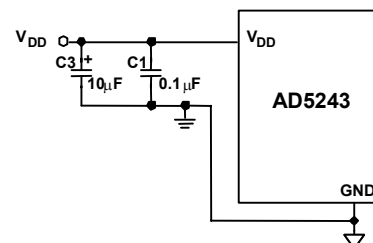


Figure 23. Power Supply Bypassing

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

### PIN CONFIGURATION

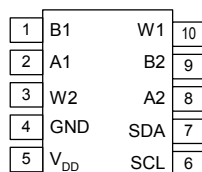


Figure 24.- AD5243 Pin Configuration

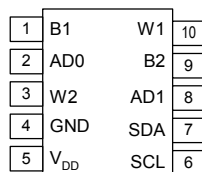


Figure 25. – AD5243 Pin Configuration

### PIN FUNCTION DESCRIPTIONS

Table 9.

Pin	Name	Description
1	B1	B1 Terminal.
2	A1	A1 Terminal.
3	W2	W2 Terminal.
4	GND	Digital Ground.
5	V <sub>DD</sub>	Positive Power Supply.
6	SCL	Serial Clock Input. Positive edge triggered.
7	SDA	Serial Data Input/Output.
8	A2	A2 Terminal.
9	B2	B2 Terminal.
10	W2	W2 Terminal.

Table 10.

Pin	Name	Description
1	B1	B1 Terminal.
2	AD0	Programmable address bit 0 for multiple package decoding.
3	W2	W2 Terminal
4	GND	Digital Ground.
5	V <sub>DD</sub>	Positive Power Supply..
6	SCL	Serial Clock Input. Positive edge triggered.
7	SDA	Serial Data Input/Output.
8	AD1	Programmable address bit 1 for multiple package decoding.
9	B2	B2 Terminal.
10	W1	W1 Terminal.

## OUTLINE DIMENSIONS

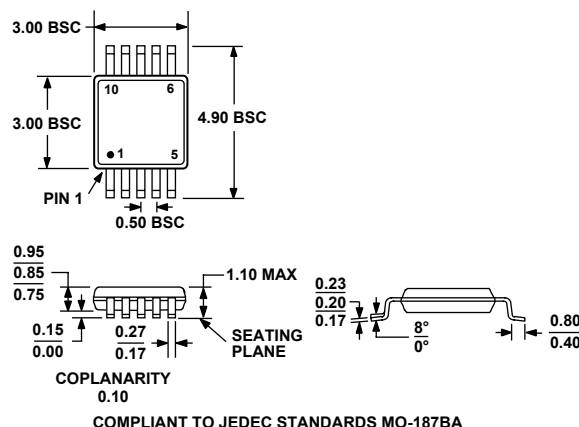


Figure 26. 10-Lead Mini Small Outline Package [MSOP]  
(RM-10)  
Dimensions shown in millimeters

## ORDERING GUIDE

Model	R <sub>AB</sub> (Ω)	Temperature	Package Description	Package Option	Branding
AD5243BRM2.5-R2	2.5k	–40°C to +125°C	MSOP-10	RM-10	D0L
AD5243BRM2.5-RL7	2.5k	–40°C to +125°C	MSOP-10	RM-10	D0L
AD5243BRM10-R2	10k	–40°C to +125°C	MSOP-10	RM-10	D0M
AD5243BRM10-RL7	10k	–40°C to +125°C	MSOP-10	RM-10	D0M
AD5243BRM50-R2	50k	–40°C to +125°C	MSOP-10	RM-10	D0N
AD5243BRM50-RL7	50k	–40°C to +125°C	MSOP-10	RM-10	D0N
AD5243BRM100-R2	100k	–40°C to +125°C	MSOP-10	RM-10	D0P
AD5243BRM100-RL7	100k	–40°C to +125°C	MSOP-10	RM-10	D0P
AD5243EVAL	See Note 1		Evaluation Board		

Model	R <sub>AB</sub> (Ω)	Temperature	Package Description	Package Option	Branding
AD5248BRM2.5-R2	2.5k	–40°C to +125°C	MSOP-10	RM-10	D1F
AD5248BRM2.5-RL7	2.5k	–40°C to +125°C	MSOP-10	RM-10	D1F
AD5248BRM10-R2	10k	–40°C to +125°C	MSOP-10	RM-10	D1G
AD5248BRM10-RL7	10k	–40°C to +125°C	MSOP-10	RM-10	D1G
AD5248BRM50-R2	50k	–40°C to +125°C	MSOP-10	RM-10	D1H
AD5248BRM50-RL7	50k	–40°C to +125°C	MSOP-10	RM-10	D1H
AD5248BRM100-R2	100k	–40°C to +125°C	MSOP-10	RM-10	D1J
AD5248BRM100-RL7	100k	–40°C to +125°C	MSOP-10	RM-10	D1J
AD5248EVAL	See Note 1		Evaluation Board		

<sup>1</sup>The evaluation board is shipped with the 10 kΩ R<sub>AB</sub> resistor option; however, the board is compatible with all available resistor value options.

The AD5243/48 contains 2532 transistors. Die size: 30.7 mil × 76.8 mil = 2,358 sq. mil.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



**NOTES**