I²C, Nonvolatile Memory, Quad 64/256-Position Digital potentiometers

Preliminary Technical Data AD5253/AD5254

FEATURES

AD5253: Quad 64-Position Resolution
AD5254: Quad 256-Position Resolution
Nonvolatile Memory[1] Maintains Wiper Settings
Resistance Tolerance Stored In Nonvolatile Memory
1 kΩ, 10 kΩ, 50 kΩ 100 kΩ
I2C Compatible Serial Interface
Wiper Settings Read Back
Linear Increment/Decrement Predefined Instructions
+/-6dB Log taper Increment/Decrement Predefined Instructions
Single Supply 2.7V to 5.5V
Dual Supply ±2.7V
Logic Operation Voltage 2.7V to 5V
Power On Presets to EEMEM Settings with Refresh Time < 1ms
Nonvolatile Memory Write Protection
100-Year Typical Data Retention T_A = 55 °C
Operating Temperature -40°C to +125°C
TSSOP-20

APPLICATIONS

Mechanical Potentiometer Replacement
Low Resolution DAC Replacement
Sensors Calibrations
Electronics Level Settings
RF Base Station Power Amp Bias Control
Programmable Gain and Offset Control
Programmable Attentuator
Programmable Voltage to Current Conversion
Programmable Power Supply
Programmable Filters
Line Impedance Matching

GENERAL DESCRIPTION

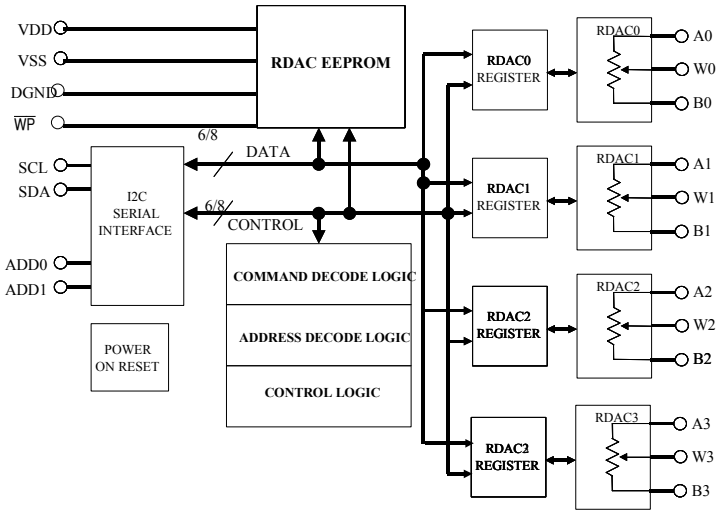
The AD5253/AD5254 is a dual channel, digitally controlled variable resistor (VR) with resolutions of 1024 positions. This device performs the same electronic adjustment function as a potentiometer or variable resistor. The AD5253/AD5254's versatile programming via a Micro Controller allows multiple modes of operation and adjustment.

In the direct program mode a predetermined setting of the RDAC register can be loaded directly from the micro controller. Another key mode of operation allows the RDAC register to be refreshed with the setting previously stored in the EEMEM register. When changes are made to the RDAC register to establish a new wiper position, the value of the setting can be saved into the EEMEM by executing an EEMEM save operation. Once the settings are saved in the EEMEM register, these values will be transferred automatically to the RDAC register to set the wiper position at system power ON. Such operation is enabled by the internal preset strobe and the preset can also be accessed externally.

The basic mode of adjustment is the increment and decrement from the present setting of the Wiper position setting (RDAC) register. An internal scratch pad RDAC register can be moved UP or DOWN, one step of the nominal resistance between terminals A-and-B. This linearly changes the wiper-to-B terminal resistance (R_{WB}) by one out of 64/256 positions of the AD5253/AD5254 end-to-end resistance (R_{AB}). For non-linear changes in wiper setting, a left/right shift command adjusts levels in 6dB steps which can be useful for sound and light alarm applications.

The AD5253/AD5254 is available in the thin TSSOP-20 package. All parts are guaranteed to operate over the extended industrial temperature range of -40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAMS



Notes

1: The terms Nonvolatile Memory and EEMEM are used interchangeably.

2: The terms digital potentiometer, VR, and RDAC are used interchangeably.

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Nonvolatile Memory Digital Potentiometers AD5253/AD5254

ELECTRICAL CHARACTERISTICS 1k, 10k , 50k, 100kΩ VERSIONS (V_{DD} = +3V±10% or +5V±10% and V_{SS}=0V, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +125°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE	Specifications apply to all VRs					
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A=NC	-1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A=NC	-2	±1/2	+2	LSB
Nominal resistor tolerance	ΔR	T_A = 25°C, V_{AB} = V_{DD},Wiper (V_W) = No connect	-30		30	%
Resistance Temperature Coefficent	R_{AB}/ΔT	V_{AB} = V_{DD}, Wiper (V_W) = No Connect		X		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = +5V		50	100	Ω
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = +3V		200		Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE	Specifications apply to all VRs					
Resolution	N	AD5253/AD5254			6/8	Bits
Integral Nonlinearity[3]	INL		–2	±1/2	+2	LSB
Differential Nonlinearity[3]	DNL		–1	±1/4	+1	LSB
Voltage Divider Temperature Coefficent	$\Delta V_W/\Delta T$	Code = Half-scale		X		ppm/°C
Full-Scale Error	V_{WFSE}	Code = Full-scale	–3	-1	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = Zero-scale	0	+1	+3	LSB
RESISTOR TERMINALS						
Voltage Range[4]	$V_{A,B,W}$		V_{SS}		V_{DD}	V
Capacitance[5] Ax, Bx	$C_{A,B}$	f = 1 MHz, measured to GND, Code = Half-scale		45		pF
Capacitance[5] Wx	C_W	f = 1 MHz, measured to GND, Code = Half-scale		60		pF
Common-mode Leakage Current[7]	I_{CM}	V_A = V_B = V_{DD}/2		0.01	1	µA
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}	with respect to GND	0.3•V_{DD}			V
Input Logic Low	V_{IL}	with respect to GND			0.7•V_{DD}	V
Output Logic High	V_{OH}	$R_{PULL-UP}$ = 2.2KΩ to +5V	4.9			V
Output Logic High	V_{OH}	I_{OH} = 40µA, V_{LOGIC} = +5V	4			V
Output Logic Low	V_{OL}	I_{OL} = 1.6mA, V_{LOGIC} = +5V			0.4	V
Input Current	I_{IL}	V_{IN} = 0V or V_{DD}			±1	µA
Input Capacitance[5]	C_{IL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}	V_{SS} = 0V	±2.2		±2.7	V
Positive Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND		2	10	µA
Programming Mode Current	$I_{DD(PG)}$	V_{IH} = V_{DD} or V_{IL} = GND		15		mA
Read Mode Current	$I_{DD(READ)}$	V_{IH} = V_{DD} or V_{IL} = GND		650		µA
Negative Supply Current	I_{SS}	V_{IH} = V_{DD} or V_{IL} = GND, V_{DD} = 2.5V, V_{SS} = -2.5V			10	µA
Power Dissipation[6]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = GND			0.05	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5V ±10%		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS[5, 7]						
Bandwidth –3dB	BW	R_{AB} = 1k/10k/50k/100kΩ		TBD		kHz
Total Harmonic Distortion	THD_W	V_A =1Vrms, V_B = 0V, f=1KHz		0.003		%
V_W Settling Time	t_S	V_A= VDD, V_B=0V, 50% of final value				
		1k/10k/50k/100k		TBD		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5KΩ, f = 1KHz		9		nV√Hz
Crosstalk	C_T	V_A = V_{DD}, V_B = 0V, Measue V_W with adjacent				
		VR making full scale change		-65		dB

ELECTRICAL CHARACTERISTICS 1k, 10k , 50k, 100kΩ VERSIONS (V_{DD} = +3V±10% to +5V±10% and V_{SS}=0V, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +125°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
INTERFACE TIMING CHARACTERISTICS applies to all parts(Notes 5,8)						
SCL Clock Frequency	f_{SCL}		0		400	kHz
t_{BUF} Bus free time between STOP & START	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (repeated START)	t_2	After this period the first clock pulse is generated	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6			µs
$t_{SU;STA}$ Setup Time For START Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6		0		0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of both SDA & SCL signals	t_8				300	ns
t_R Rise Time of both SDA & SCL signals	t_9				300	ns
$t_{SU;STO}$ Setup time for STOP Condition	t_{10}		0.6			µs
Store to Nonvolatile EEMEM Save Time[9]	t_{12}	Applies to Command 2_H, 3_H			25	ms
RDY Rise to CS Fall	t_{15}					ns
Preset Pulse Width	t_{PR}		50			ns

NOTES:

1. Typicals represent average readings at +25°C and V_{DD} = +5V.
2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See figure 20 test circuit. I_W = V_{DD}/R for both V_{DD}=+3V or V_{DD}=+5V.
3. INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0V. DNL specification limits of ±1LSB maximum are Guaranteed Monotonic operating conditions. See Figure 19 test circuit.
4. Resistor terminals A,B,W have no limitations on polarity with respect to each other.
5. Guaranteed by design and not subject to production test.
6. P_{DISS} is calculated from (I_{DD} x V_{DD}=+5V).
7. All dynamic characteristics use V_{DD} = +5V.
8. See timing diagram for location of measured values. All input control voltages are specified with t_R=t_F=2.5ns(10% to 90% of 3V) and timed from a voltage level of 1.5V. Switching characteristics are measured using both V_{DD} = +3V or +5V.
9. Low only for commands 8, 9,10, 2, 3: CMD_8 ~ 1ms; CMD_9,10 ~0.1ms; CMD_2,3 ~20ms

Timing Diagram

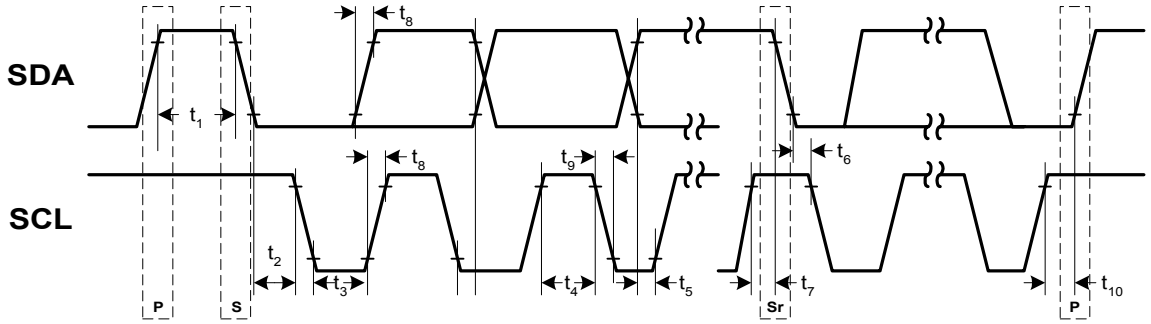


Figure 1. Timing Diagram

Data of AD5253/AD5254 is accepted from the I²C bus in the following serial format:

S	0	1	0	1	1	ADD1	ADD0	R/$\overline{W}$	A	I7	I6	I5	I4	I3	I2	I1	I0	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Where:
S = Start Condition
P = Stop Condition
A = Acknowledge
X = Don't Care

ADD1, **ADD0** = Package pin programmable address bits
R/$\overline{W}$= Read Enable at High and Write Enable at Low
I7 – I0 = Instruction bits
D5 - D0 = 6 Data Bits. D7 and D6 = X (AD5253)
D7 - D0 = 8 Data Bits (AD5254)

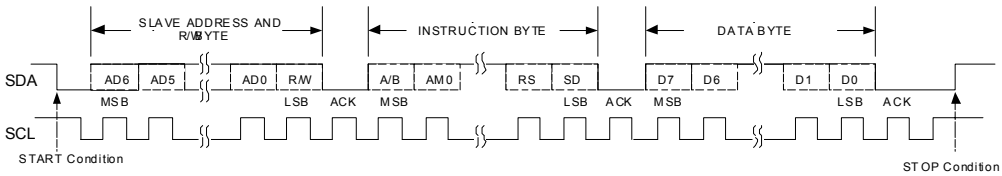


Figure 2.Complete Serial Transmission

Absolute Maximum Rating (T_A = +25°C, unless otherwise noted)

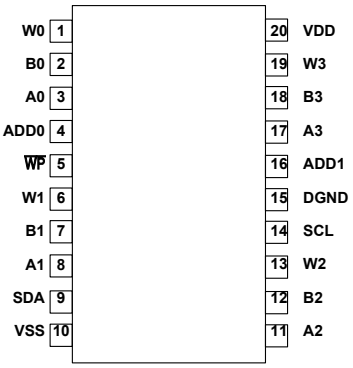
V_{DD} to GND .....-0.3, +7V
V_{SS} to GND .....+0.3, -7V
V_{DD} to V_{SS} .....+7V
V_A, V_B, V_W to GND.....V_{SS}, V_{DD}
$A_X - B_X$, $A_X - W_X$, $B_X - W_X$
Pulse .....±20mA
Continuous.....±5mA
Digital Inputs & Output Voltage to GND.....0V, +7V
Operating Temperature Range.....-40°C to +85°C
Maximum Junction Temperature ($T_{J\ MAX}$).....+150°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (Soldering, 10 sec).....+300°C
Thermal Resistance θ_{JA},
TSSOP-20..... XXX°C/W
Package Power Dissipation = (T_JMAX - T_A) / θ_{JA}

Ordering Guide

Model	Step	R_{AB} (kΩ)	Temp Range (°C)	Package Description	Package Option
AD5253BRU1	64	1	-40/+125	TSSOP-20	RU-20
AD5253BRU10	64	10	-40/+125	TSSOP-20	RU-20
AD5253BRU50	64	50	-40/+125	TSSOP-20	RU-20
AD5253BRU100	64	100	-40/+125	TSSOP-20	RU-20
AD5254BRU1	256	1	-40/+125	TSSOP-20	RU-20
AD5254BRU10	256	10	-40/+125	TSSOP-20	RU-20
AD5254BRU50	256	50	-40/+125	TSSOP-20	RU-20
AD5254BRU100	256	100	-40/+125	TSSOP-20	RU-20

The AD5253/AD5254 contain x,xxx transistors.
Die size: x' mil x y' mil, z' sq. mil

AD5253/AD5254 PIN CONFIGURATION



AD5253/AD5254 PIN FUNCTION DESCRIPTION

#	Name	Description
1	W0	Wiper terminal of RDAC0.
2	B0	B terminal of RDAC0
3	A0	A terminal of RDAC0.
4	ADD0	I2C Device Address 0
5	$\overline{WP}$	Write Protect, Active Low
6	W1	Wiper terminal of RDAC1
7	B1	B terminal of RDAC1
8	A1	A terminal of RDAC1.
9	SDA	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first.
10	V_{SS}	Negative Supply. Connect to zero volt for single supply
11	A2	A terminal of RDAC2.
12	B2	B terminal of RDAC2.
13	W2	Wiper terminal of RDAC2
14	SCL	Serial Input Register clock pin. Shifts in one bit at a time on positive clock edges.
15	DGND	Digital Ground. Connect to System Analog Ground at a Single Point
16	ADD1	I2C Device Address 1
17	A3	A terminal of RDAC3
18	B3	Wiper terminal of RDAC3
19	W3	W terminal of RDAC3
20	V_{DD}	Positive Power Supply Pin.

OPERATIONAL OVERVIEW

The AD5253/AD5254 digital potentiometer is designed to operate as a true variable resistor replacement device for analog signals that remain within the terminal voltage range of $V_{SS}<V_{TERM}<V_{DD}$. The basic voltage range is limited to a V_{DD} - V_{SS}<5.5V. Control of the digital potentiometer allows both scratch pad register (RDAC register) changes to be made, as well as 100,000 times of nonvolatile electrically erasable memory (EEMEM) register operations. The EEMEM update process takes approximately 20.2ms, during this time the shift register is locked preventing any changes from taking place. The EEMEM retention is designed to last 10 years without refresh. The scratch pad register can be changed incrementally by using the software controlled Increment/Decrement instruction or the Shift Left/Right instruction command. Alternately the scratch pad register can be programmed with any position value using the standard I^2C serial interface mode by loading the representative data word. The scratch pad register can be loaded with the current contents of the nonvolatile EEMEM register under program control. At system power ON, the default value of the scratch pad memory is the value previously saved in the EEMEM register. The factory EEMEM preset values are mid-scale 32/128 for AD5253/AD5254 respectively.

The serial input data register uses a 32-bit slave address/instruction/data WORD.

SERIAL DATA INTERFACE

The AD5253/AD5254 employs a two-wire I^2C serial interface requiring only two I/O lines of a standard microprocessor port. Key features of this interface include:

- Read & Write capability to all registers
- Direct parallel refresh of all RDAC wiper registers from corresponding EEMEM registers
- Increment & Decrement instructions for each RDAC wiper register
- Left & right Bit Shift of all RDAC wiper registers to achieve 6dB level changes
- Permanent storage of the present scratch pad RDAC register values into the corresponding EEMEM register
- EEMEM Write Protect

Figure 1 shows the timing diagram for signals on the wire bus. The 2-wire bus can have several devices attached in addition to the AD5253/AD5254. The two bus lines (SDA and SCL) must be high when the bus is not in use. When in use, the port bits are toggled to generate the appropriate signals for SDA and SCL. For I^2C applications, two pull up resistors are required at both the SDA and SCL pins to VDD.

The AD5253/AD5254 can operate SCL of up to 400kHz. A master device sends information to the AD5253/AD5254 by transmitting the AD5253/AD5254's address over the bus and then transmitting the desired information. Each transmission consists of a START condition, the AD5253/AD5254's programmable slave address, an instruction byte, 2 data bytes consist of 10 data bits, and a STOP condition.

The address byte, instruction byte, and data bytes are transmitted between the START and STOP conditions. The state of SDA is allowed to change only if SCL is low, with the exceptions at START and STOP conditions. SDA must remain stable and is sampled (read or write depends upon the state of R/W) when SCL is high. Data is transmitted in 8-bit bytes.

The START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 3). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

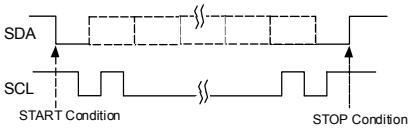


Figure 3.START and STOP Conditions

The Slave Address

The AD5253/AD5254's slave address is seven bits long (Figure 4). The first five bits (MSBs) of the slave address have been factory programmed to 01011. The state of the AD5253/AD5254 inputs AD0 and AD1 determine the final two bits of the 7-bit slave address, These input pins may be connected to VDD or GND, or may be actively driven by TTL or CMOS logic levels. There are four possible addresses for the AD5253/AD5254, and therefore a maximum of four such devices may be on the bus at the same time. The eighth bit (LSB) in the slave address byte is for read write purpose. Active high allows data to be read back from the input register. Active low allows data to be written to the input register. The AD5253/AD5254 watches the bus continuously, waiting for a START condition followed by its slave address. When it recognizes its slave address, it is ready to accept data.

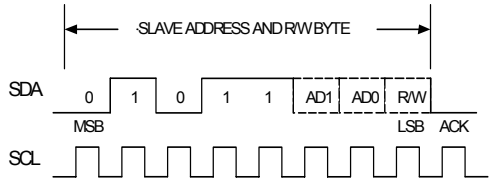


Figure 4. Slave Address and R/W Byte

The Instruction Byte

(To be determined)

The Data Bytes

(To be determined)

Table 1. AD5253/AD5254 Instruction/Operation Truth Table

Slave Address & R/W Byte B31 …………………………………. B24 AD6 AD5 AD4 AD3 AD2 AD1 AD0 R/W	Instruction Byte B23 …………………………………. B16 I7 I6 I5 I4 I3 I2 I1 I0	Data Byte B7 ……… B0 D7 ……… D0	Operation
0 1 0 1 1 0 0 0	0	X ……….. X	
0 1 0 1 1 0 0 1	0	X ……….. X	
0 1 0 1 1 0 0 0	1	X ……….. X	
0 1 0 1 1 0 0 1	1	X ……….. X	
0 1 0 1 1 0 0 0	0	X ……….. X	
0 1 0 1 1 0 0 1	0	X ……….. X	
0 1 0 1 1 0 0 0	1	X ……….. X	
0 1 0 1 1 0 0 1	1	X ……….. X	
0 1 0 1 1 0 0 0	0	X ……….. X	
0 1 0 1 1 0 0 1	0	X ……….. X	
0 1 0 1 1 0 0 0	1	X ……….. X	
0 1 0 1 1 0 0 1	1	X ……….. X	
0 1 0 1 1 0 0 0	0	X ……….. X	
0 1 0 1 1 0 0 1	0	X ……….. X	
0 1 0 1 1 0 0 0	1	X ……….. X	
0 1 0 1 1 0 0 1	1	X ……….. X	

NOTES:

1. The RDAC register is a volatile scratch pad register that is refreshed at power ON from the corresponding non-volatile EEMEM register.
2. The increment, decrement and shift commands ignore the contents of the shift register Data Byte.

Detail Potentiometer Operation

The actual structure of the RDAC is designed to emulate the performance of a mechanical potentiometer. The RDAC contains a string of connected resistor segments, with an array of analog switches that act as the wiper connection to several points along the resistor array. The number of points is the resolution of the device. For example, the AD5253/AD5254 emulates 64/256 connection points with 64/256 equal resistance, R_s, allowing it to provide better than 1.5%/0.4% set-ability resolution. Figure 5 provides an equivalent diagram of the connections between the three terminals that make up one channel of the RDAC. The switches SW_A and SW_B will always be ON while one of the switches SW(0) to SW(2^N-1) will be ON one at a time depends upon the resistance step decoded from the data. The total resistance of the active switches makes up the wiper resistance, R_W.

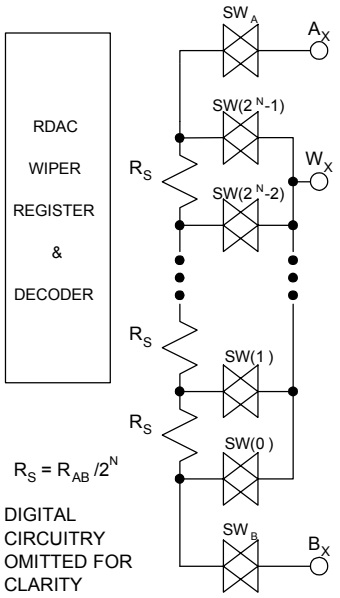


Figure 5. Equivalent RDAC structure

PROGRAMMING THE VARIABLE RESISTOR
Rheostat Operation

The nominal resistance of the RDAC between terminals A and B are available with values of 1kΩ, 10kΩ, 50kΩ, and 100kΩ. The final digits of the part number determine the nominal resistance value, e.g., 1kΩ = 1, 10kΩ = 10, 50kΩ = 50, and 100kΩ = 100. The nominal resistance (R_{AB}) of the AD5253/AD5254 VR has 64/256 contact points accessed by the wiper terminal, plus the B terminal contact. The 6/8-bit data word in the RDAC latch is decoded to select one of the 64/256 possible settings. The wiper's first connection starts at the B terminal for data 00_H. This B–terminal connection has a wiper contact resistance, R_w of 50Ω, regardless of what the nominal resistance is. The second connection (AD5253 10kΩ part) is the first tap point where R_{WB}=206Ω [R_{WB}=R_{AB}/64 + R_W = 156Ω+50Ω)] for data 01_H. The third connection is the next tap point representing R_{WB}=312+50= 362Ω for data 02_H. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at R_{WB}=9893Ω. See figure 6 for a simplified diagram of the equivalent RDAC circuit.

The general equation, which determines the digitally programmed output resistance between Wx and Bx, is:

$$R_{WB}(Dx) = (Dx/2^N)*R_{AB} + R_W \qquad \text{eqn. 1}$$

Where N is the resolution of the VR, Dx is the data contained in the RDACx latch, and R_{AB} is the nominal end-to-end resistance. Since N=6/8-bit and R_w=50Ω for AD5253/AD5254, eqn. 1 becomes:

$$R_{WB}(Dx) = (Dx/64)*R_{AB} + 50\Omega \qquad \text{(AD5253) eqn. 2}$$

$$R_{WB}(Dx) = (Dx/256)*R_{AB} + 50\Omega \qquad \text{(AD5254) eqn. 3}$$

For example, when V_B = 0V and A–terminal is open circuit, the following output resistance values will be set by the corresponding RDAC latch codes (applies to AD5253 R_{AB}=10kΩ potentiometers):

Dx (DEC)	R_{WB} (Ω)	Output State
63	9893Ω	Full-Scale
32	5050Ω	Mid-Scale
1	206Ω	1 LSB
0	50Ω	Zero-Scale (Wiper contact resistance)

Note that in the zero-scale condition a finite wiper resistance of 50Ω is present. Care should be taken to limit the current conduction between W and B in this state to a no more than ±5mA continuous or ±20mA pulse to avoid degradation or possible destruction of the internal switch contact.

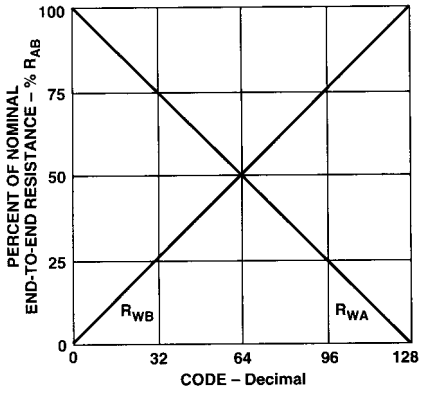


Figure 6. Symmetrical RDAC Operation

Like the mechanical potentiometer the RDAC replaces, the AD5253/AD5254 part is totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled resistance R_{WA}. Figure 6 shows the symmetrical programmability of the various terminal connections. When these terminals are used, the B–terminal should be tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general equation for this operation is:

$R_{WA}(Dx) = [(64-Dx)/64]*R_{AB} + 50\Omega$ (AD5253) eqn. 4

$R_{WA}(Dx) = [(256-Dx)/256]*R_{AB} + 50\Omega$ (AD5254) eqn. 5

For example, when $V_A = 0V$ and B–terminal is tied to the wiper W the following output resistance values will be set by the corresponding RDAC latch codes (applies to AD5253 R_{AB}=10kΩ potentiometers):

Dx (DEC)	R_{WA} (Ω)	Output State
63	206	Full-Scale
32	5050	Mid-Scale
1	9893	1 LSB
0	10050	Zero-Scale

The typical distribution of R_{AB} from channel-to-channel matches of less than ±1% within the same package. On the other hand, device to device matching is process lot dependent such that a maximum of ±30% variation is possible.

PROGRAMMING THE POTENTIOMETER DIVIDER
Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example connecting A–terminal to +5V and B–terminal to ground produces an output voltage at the wiper which can be any value starting at zero volts up to 1 LSB less than +5V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 2^N position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to terminals AB is:

$V_W(Dx) = (Dx/64) * V_{AB} + V_B$ (AD5253) eqn. 6

$V_W(Dx) = (Dx/256) * V_{AB} + V_B$ (AD5254) eqn. 7

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors and not the absolute value. Therefore, the drift reduces to 50ppm/°C.

ESD PROTECTION CIRCUITS

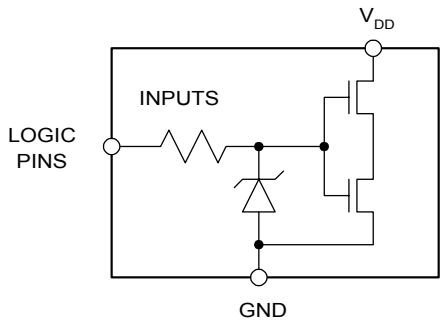


Figure 7A. Equivalent Digital Input ESD Protection

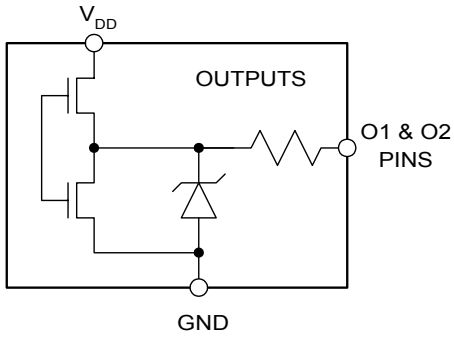


Figure 7B. Equivalent Digital Output ESD Protection

Figure 7 shows the equivalent ESD protection circuit for digital pins. Figure 8 shows the equivalent analog-terminal protection circuit for the variable resistors.

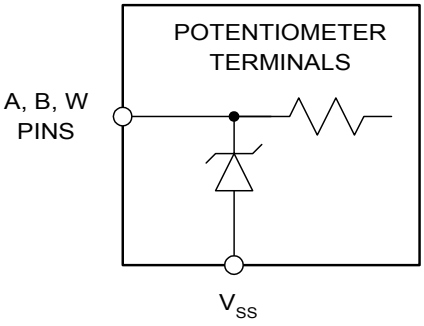


Figure 8. Equivalent VR-Terminal ESD Protection

TEST CIRCUITS

Figures 9 to 18 define the test conditions used in the product specification's table.

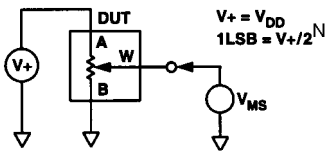


Figure 9. Potentiometer Divider Nonlinearity error test circuit (INL, DNL)

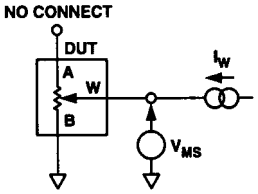


Figure 10. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

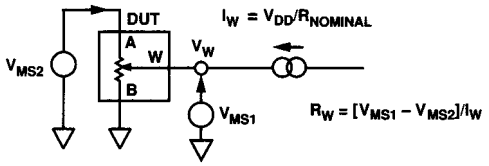


Figure 11. Wiper Resistance test Circuit

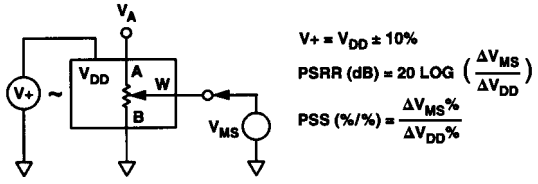


Figure 12. Power supply sensitivity test circuit (PSS, PSSR)

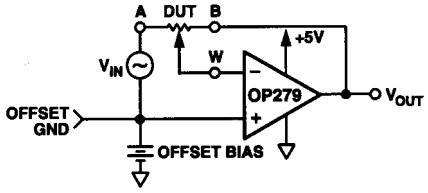


Figure 13. Inverting Gain test Circuit

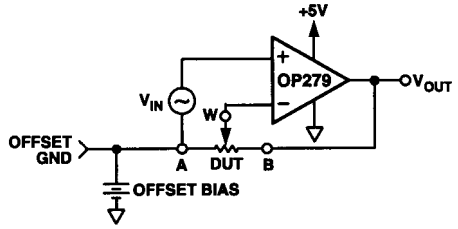


Figure 14. Non-Inverting Gain test circuit

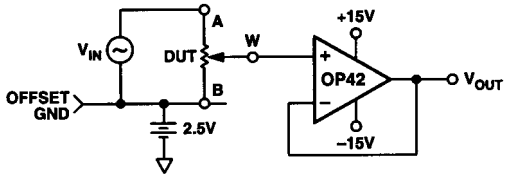


Figure 15. Gain Vs Frequency test circuit

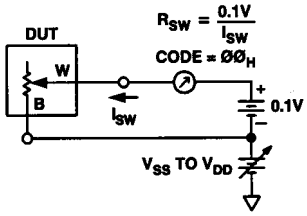


Figure 16. Incremental ON Resistance Test Circuit

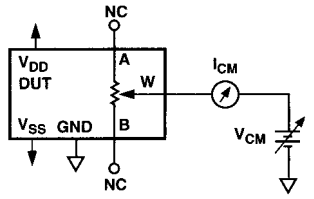


Figure 17. Common Mode Leakage current test circuit

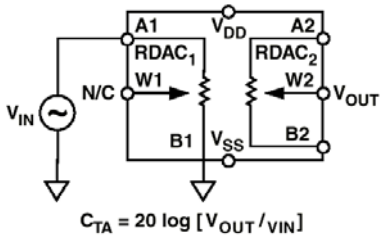


Figure 18. Analog Crosstalk Test Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)