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PWM Switching Regulator for High-performance Voltage Mode Control



ADE-204-012C (Z)

Rev.3 Jul. 2002

#### Description

The IC products in this series are primary control switching regulator control IC's appropriate for obtaining stabilized DC voltages from commercial AC power.

These IC's can directly drive power MOS FET's, they have a timer function built in to the secondary overcurrent protection, and they can perform intermittent operation or delayed latched shutdown as protection operations in unusual conditions. They can be used to implement switching power supplies with a high level of safety due to the wide range of built-in functionality.

#### Functions

- 6.45 V reference voltage
- Triangle wave generator
- Error amplifier
- Under voltage lockout protector
- PWM comparator
- Pulse-by-pulse current limitting
- Timer-latch current limitting (HA16107)
- ON/OFF timer function (HA16108)
- Soft start and quick shutdown
- Output circuit for power MOS FET driving

#### Features

- Operating frequencies up to a high 600 kHz
- Built-in pre-driver circuit for driving power MOS FET
- Built-in timer latch over-current protection function (HA16107)
- The OCL enables intermittent operation by an ON/OFF timer for prevention of secondary overcurrent. (HA16108)
- The UVL function (under voltage lockout) is applied to both Vin and Vref.
- ON/OFF reset: an auto-reset function which is based on the time constant of an external capacitor and observation of drops in Vin.
- Since the over-voltage protection function OVP (the TL pin) only observes voltage drops in Vin, it is possible to use the OVP and ON/OFF pin for independent purposes.
- Built-in 34 V Zener diode between Vin and ground.

#### **Ordering Information**

|           | Typical Threshold | d Voltage |                                   |         |
|-----------|-------------------|-----------|-----------------------------------|---------|
| Product   | UVL1              | OVP       | Notes                             | Package |
| HA16107P  | Hi: 16.2 V        | 7.0 V     | Timer latch protection            | DP-16   |
| HA16107FP | Lo: 9.5 V         |           |                                   | FP-16DA |
| HA16108P  | Hi: 16.2 V        | Hi: 7.0 V | On-off timer protection           | DP-16   |
| HA16108FP | Lo: 9.5 V         | Lo: 1.3 V | (intermittent operation possible) | FP-16DA |

#### **Pin Arrangement**



#### **Pin Functions**

• HA16107P, HA16108P

| Pin No. | Symbol          | Pin Functions                           |
|---------|-----------------|---|
| 1       | V <sub>IN</sub> | Input voltage                           |
| 2       | OUT             | Pulse output                            |
| 3       | CL (+)          | Current limiter                         |
| 4       | V <sub>E</sub>  | Output ground                           |
| 5       | CL (–)          | Current limiter                         |
| 6       | R <sub>T1</sub> | Timing resistor (rising time)           |
| 7       | C <sub>T</sub>  | Timing capacitor                        |
| 8       | R <sub>T2</sub> | Timing resistor (falling time)          |
| 9       | Vref            | Reference voltage output                |
| 10      | ST              | Soft start                              |
| 11      | IN (+)          | Error amp (+) input                     |
| 12      | GND             | Ground                                  |
| 13      | NC              | NC                                      |
| 14      | IN (–)          | Error amp (-) input                     |
| 15      | E/O             | Error output                            |
| 16      | TL, ON/OFF      | Timer latch (HA16107), ON/OFF (HA16108) |

| • HA16107FP, HA16108FP |                 |   |  |  |  |  |  |
|------------------------|-----------------|---|--|--|--|--|--|
| Pin No.                | Symbol          | Pin Functions                           |  |  |  |  |  |
| 1                      | V <sub>IN</sub> | Input voltage                           |  |  |  |  |  |
| 2                      | OUT             | Pulse output                            |  |  |  |  |  |
| 3                      | CL (+)          | Current limiter                         |  |  |  |  |  |
| 4                      | GND             | Ground                                  |  |  |  |  |  |
| 5                      | GND             | Ground                                  |  |  |  |  |  |
| 6                      | R <sub>T1</sub> | Timing resistor (rising time)           |  |  |  |  |  |
| 7                      | C <sub>T</sub>  | Timing capacitor                        |  |  |  |  |  |
| 8                      | R <sub>T2</sub> | Timing resistor (falling time)          |  |  |  |  |  |
| 9                      | Vref            | Reference voltage output                |  |  |  |  |  |
| 10                     | ST              | Soft start                              |  |  |  |  |  |
| 11                     | IN (+)          | Error amp (+) input                     |  |  |  |  |  |
| 12                     | GND             | Ground                                  |  |  |  |  |  |
| 13                     | GND             | Ground                                  |  |  |  |  |  |
| 14                     | IN (–)          | Error amp (-) input                     |  |  |  |  |  |
| 15                     | E/O             | Error output                            |  |  |  |  |  |
| 16                     | TL, ON/OFF      | Timer latch (HA16107), ON/OFF (HA16108) |  |  |  |  |  |

#### **Block Diagram**





#### **Function and Timing Chart**

#### **Triangle Waveform and PWM Output**



1. Timing in Normal Operation

Timing in these ICs is based on a triangular voltage waveform. The rising edge (leading edge) defines the deadband time  $t_{DB}$ . The falling edge (trailing edge) defines the ON-duty control band  $t_{ON}$ . PWM output is on in the area within  $t_{ON}$  that is bounded above by the triangle wave  $V_{CT}$  and error output  $V_{E/O}$ . The following pin outputs are related to PWM control:

- $C_{T}$  (pin 7): triangle-wave voltage output
- E/O (pin 15): error output voltage
- R<sub>12</sub> (pin 8): ON-duty pulse output voltage
- OUT (pin 2): PWM pulse output (for driving the gate of a power MOS FET)
- 2. Triangle Oscillator, Waveform and Frequency

The triangle oscillator in these ICs generates a triangular waveform by charging and discharging timing capacitor  $C_{\tau}$  with a constant current, as shown in the equivalent circuit. The  $C_{\tau}$  charge current is:

$$I(C_{Tchg}) = I_1 = \frac{V_{REF} - 2V_{BE}}{R_{T1}}$$

The discharge current is:

$$I(C_{Tdischg}) = 2I_2 - I_1, \text{ where } I_2 = \frac{V_{REF} - 2V_{BE}}{R_{T2}}$$

In these equations Vref (reference voltage) is typically 6.45 V, and  $V_{BE}$  (base-emitter voltage of internal transistors) is about 0.7 V.

The deadband time is:

$$t_{DB} = \frac{C_T \times R_{T1} \times 2V}{V_{REF} - 2V_{BE}} + 0.25 \ \mu s$$
$$\approx 0.4 \times C_T \times R_{T1} + 0.25 \ \mu s$$

The ON-duty time is:

$$t_{ON} = t_{DB} \times \frac{R_{T2}}{2R_{T1} - R_{T2}}$$

The 0.25  $\mu$ s in these equations is a correction term for internal circuit delays.

The maximum ON-duty is

$$Du \max = \frac{R_{T2}}{2R_{T1}}$$

The oscillating frequency is:

$$f_{OSC} = \frac{\frac{1}{0.4 C_{T} R_{T1} + 0.25 \mu} + 0.25 \mu}{1 - \frac{R_{T2}}{2R_{T1}}} + \frac{1}{1 - \frac{R_{T2}}{2R_{T1}}} + \frac{1}{0.8 C_{T} R_{T1}^{2} + 0.25 \mu \times 2R_{T1}} + 0.25 \mu}$$
(Hz)

When  $R_{T1} = R_{T2}$ , the maximum ON-duty is 50%, and:

$$f_{OSC} \approx \frac{1}{0.8 \text{ C}_{T} \text{ R}_{T1} + 0.25 \,\mu \times 2 + 0.25 \,\mu}$$
$$= \frac{1}{0.8 \text{ C}_{T} \text{ R}_{T1} + 0.75 \,\mu} \text{ (Hz)}$$

This approximation is fairly close, but it should be checked in-circuit.

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3. Programming of Maximum ON-Duty (Du Max)

The preceding equations should be used to program the deadband or maximum ON-duty. The following table gives a summary.

| Condition            | $R_{_{T1}} > R_{_{T2}}$ | $\mathbf{R}_{T1} = \mathbf{R}_{T2}$ | $R_{_{T1}} < R_{_{T2}}$ |
|----------------------|-------------------------|-------------------------------------|-------------------------|
| Triangle<br>waveform |                         |                                     |                         |
| Du max               | Less than 50%           | 50%                                 | Greater than 50%*       |
| NI 1 1 1             |                         |                                     |                         |

Note: In a primary-control switching regulator, Du Max > 50% is dangerous because the transformer will saturate.

#### Soft Start and Quick Shutdown

One purpose of the soft-start function is to protect the switching controller and power MOS FET from surges at power-up. Another purpose is to let the secondary-side DC voltage rise smoothly.

When power goes off, the quick-shutdown function rapidly discharges the capacitor in the soft-start circuit (and at the same time switches the PWM output off) to prepare for the next power-on.

The soft-start function in these ICs lets the PWM output develop smoothly from zero to the designated pulse width at power-up. The soft-start voltage is the 3.8 V voltage value of an internal Zener diode, so the PWM output is able to start widening gradually as soon as the soft-start function starts operating. The soft-start function will start promptly even if  $C_{st}$  is large.

The soft-start and quick-shutdown modes are selected automatically in the IC, under control of the UVL signal.





#### Vref Protection Functions: Overvoltage and Undervoltage

Vref overvoltage and undervoltage conditions are detected by the overvoltage detection circuit and UVL2 circuit. PWM output shuts down when Vref  $\ge 8$  V. UVL2 detects undervoltage with hysteresis between approximately 4 V and 5 V. PWM output also shuts down below these voltages. It follows that PWM output will shut off whenever the Vref pin is shorted to the power supply (V<sub>IN</sub>) or ground (GND). PWM output also shuts off when V<sub>IN</sub> is turned on or off.

The following diagram shows how these protection functions operate when power comes on and goes off (Vref < 6.45 V), and when a high external voltage is applied to the Vref pin (Vref > 6.45 V).



#### 1. Current-Limiter Circuit

The current limiter pin (CL) is connected to the emitter of an npn transistor, as shown in the block diagram. The threshold voltage is 240 mV typ. The switching speed of this circuit is approximately 100 ns from detection of overcurrent to shut-down of PWM output. Switching speed increases with the strength of the signal input to the CL pin.

Instead of simple pulse-by-pulse current limiting, in these ICs the current limiting circuit is linked to the timer-and-latch or ON/OFF timer circuit, and also detects the degree of overcurrent. The overcurrent value is determined from the point at which current limiting is triggered in the ON-duty cycle. With a large overcurrent (causing current limiting to operate even at a small ON-duty), the IC automatically shortens the timer time.

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#### **Undervoltage Lockout and PWM Output**

The undervoltage lockout function turns off the PWM pulse output when the controller's supply voltage goes below a designated value. These ICs have two undervoltage lockout circuits. The UVL1 circuit senses the supply voltage  $V_{IN}$ . The UVL2 circuit senses the Vref voltage. A feature of these ICs is that PWM output is turned on only when both voltages are above designated values. Otherwise, the IC operates in standby mode.

The two built-in undervoltage lockout circuits make it possible to configure an extremely safe power supply system. PWM output will shut down under a variety of abnormal conditions, such as if Vref is shorted to ground while  $V_{IN}$  is applied.





#### **Timer Latch and ON/OFF Timer**

The HA16107 has a built-in timer-latch function. The HA16108 has a built-in ON/OFF timer function.

The timer-latch function is an overvoltage protection function that combines latched shutdown of PWM output with a timer function to vary the time until latched shutdown occurs according to the overcurrent value. A dedicated voltage detection pin is provided in addition to Vref overvoltage protection.

The ON/OFF timer function is equivalent to the above timer-latch function without the latch. If overcurrent is detected continuously, PWM output shuts down temporarily, then normal operation resumes. This process repeats, temporary shutdown alternating with normal operation.

Both the timer-latch function in the HA16107 and the ON/OFF function in the HA16108 wait for an interval after overcurrent detection before shutting down PWM output. The interval is determined by capacitor  $C_{TM}$  and the value of the charge/discharge current supplied internally from the IC. Normal operation therefore continues if a single overcurrent spike is detected, while if continuous overcurrent is detected, the current and voltage droop curves for the secondary-side output have sharp characteristics.

- 1. Use of Timer-Latch Pin (HA16107)
- Timer-Latch Usage

See external circuit 1 in the following diagram. Under continuous overcurrent, the CML switch turns on, charging  $C_{TM}$  with 12  $\mu$ A. PWM output shuts down when the voltage at pin 15 exceeds 7 V.

Overvoltage Protection Usage

See external circuit 2 in the diagram. This configuration is suitable when overvoltage is detected by an OVP signal received through an optocoupler from the DC output on the secondary side of an AC/DC converter. PWM output shuts down when the OVP signal allows the voltage at the TL pin to exceed 7 V. The shutdown is latched.  $V_{IN}$  must go below approximately 6.5 V ( $V_{INR}$ ) to release the latched state.



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- 2. Use of ON/OFF Timer Pin (HA16108)
- External Circuit



• ON/OFF Timer Operation



4. If the timer goes off during soft start or in the undervoltage lockout region, after recovery, output will come on after the soft-start time or after the rise time to the undervoltage lockout release point, which is determined by the time constant.

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#### **Absolute Maximum Ratings**

 $(Ta = 25^{\circ}C)$ 

| Item                        | Symbol            | Rating Value | Units | Notes |
|-----------------------------|-------------------|--------------|-------|-------|
| Supply voltage              | V <sub>IN</sub>   | 30           | V     |       |
| Output current (DC)         | I <sub>o</sub>    | ±0.2         | А     |       |
| Output current (peak)       | lopeak            | ±2           | А     |       |
| Current limiter voltage     | V <sub>cL</sub>   | +4, -1       | V     |       |
| Error amp input voltage     | V                 | Vref         | V     |       |
| E/O output voltage          | V <sub>IE/O</sub> | Vref         | V     |       |
| R <sub>T1</sub> pin current | I <sub>RT1</sub>  | 500          | μA    |       |
| $R_{T_2}$ pin current       | I <sub>RT2</sub>  | 5            | mA    |       |
| Power dissipation           | P <sub>T</sub>    | 680          | mW    | 1, 2  |
| Operating temperature range | Topr              | –20 to +85   | °C    |       |
| Storage temperature range   | Tstg              | -55 to +125  | °C    |       |

Notes: 1. For the "FP" products (SOP package), this value is when mounted on a 40 by 40 by 1.6 mm glass epoxy substrate. However, this value must be derated by 8.3 mW/°C from Ta =  $45^{\circ}$ C. When the wiring density is 10%, and 11.1 mW/°C from Ta =  $64^{\circ}$ C when the wiring density is 30%.

- For the "P" products (DIP package), this value is valid up to 45°C, and must be derated by 8.3 mW/°C above 45°C.
- 3. In the case of SOP, use center 4 pins, (4), (5), (12), (13) for solder-mounting and connect the wide ground pattern, because these pins are available for heat sink of this IC.



#### **Electrical Characteristics**

 $(Ta = 25^{\circ}C, V_{IN} = 18 V, f_{OSC} = 100 \text{ kHz})$ 

| Section           | Item   | Symbol              | Min  | Тур  | Max  | Unit | Test Conditions  | Note |
|-------------------|--|---------------------|------|------|------|------|--|------|
| Reference         | Output voltage                                     | Vref                | 6.10 | 6.45 | 6.80 | V    |  |      |
| voltage           | Line regulation                                    | Line                | —    | 30   | 60   | mV   | $12~V \leq V_{_{\rm IN}} \leq 30~V$  |      |
|                   | Load regulation                                    | Load                | —    | 30   | 60   | mV   | $0 \text{ mA} \le I_{o} \le 10 \text{ mA}$   |      |
|                   | Temperature<br>stability                           | ∆Vref/<br>∆Ta       | _    | 40   | _    | °C   |  |      |
|                   | Short circuit current                              | I <sub>os</sub>     | 30   | 50   |      | mA   | Vref = 0 V   |      |
|                   | Over voltage protec-<br>tion (Vref OVP<br>voltage) | Vrovp               | 7.4  | 8.0  | 9.0  | V    |  |      |
| Triangle          | Maximum frequency                                  | fmax                | 600  | _    | _    | kHz  |  |      |
| wave              | Minimum frequency                                  | fmin                | _    | _    | 1    | kHz  |  |      |
| gonorator         | Voltage stability                                  | $\Delta f/fo_1$     | _    | ±1   | ±3   | %    | $12 \text{ V} \le \text{V}_{\text{IN}} \le 30 \text{ V}$ $\text{fo}_1 = (\text{fmax} + \text{fmin})/2$ |      |
|                   | Temperature stability                              | $\Delta f/fo_2$     | —    | ±1   | —    | %    | $-20^{\circ}C \le Ta \le +85^{\circ}C$ $fo_{2} = (fmax + fmin)/2$                                      |      |
|                   | Frequency accuracy                                 | f <sub>osc</sub>    | 270  | 300  | 330  | kHz  | $R_{_{T1}} = R_{_{T2}} = 27 \text{ k}\Omega$<br>$C_{_{T}} = 120 \text{ pF}$                            |      |
| PWM<br>comparator | Minimum deadband pulse width                       | t <sub>DB</sub>     | _    | _    | 1.0  | μs   |  |      |
|                   | Low level threshold voltage                        | $V_{TL}$            | 1.9  | 2.2  | 2.5  | V    |  |      |
|                   | High level threshold                               | $V_{\rm TH}$        | 3.8  | 4.2  | 4.6  | V    |  |      |
|                   | Differential threshold                             | $\Delta V_{\rm TH}$ | 1.7  | 2.0  | 2.3  | V    |  |      |
|                   | Deadband width initial accuracy                    | ∆DB1                | _    | ±1   | ±3   | %    | $R_{T1} = R_{T2} = 27 \text{ k}\Omega$<br>$C_T = 470 \text{ pF}$                                       |      |
|                   | Deadband width voltage stability                   | ∆DB2                | _    | ±0.2 | ±2.0 | %    | $12 V \le V_{IN} \le 30 V$ $(Dmax - Dmin)/2$   |      |
|                   | Deadband width temperature stability               | $\Delta DB3$        | _    | ±1   | _    | %    | $-20^{\circ}C \le Ta \le +85^{\circ}C$<br>(Dmax - Dmin)/2  |      |
| Error amp         | Input offset voltage                               | V <sub>io</sub>     | —    | 2    | 10   | mV   |  |      |
|                   | Input bias current                                 | I <sub>IB</sub>     | —    | 0.8  | 2.0  | μA   |  |      |
|                   | Input sink current                                 | losink              | 80   | 140  | —    | μA   | V <sub>0</sub> = 2 V   |      |
|                   | Output source current                              | losource            | 80   | 140  |      | μA   | V <sub>o</sub> = 5 V   |      |

### **Electrical Characteristics** (cont.)

 $(Ta = 25^{\circ}C, V_{IN} = 18 \text{ V}, f_{OSC} = 100 \text{ kHz})$ 

| Section              | Item  | Symbol                | Min           | Тур    | Max           | Unit | <b>Test Conditions</b>                | Note |
|----------------------|---|-----------------------|---------------|--------|---------------|------|---------------------------------------|------|
| Error amp<br>(cont.) | High level output voltage                         | V <sub>oh</sub>       | Vref –<br>1.5 |        |               | V    | l <sub>o</sub> = 10 μA                |      |
|                      | Low level output voltage                          | V <sub>ol</sub>       | _             | _      | 0.5           | V    | l <sub>o</sub> = 10 μA                |      |
|                      | Voltage gain                                      | G <sub>v</sub>        | _             | 55     | _             | dB   | f = 10 kHz                            |      |
|                      | Band width  | BW                    | _             | 15     | _             | MHz  |                                       |      |
|                      | (–) Common mode<br>voltage                        | V <sub>cm</sub> -     | 1.2           | _      |               | V    |                                       |      |
|                      | (+) Common mode<br>voltage                        | V <sub>CM</sub> +     | _             | _      | Vref –<br>1.5 | V    |                                       |      |
| Over-                | (+) Threshold voltage                             | $V_{TH}$ +            | 0.216         | 0.240  | 0.264         | V    |                                       |      |
| current<br>detector  | (+) Bias current                                  | l <sub>B</sub> +      | —             | 180    | 250           | μA   | $V_{cL}$ + = 0 V                      |      |
| uelecioi             | (-) Threshold voltage                             | V <sub>TH</sub> -     | -0.264        | -0.240 | -0.216        | V    |                                       | 1, 2 |
|                      | (-) Bias current                                  | I <sub>B</sub> —      | _             | 950    | 1350          | μA   | $V_{_{\rm CL}} = -0.3 \text{ V}$      | 1, 2 |
|                      | Response time                                     | t <sub>off</sub>      | _             | 100    |               | ns   | CL; open<br>V <sub>CL</sub> = +0.35 V |      |
| Soft start           | High level voltage                                | $V_{_{\mathrm{STH}}}$ | 3.2           | 3.8    | 4.4           | V    | lsink = 1 mA                          |      |
|                      | Sink current                                      | Isink                 | 7             | 10     | 13            | μA   | V <sub>st</sub> = 2.0 V               |      |
| Under<br>voltage     | V <sub>IN</sub> high level thre-<br>shold voltage | $V_{\rm inth}$        | 14.7          | 16.2   | 17.7          | V    |                                       |      |
| lockout 1            | V <sub>IN</sub> low level thre-<br>shold voltage  | $V_{\rm intl}$        | 8.5           | 9.5    | 10.5          | V    |                                       |      |
|                      | Threshold differential voltage                    | $\Delta V_{\rm TH}$   | 5.2           | 6.2    | 7.2           | V    | $(V_{INTH} - V_{INTL})$               |      |
| Under<br>voltage     | Vref high level thre-<br>shold voltage            | $V_{\rm rTH}$         | 4.5           | 5.0    | 5.5           | V    |                                       |      |
| lockout 2            | Vref low level thre-<br>shold voltage             | $V_{\rm rTL}$         | 3.5           | 4.0    | 4.5           | V    |                                       |      |
| Natas, 1             |   |                       | 1410100       | -      |               |      |                                       |      |

Notes: 1. Only applies to the HA16107P, HA16108P

2. The terminal should not be applied under -1.0 V.

#### Electrical Characteristics (cont.)

#### $(Ta = 25^{\circ}C, V_{IN} = 18 V, f_{OSC} = 100 \text{ kHz})$

| Section             | Item   | Symbol            | Min                     | Тур | Max | Unit | Test Conditions   | Note |
|---------------------|--|-------------------|-------------------------|-----|-----|------|---|------|
| Timer latch, ON/OFF | Latch threshold voltage                      | $V_{\text{THH}}$  | 6.5                     | 7.0 | 7.5 | V    |   |      |
| timer**             | $V_{IN}$ reset voltage                       | $V_{_{\rm INR2}}$ | 6.0                     | 6.5 | 7.0 | V    |   |      |
|                     | Reset voltage                                | $V_{\rm THL2}$    | 1.0                     | 1.3 | 1.6 | V    |   | 1    |
|                     | Differential threshold<br>to UVL low voltage | ΔV                | 2.0                     | 3.0 | _   | V    | $(V_{INTL} - V_{INR2})$   |      |
|                     | Source current<br>(OCL mode)                 | Isource           | 8                       | 12  | 16  | μA   | Over current detection mode   |      |
|                     | Sink current<br>(latch mode)                 | Isink             | 2.5                     | 4   | 5.5 | μA   | TL(ON/OFF)<br>terminal = 4 V  |      |
| Output              | Low voltage                                  | V <sub>ol1</sub>  | _                       | 1.7 | 2.2 | V    | losink = 0.2 A  |      |
|                     | High voltage                                 | V <sub>OH</sub>   | V <sub>⊪</sub> −<br>2.2 | _   | —   | V    | losource = 0.2 A  |      |
|                     | Low voltage<br>(standby mode)                | $V_{ol2}$         | _                       | —   | 0.5 | V    | losink = 1 mA   |      |
|                     | Rising time                                  | t,                | —                       | 40  | _   | ns   | C <sub>L</sub> = 1000 pF  |      |
|                     | Falling time                                 | t <sub>r</sub>    | _                       | 60  | _   | ns   | $C_{L} = 1000 \text{ pF}$   |      |
| Total               | Standby current                              | lst               | _                       | 160 | 250 | μA   | V <sub>IN</sub> = 14 V  |      |
|                     | Operation current                            | I <sub>IN1</sub>  | _                       | 16  | 20  | mA   | V <sub>IN</sub> = 30 V,<br>C <sub>L</sub> = 1000 pF,<br>f = 100 kHz |      |
|                     | Operation current                            | I <sub>IN2</sub>  | —                       | 12  | 16  | mA   | $V_{IN} = 30 V,$<br>f = 100 kHz,<br>Output open                     |      |
|                     | ON/OFF latch<br>current                      | I <sub>IN3</sub>  | _                       | 350 | 460 | μA   | V <sub>IN</sub> = 14 V  |      |
|                     | V <sub>IN</sub> – GND Zener<br>voltage       | Vz                | 30                      | 34  | _   | V    |   |      |

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Notes: 1. Only applies to the HA16108P/FP.

2. Timer latch: HA16107P/FP. ON/OFF timer: HA16108P/FP.

#### Note on Standby Current

In the test circuit shown in figure 1, the operating current at the start of PWM pulse output is the standby current.

If the resistance connected externally to the Vref pin (including  $R_{T2}$ ) is smaller than that of the test circuit, the apparent standby current will increase.



Figure 1 Standby Current Test Circuit



#### **Application Note**

• Case:

When DC power is applied directly as the power supply of the HA16107/HA16108, without using the transformer backup coil.

• Phenomenon:

The IC may not be activated in the case of a circuit in which  $V_{IN}$  rises quickly (10 V/100 µs or faster), such as that shown in figure 2.

• Reason:

Because of the IC circuit configuration, the timer latch block operates first.

• Remedy (counter measure):

Take remedial action such as configuring a time constant circuit as shown in figure 3, to keep the  $V_{IN}$  rise speed below 10 V/100  $\mu$ s.

If the IC power supply consists of an activation resistance and backup coil, as in an AC/DC converter, The  $V_{IN}$  rise speed is usually around 1 V/100  $\mu$ s, and there is no risk of this phenomenon occurring.



Figure 2 Example of Circuit with Fast  $V_{IN}$  Rise Time



Figure 3 Sample Remedial Circuit

#### **Characteristic Curves**



























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#### **Error Amplifier Characteristic**



**Examples of Drooping Characteristics of Power Supplies Using these ICs** 



#### **Operating Circuit Example**







#### Application

#### 1. Use of Error Amplifier for Flyback Transformer Primary-Side Control

In this example, the fact that the transformer winding ratio and voltage ratio in Figure 1.1 are mutually proportional is made use of in a flyback transformer type AC-DC converter. As fluctuation of output voltage  $V_2$  also appears in IC power supply voltage  $V_3$ , this is divided by a resistance and amplified by an error amplifier. An advantage of this method is that a photocoupler need not be used, making it possible to configure a power supply with a small number of parts (this example cannot be applied to a forward transformer).



Figure 1.1 Error Amplifier Peripheral Circuitry Diagram

#### <Determining External Constants around Error Amplifier>

1. Detrrmining DC Characteristics

In Figure 1.1, the relational expression in the box is satisfied, and therefore parameters are determined based on this. The absolute value of the number of transformer windings is determined based on the equation  $N_1:N_2:N_3 = V_1:V_2:V_3$ , taking primary inductance into consideration. Next, IC operating voltage  $V_3$  is made around 11V to 18V, taking the UVL voltage into consideration. If  $V_3$  is too large, the power consumption of the IC will increase, causing heat emission problems. If  $V_3$  is too small, on the other hand, there will be problems with defective power supply start-up.

2. Determining Error Amplifier Gain vs. Frequency Characteristic

Taking the configuration in Figure 1.1, the error amplifier gain characteristic with respect to fluctuation of output voltage  $V_2$  is as shown in Figure 1.2.



Figure 1.2 Error Amplifier Characteristic

In Figure 1.2, the parameters are given by the following equations.

Gain

 $G1 = V3/V2 \times R3/R1$  $G2 = V3/V2 \times R4/R1$ 

Corner frequencies

G<sub>1</sub> is made around 30 to 50 dB, taking both regulation and stability into consideration.

 $f_1$  is made a lower value than commercial frequency ripple  $f_{AC}$ , thus preventing hunting (a system instability phenomenon).

Next,  $G_2$  is set to 0 dB or less as a guideline, so that there is no gain in IC operating frequency  $f_{osc}$  (several tens to several hundreds of kHz).  $f_2$  should be set to a value that is substantially smaller than  $f_{osc}$ , and that is appropriate for the power supply response speed (several kHz). In the case of a bridge type rectification circuit, the commercial frequency ripple is twice the input frequency (with a 50 Hz commercial frequency,  $f_{AC} = 100$  Hz).

#### 2. External Constant Design for Current Detection Section (HA16107, HA16108, HA16666)

In the above IC models, which incorporate a current detection function, a low-pass filter such as shown in Figure 2.1 must be inserted between switch element current detection resistance  $R_{cs}$  and the current detection pin of the IC.



Figure 2.1 Current Detection Circuit

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The reason for this is that, when the switch element is on in each cycle, there is an impulse current associated with charging of transformer floating capacitance  $C_x$ , and IC current detection malfunctions (see Figure 2.2).



Figure 2.2 Current Detection Waveform

#### <Setting Numeric Values>

If the switch element current to be detected is designated  $I_{D}$ , and the current detection resistance  $R_{CS}$ , then the following equation is satisfied using the parameters in Figure 2.1.

$$I_{D} \times R_{CS} = ((R_{A} + R_{B})/R_{B}) V_{TH}$$

 $V_{_{TH}}$  is the detection level voltage of the IC (240 mV in the case of the HA16107, for example).  $R_{_A}$  and  $R_{_B}$  are set to values on the order of several hundred  $\Omega$  to several k $\Omega$ , so that  $R_{_{CS}}$  is not affected. Next, the filter cutoff frequency is set according to the following equation.

$$f_{c} = 1/(2\pi C_{A} (R_{A}/R_{B}))$$

 $f_c$  can be found with the following guideline, using IC operating frequency  $f_{osc}$ , power supply rating onduty D, and power MOS element turn-on time  $t_{osc}$ .

 $fosc/D \le f_{c} \le 1/(100 \times t_{on})$ 

Value 100 in the above equation provides a margin for noise, ringing, and so forth.

#### <Actual Example>

In an SW power supply using an HA16107, with a 100 kHz operating frequency and a D value of 30%, the relevant values were as follows:  $V_{B} = 140 \text{ V}$ ,  $C_{X} = 80 \text{ pF}$ ,  $t_{ON} = 10 \text{ ns}$ . Thus, when  $R_{CS} = 1 \Omega$ , the  $V_{11}$  level peak value reaches the following figure.

$$\begin{split} \mathsf{V}_{_{11}} \text{ (peak)} &= \mathsf{R}_{_{\mathrm{CS}}} \times \mathsf{I}_{_{\mathrm{D}}} \text{ peak} \\ &= \mathsf{R}_{_{\mathrm{CS}}} \times (\mathsf{V}_{_{\mathrm{B}}} \times C_{_{X}})/t_{_{\mathrm{ON}}} \\ &= 1\Omega \times (140 \text{ V} \times 80 \text{ pF})/10 \text{ ns} \\ &= 1.12 \text{ (V)} \end{split}$$

A filter with the following constants was then inserted.

 $R_{A} = R_{B} = 1 \text{ k}\Omega, C_{A} = 1000 \text{ pF}$ 

At this time, the detectable drain current is 0.48 (A), and the filter cutoff frequency is 318 (kHz). Note that increasing a filter time constant is effective against noise, but if the value is too large, error will arise in the switch element current detection level.

#### 3. IC Heat Emission Problem and Countermeasures (HA16107 Series, HA16114 Series)

While the above ICs can directly drive a power MOS FET gate, if the method of use is not thoroughly investigated, there will be a tendency for the gate drive power to increase and a problem of heat emission by the IC may occur.

This section should therefore be noted and appropriate measures taken to prevent this kind of problem.

1. Power MOS FET Drive Characteristics

When power MOS FET drive is performed, in order to lower the on-resistance sufficiently, overdrive is normally performed with a voltage considerably higher than 5 V, for example, such as the 15 V power supply voltage of the IC.

At this time, the power that should be supplied from the IC to the power MOS FET is determined by gate load Qg in Figure 4.2.

2. IC Heat-Emission Power Calculation (Figure 4.2)

The power that contributes to IC heat emission is calculated by means of the following equation.  $Pd = V_{IN} I_{O} + 2Qg V_{IN} f$ 

Where

 $V_{IN}$ : Power supply voltage of IC

- I<sub>o</sub> : Operating current of IC (unloaded)
- Qg : Above-mentioned gate load
- f : Operating frequency of IC

The coefficient, 2, indicates that gate discharging also contributes to heat emission.

#### 4. Power MOS FET Gate Resistance Design (HA16107 Series, HA16114 Series)

There are the following three purposes in connecting a gate resistance, and the circuit is generally of the kind shown in Figure 4.1.

- (1) To suppress peak current due to gate charging
- (2) To protect IC output pins
- (3) To provide drive appropriate to power MOS FET input characteristics



Figure 4.1 Gate Drive Circuit

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This gate resistance  $R_{g}$  is given by the following equation.

 $\mathbf{R}_{_{\mathrm{G}}}=(\mathbf{V}_{_{\mathrm{G}}}\!/\mathbf{I}_{_{\mathrm{G}}})-(\mathbf{V}_{_{\mathrm{G}}}\times t_{_{\mathrm{ON}}})\!/\mathbf{Qg}, \quad \mathbf{R}_{_{\mathrm{G}}}=\mathbf{R}_{_{\mathrm{G1}}}+\mathbf{R}_{_{\mathrm{G2}}}$ 

- $I_{G}$  : Gate input peak current
- $V_{G}$  : Gate drive voltage wave high value (equal to power supply voltage of IC)
- $t_{on}$  : Power MOS FET turn-on time
- t<sub>OFF</sub> : Power MOS FET turn-off time
- Qg : Gate charge according to Figure 4.2



Figure 4.2 Power MOS FET Dynamic Input Characteristics

Refer to the power MOS FET catalog for information on  $t_{oN}$  and Qg.

By dividing  $R_{G}$  into  $R_{G1}$  and  $R_{G2}$ , it is possible for speed to be slowed when the power MOS FET is on, and increased when off.

Power MOS FET on and off times when mounted,  $t_{oN}$ ' and  $t_{oFF}$ ', are as follows.

$$\begin{split} t_{_{ON}}' &= t_{_{ON}} + Qg(R_{_{G1}} + R_{_{G2}})/V_{_{G}} \\ t_{_{OFF}}' &= t_{_{OFF}} + Qg \cdot R_{_{G2}}/V_{_{G}} \end{split}$$

#### <Actual Example>

When driving a power MOS FET and 2SK1567 with an HA16107, etc.

 $(R_{G1} = 100 \Omega, R_{G2} = 20 \Omega, V_G = 15 V)$ 

, i = 70 ns + 36 nc  $\cdot$  (100  $\Omega$  + 20  $\Omega)/(15$  V) = 360 (ns)

t\_{\_{OFF}}' = 135 ns + 36 nc  $\cdot$  (20  $\Omega)/(15 \text{ V})$  = 183 (ns)

Generally, the gate resistance values in the case of this circuit configuration are on the order of 100 to 470  $\Omega$  for R<sub>G1</sub> and 10 to 47  $\Omega$  for R<sub>G2</sub>.

#### **Package Dimensions**





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