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HM62A16100I Series

Wide Temperature Range Version
16 M SRAM (1-Mword × 16-bit)

Description

The Renesas HM62A16100I Series is 16-Mbit static RAM organized 1-Mword × 16-bit. HM62A16100I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has the package variations of 48-bump chip size package with 0.75 mm bump pitch for high density surface mounting.

Features

- Single 1.8 V supply: 1.65 V to 2.2 V
- Fast access time: 70 ns (max)
- Power dissipation:
    — Active: 3.6 mW/MHz (typ)
    — Standby: 0.9 μW (typ)
- Completely static memory.
    — No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
    — Three state output
- Battery backup operation.
    — 2 chip selection for battery backup
- Temperature range: −40 to +85°C

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Ordering Information

Type No.	Access time	Package
HM62A16100LBPI-7	70 ns	48-bump CSP with 0.75 mm bump pitch (TBP-48F)
HM62A16100LBPI-7SL	70 ns	

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Pin Arrangement

48-bumps CSP

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CS2
B	I/O8	$\overline{UB}$	A3	A4	$\overline{CS1}$	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	V_{SS}	I/O11	A17	A7	I/O3	V_{CC}
E	V_{CC}	I/O12	V_{SS}	A16	I/O4	V_{SS}
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	A19	A12	A13	$\overline{WE}$	I/O7
H	A18	A8	A9	A10	A11	NU

(Top view)
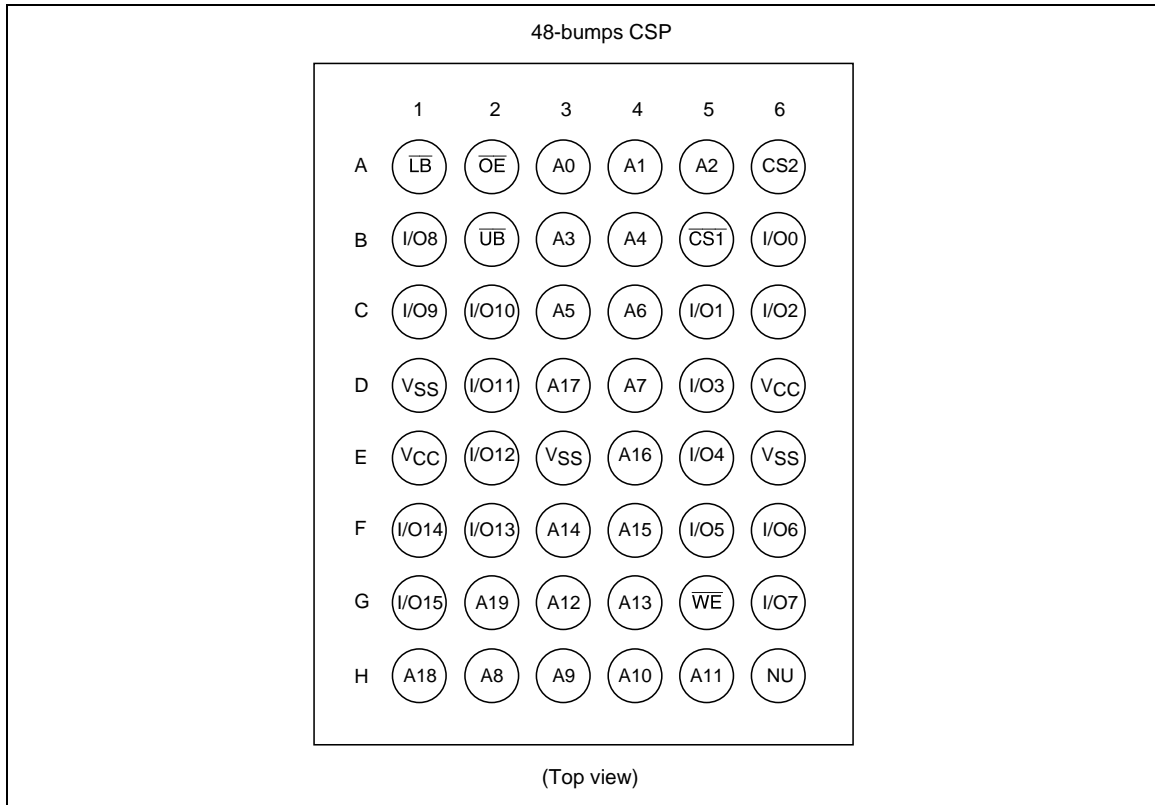
Pin Description

Pin name	Function
A0 to A19	Address input
I/O0 to I/O15	Data input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
LB	Lower byte select
UB	Upper byte select
V_{cc}	Power supply
V_{ss}	Ground
NU[1]	Not used (test mode pin)

Note: 1. This pin should be connected to a ground (V_{ss}), or not be connected (open).

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Block Diagram
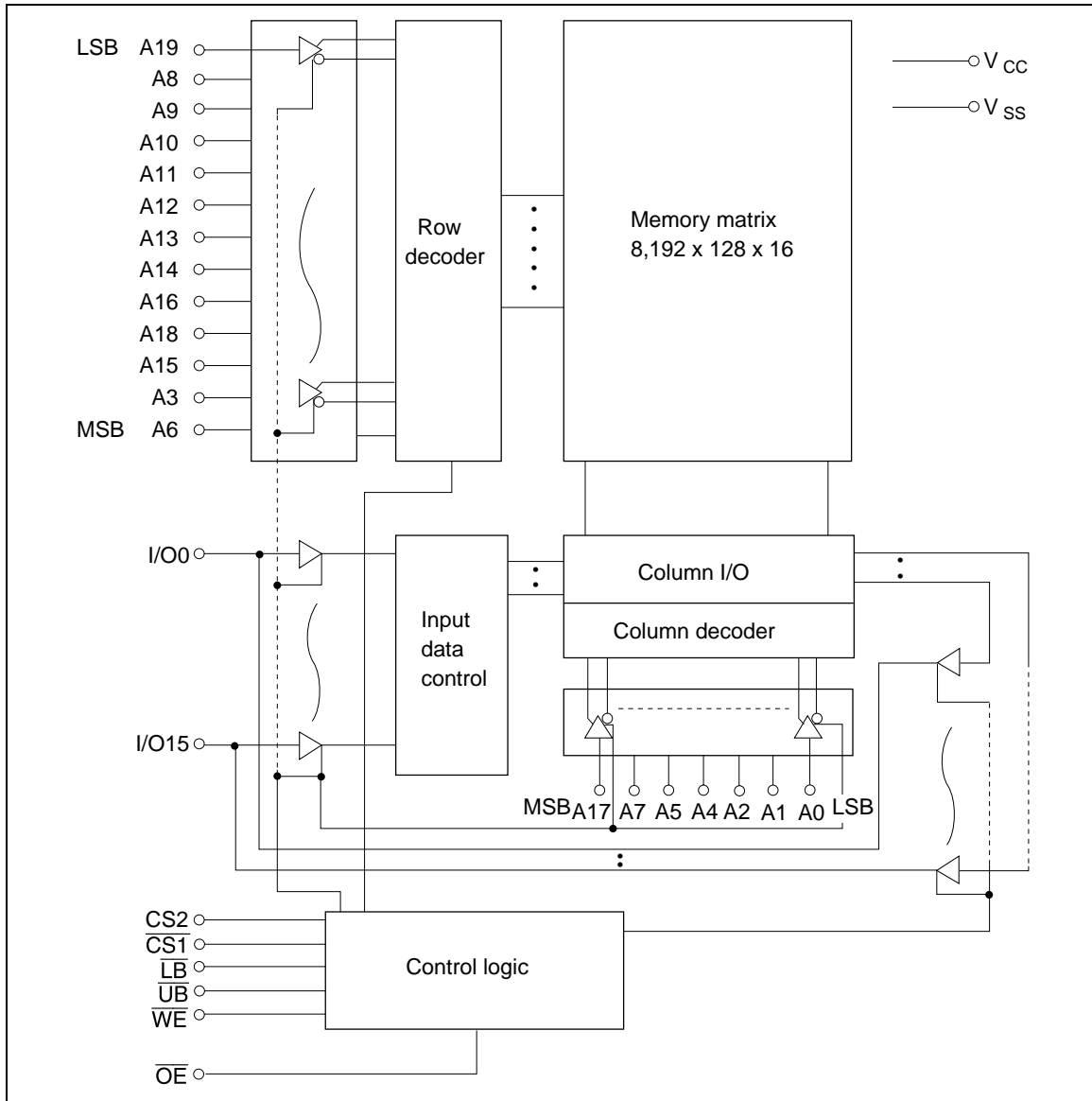
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Operation Table

CS1	CS2	WE	OE	UB	LB	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	−0.3 to + 2.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	−0.3[*1] to V_{CC} + 0.3[*2]	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−40 to +85	°C

Notes: 1. V_T min: −2.0 V for pulse half-width ≤ 10 ns.
2. Maximum voltage is +2.6 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	1.65	1.8	2.2	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	$0.75 \times V_{CC}$	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	−0.3	—	$0.25 \times V_{CC}$	V	1
Ambient temperature range	Ta	−40	—	85	°C	

Note: 1. V_{IL} min: −2.0 V for pulse half-width ≤ 10 ns.

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DC Characteristics

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$|I_{LI}|$	—	—	1	µA	$V_{in} = V_{ss}$ to V_{cc}
Output leakage current	$|I_{LO}|$	—	—	1	µA	$CS1 = V_{IH}$ or $CS2 = V_{IL}$ or $OE = V_{IH}$ or $WE = V_{IL}$ or $LB = UB = V_{IH}$, $V_{I/O} = V_{ss}$ to V_{cc}
Operating current	I_{CC}	—	—	8	mA	$CS1 = V_{IL}$, $CS2 = V_{IH}$, Others $= V_{IH}/V_{IL}$, $I_{I/O} = 0$ mA
Average operating current	I_{CC1}	—	20	30	mA	Min. cycle, duty = 100%, $I_{I/O} = 0$ mA, $CS1 = V_{IL}$, $CS2 = V_{IH}$, Others $= V_{IH}/V_{IL}$
	I_{CC2}	—	2	5	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O} = 0$ mA, $CS1 \leq 0.2$ V, $CS2 \geq V_{cc} - 0.2$ V, $V_{IH} \geq V_{cc} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current	I_{SB}	—	0.1	0.5	mA	$CS2 = V_{IL}$
Standby current	I_{SB1} *2	—	0.5	25	µA	0 V $\leq V_{in}$ (1) 0 V $\leq CS2 \leq 0.2$ V or (2) $CS1 \geq V_{cc} - 0.2$ V, $CS2 \geq V_{cc} - 0.2$ V or (3) $LB = UB \geq V_{cc} - 0.2$ V, $CS2 \geq V_{cc} - 0.2$ V, $CS1 \leq 0.2$ V Average value
	I_{SB1} *3	—	0.5	8	µA	
Output high voltage	V_{OH}	$V_{cc} - 0.2$	—	—	V	$I_{OH} = -100$ µA
Output low voltage	V_{OL}	—	—	0.2	V	$I_{OL} = 100$ µA

Notes: 1. Typical values are at $V_{cc} = 1.8$ V, Ta = +25°C and not guaranteed.
2. This characteristic is guaranteed only for L-version.
3. This characteristic is guaranteed only for L-SL version.

Capacitance

(Ta = +25°C, f = 1.0 MHz)

| Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	8	pF	$V_{in} = 0$ V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0$ V	1

Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics

(Ta = −40 to +85°C, V_{CC} = 1.65 V to 2.2 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.2 V, V_{IH} = V_{CC} − 0.2 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: $0.5 \times V_{CC}$
- Output load: See figures (Including scope and jig)
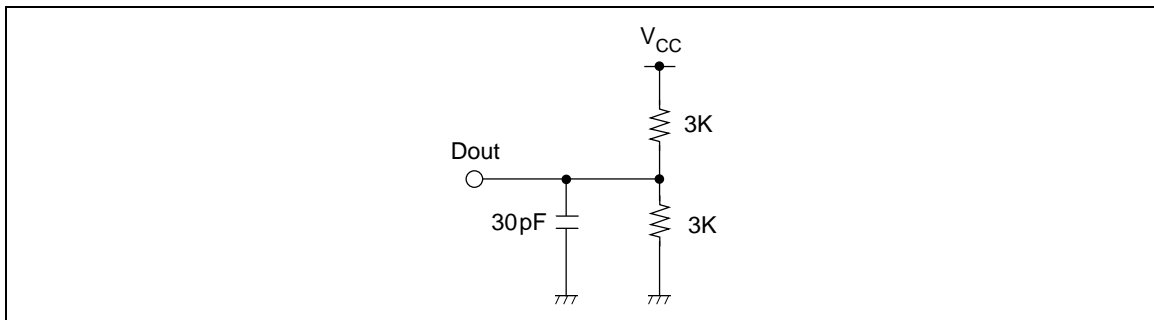
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Read Cycle

Parameter	Symbol	HM62A16100I -7 Min	Max	Unit	Notes
Read cycle time	t_{RC}	70	—	ns	
Address access time	t_{AA}	—	70	ns	
Chip select access time	t_{ACS1}	—	70	ns	
	t_{ACS2}	—	70	ns	
Output enable to output valid	t_{OE}	—	35	ns	
Output hold from address change	t_{OH}	10	—	ns	
LB, UB access time	t_{BA}	—	70	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	ns	2, 3
	t_{CLZ2}	10	—	ns	2, 3
LB, UB enable to low-Z	t_{BLZ}	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ1}	0	25	ns	1, 2, 3
	t_{CHZ2}	0	25	ns	1, 2, 3
LB, UB disable to high-Z	t_{BHZ}	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	25	ns	1, 2, 3

Write Cycle

Parameter	Symbol	HM62A16100I -7 Min	Max	Unit	Notes
Write cycle time	t_{WC}	70	—	ns	
Address valid to end of write	t_{AW}	60	—	ns	
Chip selection to end of write	t_{CW}	60	—	ns	5
Write pulse width	t_{WP}	50	—	ns	4
LB, UB valid to end of write	t_{BW}	60	—	ns	
Address setup time	t_{AS}	0	—	ns	6
Write recovery time	t_{WR}	0	—	ns	7
Data to write time overlap	t_{DW}	30	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Output active from end of write	t_{OW}	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	25	ns	1, 2
Write to output in high-Z	t_{WHZ}	0	25	ns	1, 2

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Notes: 1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

4. A write occurs during the overlap of a low CS1, a high CS2, a low WE and a low LB or a low UB. A write begins at the latest transition among CS1 going low, CS2 going high, WE going low and LB going low or UB going low. A write ends at the earliest transition among CS1 going high, CS2 going low, WE going high and LB going high or UB going high. t_{WP} is measured from the beginning of write to the end of write.

5. t_{CW} is measured from the later of CS1 going low or CS2 going high to the end of write.

6. t_{AS} is measured from the address valid to the beginning of write.

7. t_{WR} is measured from the earliest of CS1 or WE going high or CS2 going low to the end of write cycle.
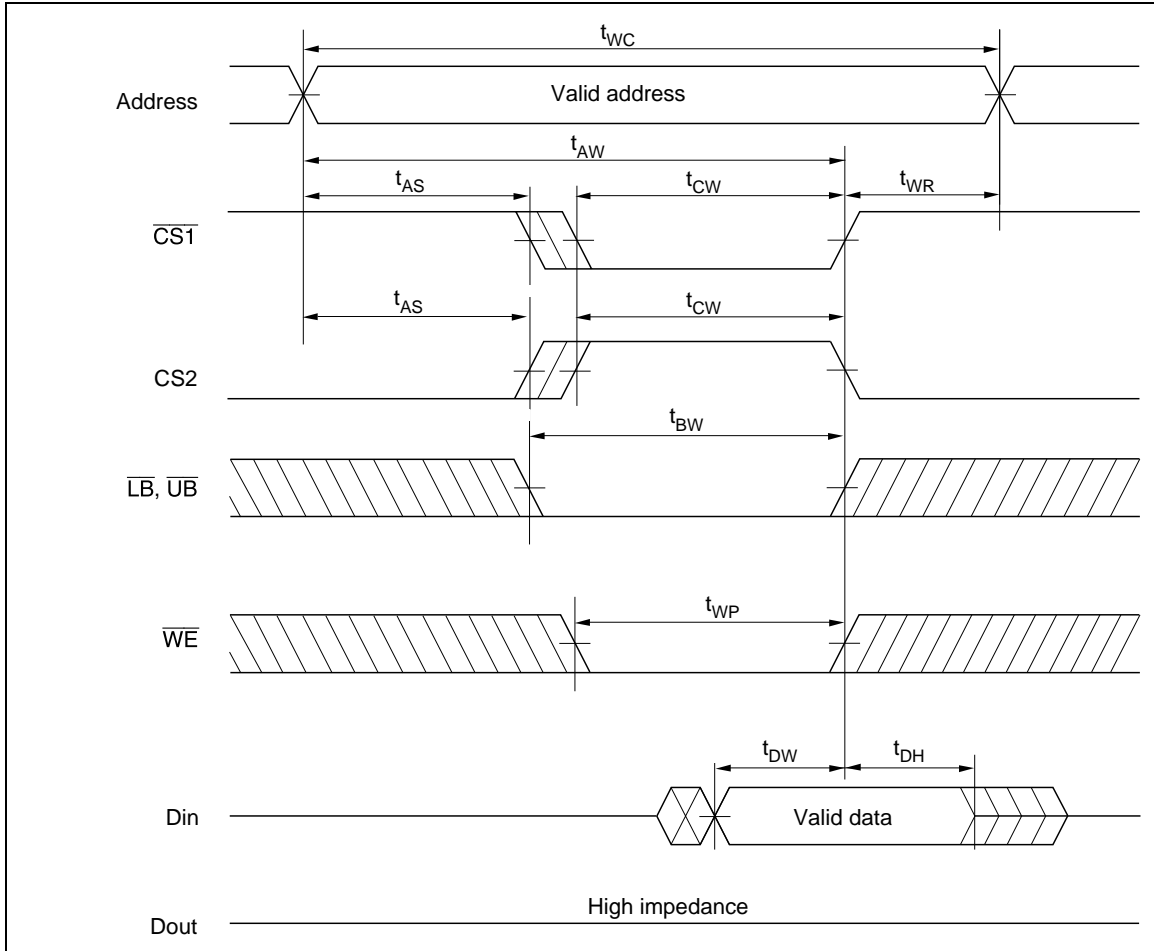
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Timing Waveform

Read Cycle
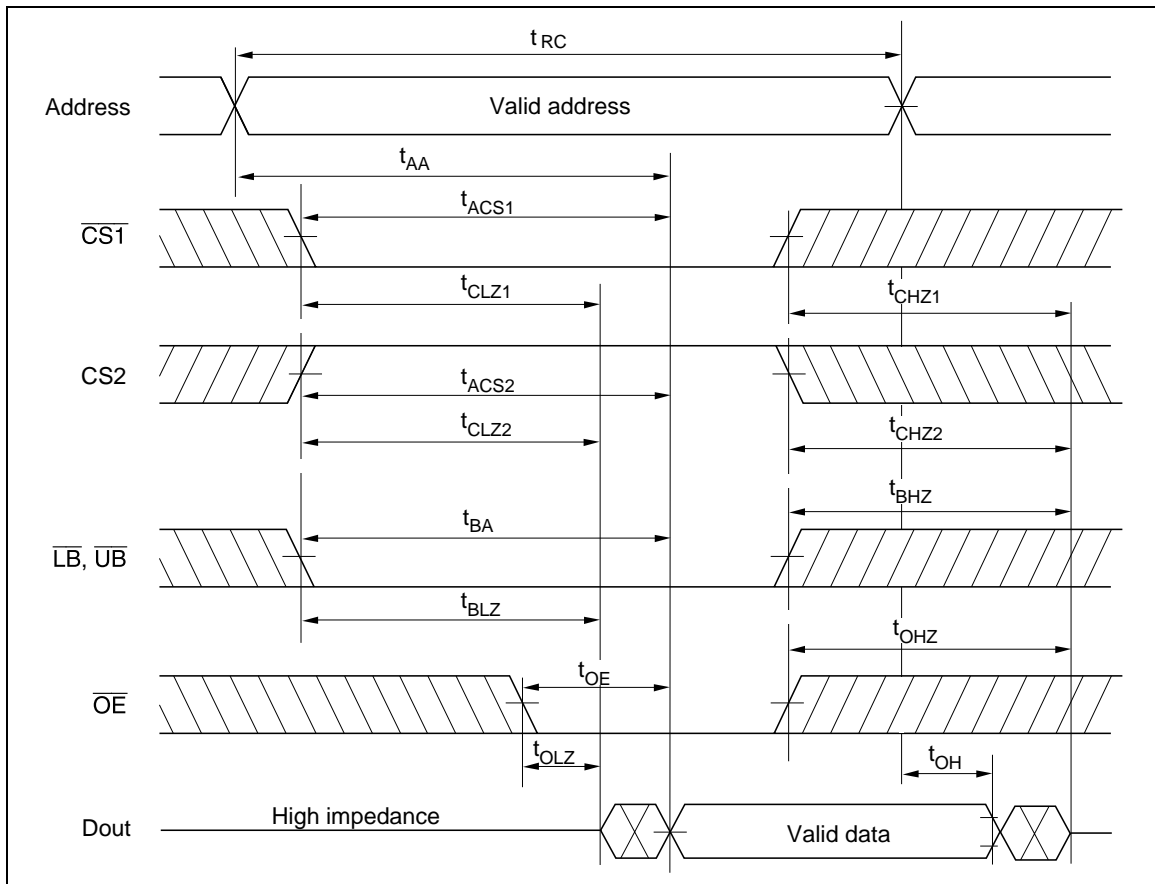
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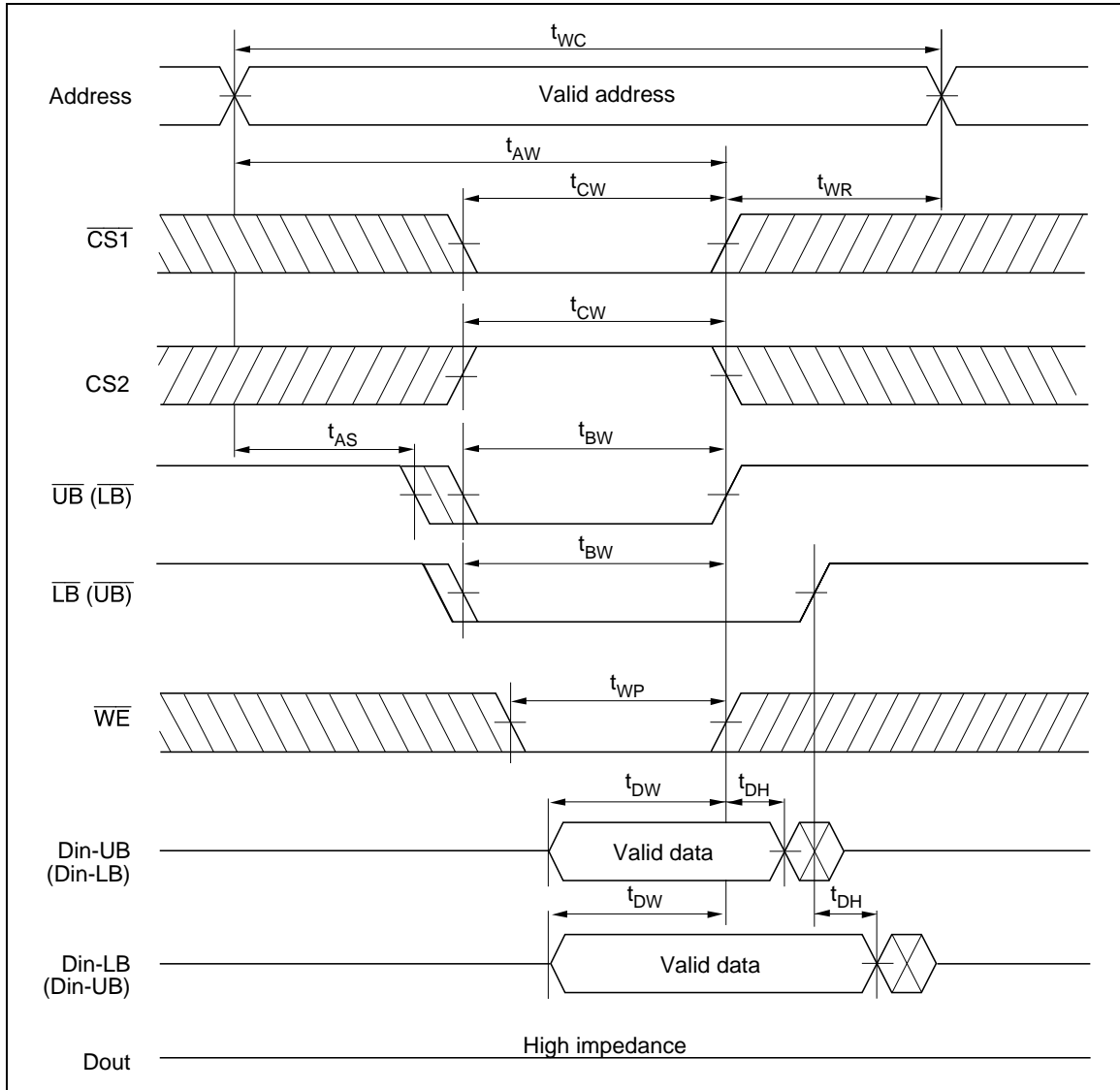
Write Cycle (1) (WE Clock)
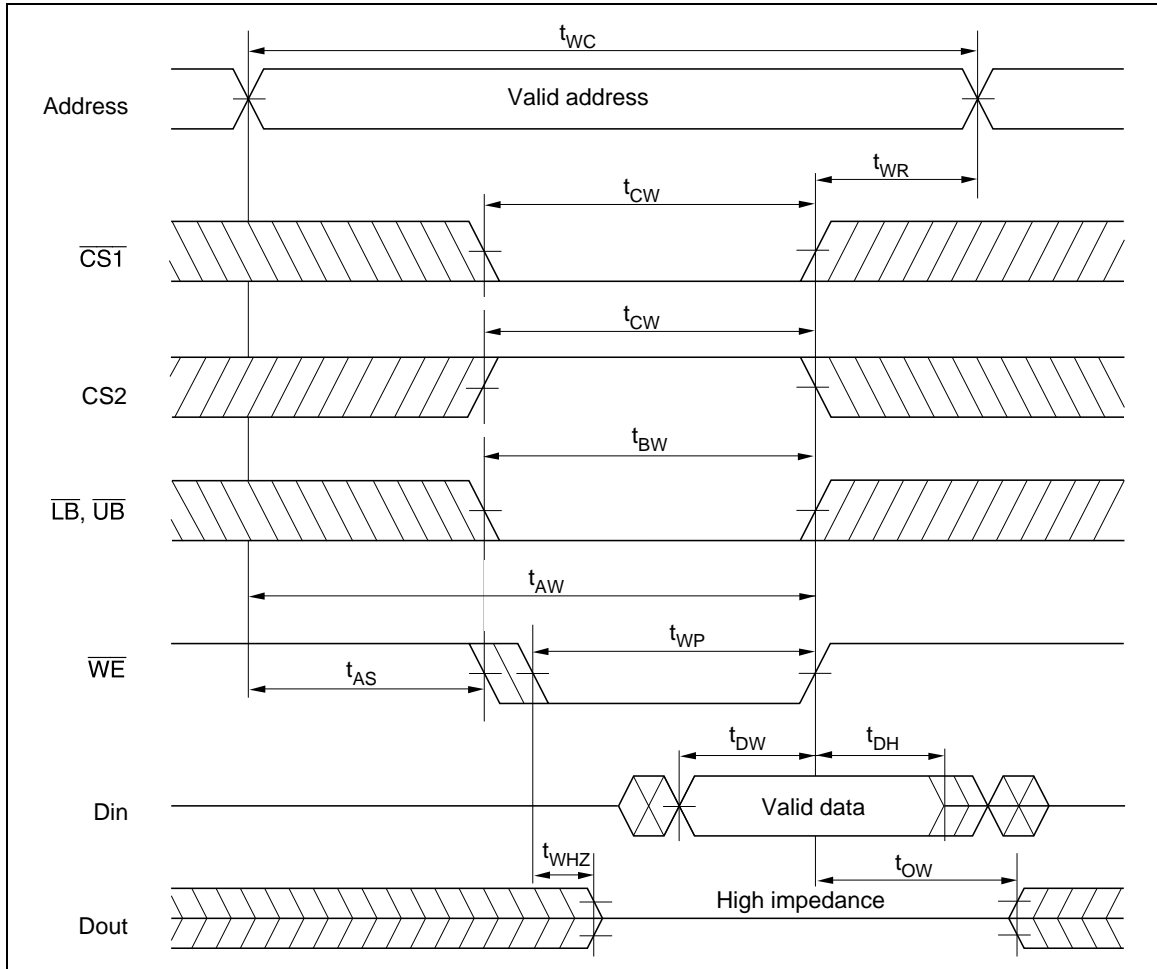
Write Cycle (2) (CS1, CS2 Clock, OE = V$_{IH}$)

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Write Cycle (3) (LB, UB Clock, OE = V_{IH})

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Low V$_{CC}$ Data Retention Characteristics

(Ta = −40 to +85°C)

| Parameter	Symbol	Min	Typ[4]	Max	Unit	Test conditions[3]

V$_{CC}$ for data retention	V$_{DR}$	1.0	—	2.2	V	Vin ≥ 0 V
						(1) 0 V ≤ CS2 ≤ 0.2 V or
						(2) CS2 ≥ V$_{CC}$ − 0.2 V,
						    CS1 ≥ V$_{CC}$ − 0.2 V or
						(3) LB = UB ≥ V$_{CC}$ − 0.2 V,
						    CS2 ≥ V$_{CC}$ − 0.2 V,
						    CS1 ≤ 0.2 V

Data retention current	I$_{CCDR}$[1]	—	0.5	25	µA	V$_{CC}$ = 1.5 V, Vin ≥ 0 V
						(1) 0 V ≤ CS2 ≤ 0.2 V or
						(2) CS2 ≥ V$_{CC}$ − 0.2 V,
						    CS1 ≥ V$_{CC}$ − 0.2 V or
						(3) LB = UB ≥ V$_{CC}$ − 0.2 V,
						    CS2 ≥ V$_{CC}$ − 0.2 V,
						    CS1 ≤ 0.2 V
						Average value

	I$_{CCDR}$[2]	—	0.5	8	µA	
Chip deselect to data retention time	t$_{CDR}$	0	—	—	ns	See retention waveforms
Operation recovery time	t$_R$	5	—	—	ms	

Notes: 1. This characteristic is guaranteed only for L-version.

2. This characteristic is guaranteed only for L-SL version.

3. CS2 controls address buffer, WE buffer, CS1 buffer, OE buffer, LB, UB buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE, OE, CS1, LB, UB, I/O) can be in the high impedance state. If CS1 controls data retention mode, CS2 must be CS2 ≥ V$_{CC}$ − 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, WE, OE, LB, UB, I/O) can be in the high impedance state.

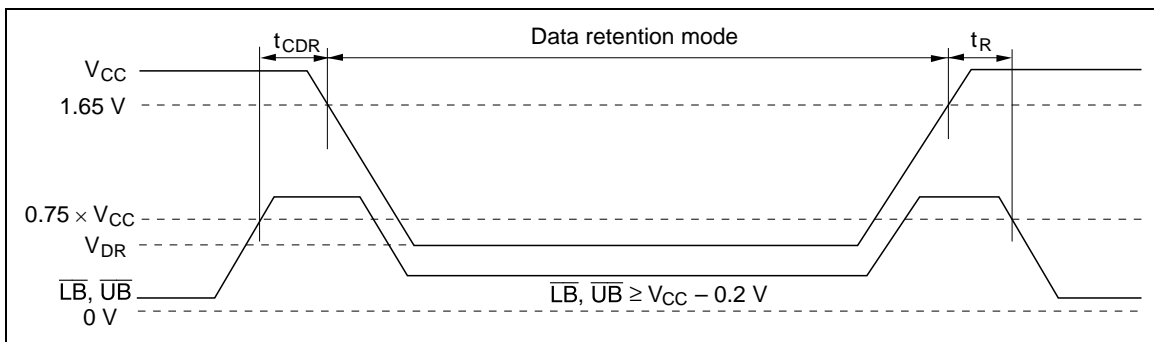4. Typical values are at V$_{CC}$ = 1.5 V, Ta = +25°C and not guaranteed.

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Low V$_{cc}$ Data Retention Timing Waveform (1) (CS1 Controlled)
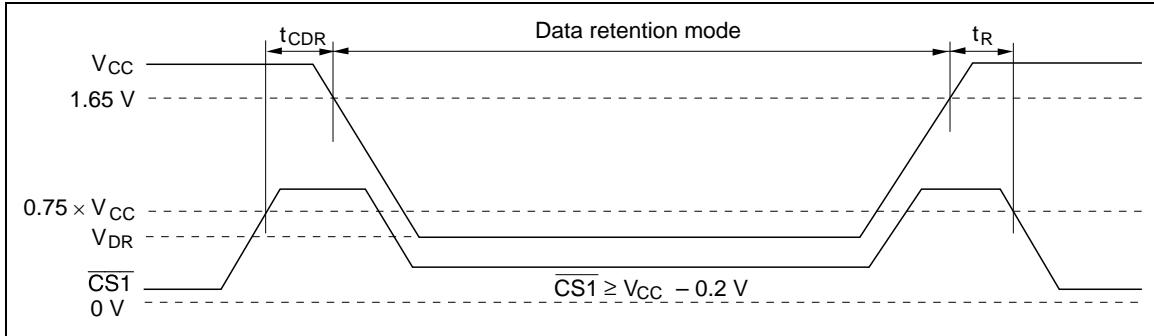
Low V$_{cc}$ Data Retention Timing Waveform (2) (CS2 Controlled)
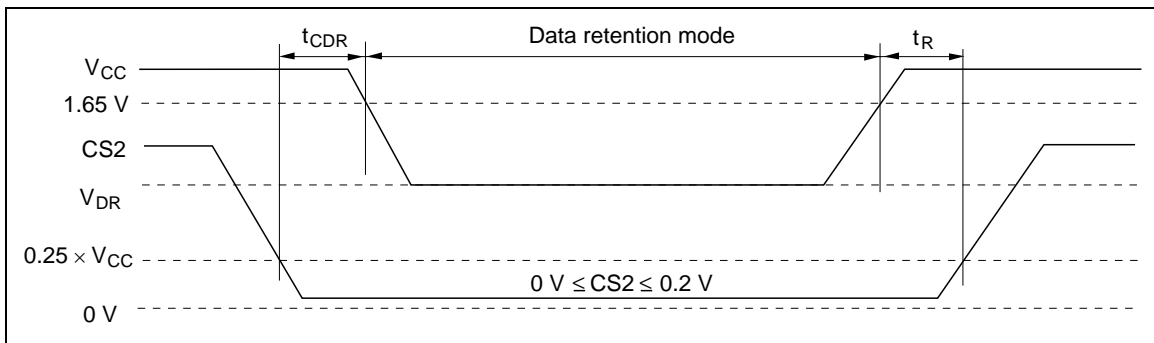
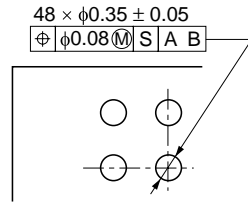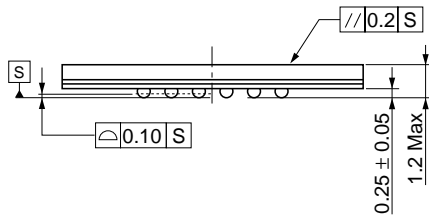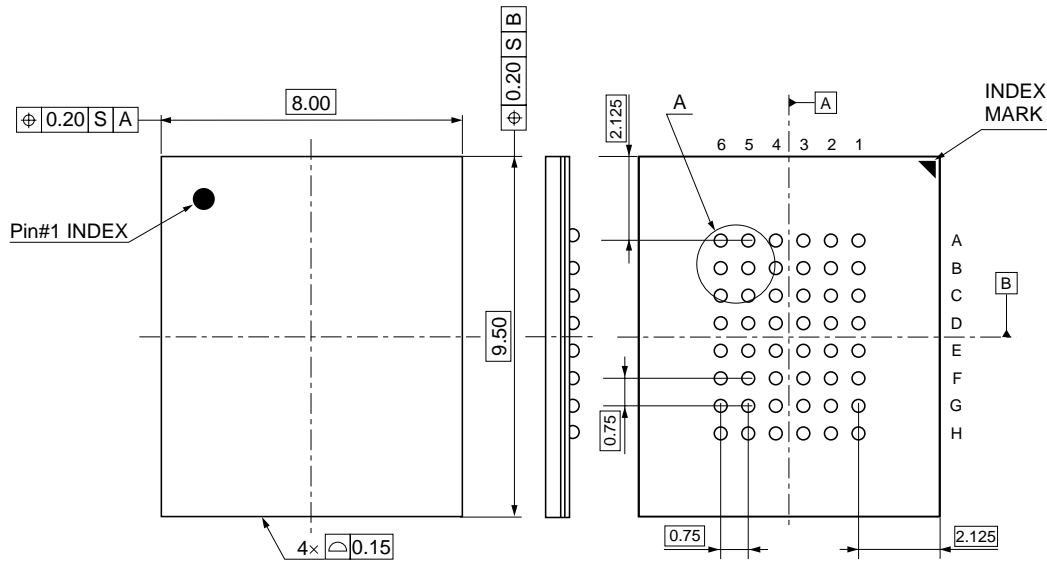**Low V$_{cc}$ Data Retention Timing Waveform (3)** (LB, UB Controlled)

Package Dimensions

HM62A16100LBPI Series (TBP-48F)

As of January, 2003

Unit: mm

INDEX MARK

Pin#1 INDEX

8.00

9.50

0.20 S A

0.20 S B

4× △ 0.15

2.125

0.75

0.75

2.125

6 5 4 3 2 1

A B C D E F G H

A

A

B

// 0.2 S

△ 0.10 S

S

0.25 ± 0.05

1.2 Max

48 × φ0.35 ± 0.05

φ0.08 Ⓜ S A B

Details of the part A

Package Code	TBP-48F
JEDEC	–
JEITA	–
Mass (reference value)	0.15 g

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